

SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDLS135 – DECEMBER 1983 – REVISED MARCH 1988

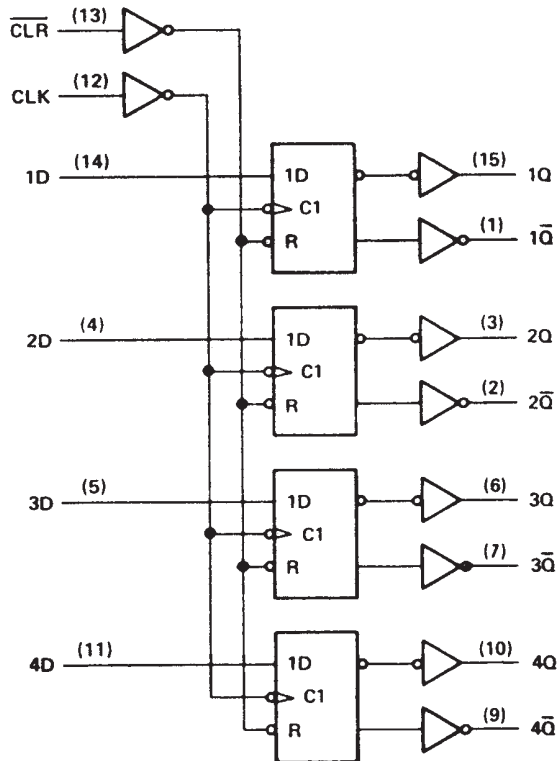
- Contains Four Flip-Flops with Double Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

description

These monolithic, positive-edge triggered flip-flops utilize the latest low-power Schottky circuitry to implement D-type flip-flop logic. They have a direct clear input and complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

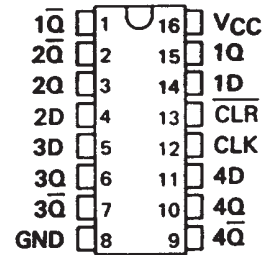
logic diagram (positive logic)



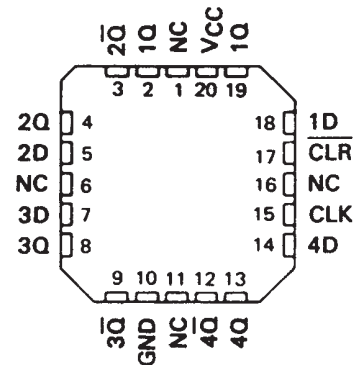
Pin numbers shown are for D, J, N, and W packages.

SN54LS171 . . . J OR W PACKAGE
SN74LS171 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS171 . . . FK PACKAGE
(TOP VIEW)

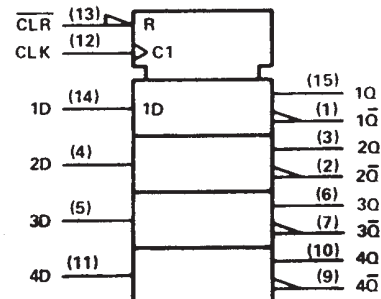


NC-No internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q _O	Q̄ _O

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

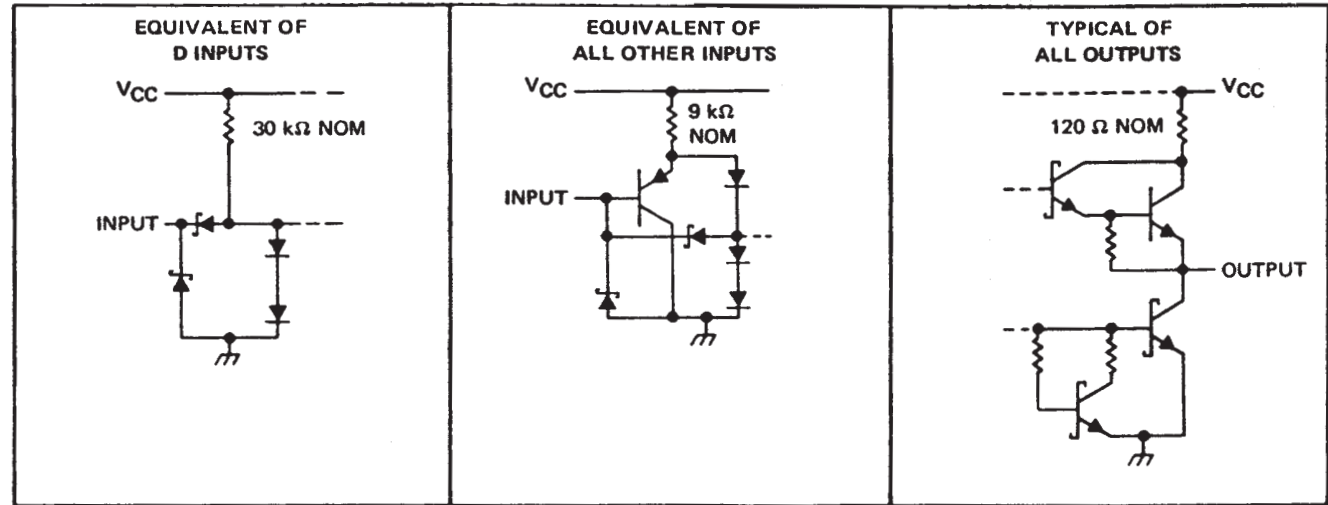
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated

SN54LS171, SN74LS171
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDLS135 – DECEMBER 1983 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS171 Circuits	– 55°C to 125°C
SN74LS171 Circuits	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS171			SN74LS171			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		20	0		20	MHz
t_w	Width of clock or clear pulse	20			20			ns
t_{su}	Setup time	Data input		20	20			ns
		Clear inactive-state		25	25			
t_h	Data hold time	5			5			ns
T_A	Operating free-air temperature	– 55		125	0		70	°C

SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDLS135 – DECEMBER 1983 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS171		SN74LS171		UNIT
					MIN	TYP‡	MAX	MIN	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = − 18 mA		− 1.5		− 1.5		V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = − 1 mA	2.5	3.4	2.7	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
				I _{OL} = 8 mA			0.35	0.5	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL}	Low-level input current	D inputs	V _{CC} = MAX, V _I = 0.4 V		− 0.4		− 0.4		mA
		All others			− 0.2		− 0.2		mA
I _{OS§}	Short-circuit output current		V _{CC} = MAX, V _O = 0 V		− 20	− 100	− 20	− 100	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 1		14	25	14	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS171			UNIT
				MIN	TYP	MAX	
f _{max}			R _L = 2 kΩ, C _L = 15 pF	20	30		MHz
t _{PLH}	CLK	Q, $\overline{Q}$			15	25	ns
t _{PHL}					18	30	ns
t _{PLH}					18	30	ns
t _{PHL}	$\overline{\text{CLR}}$	Q			24	40	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.