9 CLK

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Common Positive-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Fully Buffered Outputs
- Typical Clock Input Frequency . . . 45 MHz

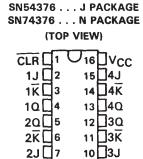
description

These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by as much as 50%. They feature hysteresis at the clock input, fully buffered outputs, and direct clear capability. The positive-edge-triggered SN54376 and SN74376 are directly compatible with most Series 54/74 MSI registers.

The SN54376 is characterized for operation over the full military temperature range of -55°C to 125°C; the SN74376 is characterized for operation from 0°C to 70°C.

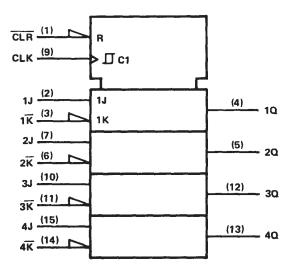
FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INP	UTS	OUTPUT		
CLEAR	CLOCK	J	ĸ	α		
L	Х	X	Х	L		
н	†	L	Н	σ_0		
н	†	Н	Н	н		
н	†	L	L	L		
н	†	.н	L	TOGGLE		
Н	L	×	×	a_0		



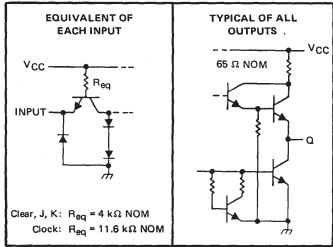
GND □8

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



Resistor values shown are nominal.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		7 V
Input voltage		5.5 V
Operating free-air temperature range:	SN5437655	5°C to 125°C
operating mee an emperation anger	SN74376	0°C to 70°C
	65	

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54376		SN74376			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-800			-800	μΑ
Low-level output current, IOL				16			16	mA
Clock frequency		0		30	0		30	MHz
Puise width, t _W	Clock high	22			22			
	Clock low	12			12			ns
	Preset or clear low	12			12			
Setup time, t _{su}	J, K inputs	01			01			ns
	Clear inactive state	10↑			10↑			113
Input hold time, th		201			201			ns
Operating free-air temperature, TA		-55		125	0		70	°C

^{↑↓}The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge,

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					8.0	V
VIK	Input clamp voltage	V _{CC} = MIN,	I _I = -12 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{1H} = 2 V, I _{OH} = -800 μA	2.4	3,4		٧
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4	V
I _I	Input current at maximum input voltage	VCC = MAX,	V _I = 5.5 V			1	mA
Тін	High-level input current	V _{CC} = MAX,	V _I = 2.4 V			40	μΑ
TIL	Low-level input current	V _{CC} = MAX,	V ₁ = 0.4 V			-1.6	mA
los	Short-circuit output current§	V _{CC} = MAX		-30		-85	mA
ICC	Supply current	V _{CC} = MAX			52	74	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency	C 15 pF	30	45		MHz
tPHL	Propagation delay time, high-to-low-level output from clear	$C_L = 15 pF$, $R_L = 400 \Omega$,		17	30	ns
tPLH	Propagation delay time, low-to-high-level output from clock	See Note 2		22	35	ns
tPHL	Propagation delay time, high-to-low-level output from clock	366 IAO(6.2		24	35	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



 $^{^{\}ddagger}$ Ail typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}$ C.

[§]Not more than one output should be shorted at a time.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated