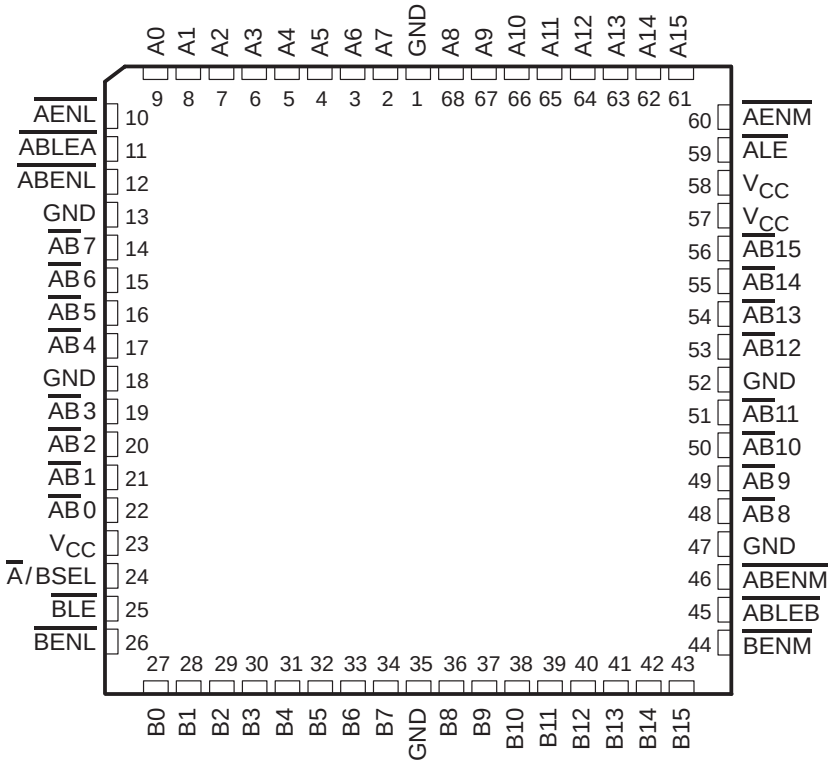
SDIS013 – JULY 1989 – REVISED AUGUST 1990

- **Multiplexed Real-Time and Latched Data**
- **Byte Control for Byte-Write Applications**
- **Useful in NuBus™ Interface Applications**
- **Useful in Memory Interleave Applications**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas Instruments Quality and Reliability**

SN74BCT2423A . . . FN PACKAGE
(TOP VIEW)



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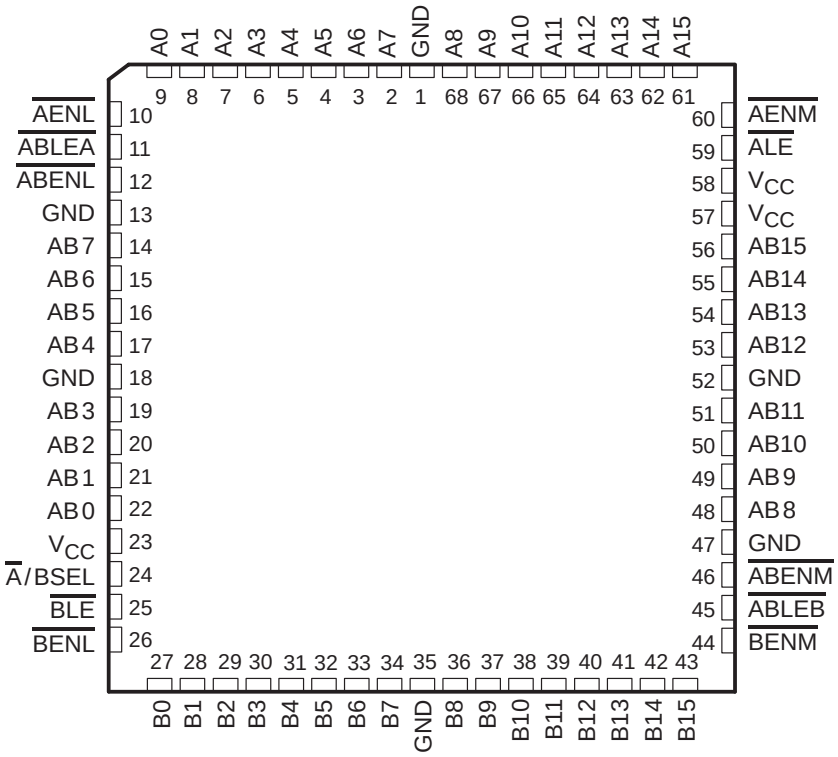
SN74BCT2424A . . . FN PACKAGE
(TOP VIEW)



description

The ’BCT2423A and ’BCT2424A are general-purpose 16-bit bidirectional transceivers with data storage latches and byte control circuitry arranged for use in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. These devices are also useful in memory-interleaving applications. The ’BCT2423A and ’BCT2424A offer inverted and noninverted data paths, respectively.

The ’BCT2423A and ’BCT2424A were designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics, but also greatly reduces the standby power of the device when disabled. This is valuable when the device is not performing an address or data transfer.

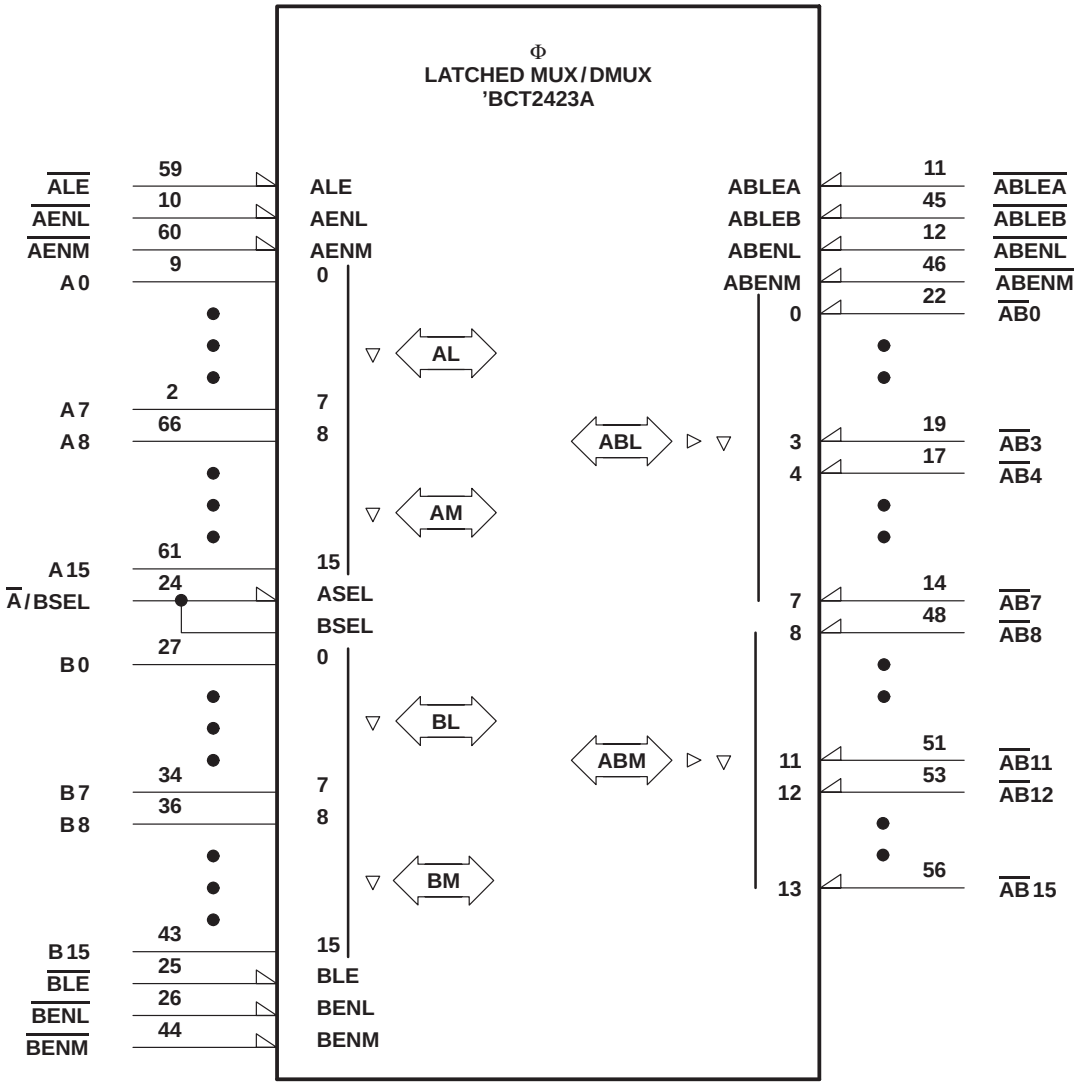
Three 16-bit I/O ports, A15–A0, B15–B0, and AB15–AB0 are available for address and/or data transfer. The $\overline{\text{AENM}}$, $\overline{\text{AENL}}$, $\overline{\text{BENM}}$, $\overline{\text{BENL}}$, $\overline{\text{ABENM}}$, and $\overline{\text{ABENL}}$ inputs control the bus transceiver functions. These control signals also allow byte-control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The $\overline{\text{ALE}}$, $\overline{\text{BLE}}$, $\overline{\text{ABLEA}}$, and $\overline{\text{ABLEB}}$ inputs are active low, and are used to control data storage. When the latch enable input is low, the latch is transparent. When the latch enable input goes high, the data present at the inputs is latched, and remains latched until the latch enable input is returned low.

Data on the ’A’ bus and ’B’ bus are multiplexed onto the ’AB’ bus via the $\overline{\text{A}}$/BSEL control line. When $\overline{\text{A}}$/BSEL is low, A15–A0 is mapped to the AB15–AB0 outputs. When $\overline{\text{A}}$/BSEL is high, B15–B0 is mapped to the AB15–AB0 outputs.

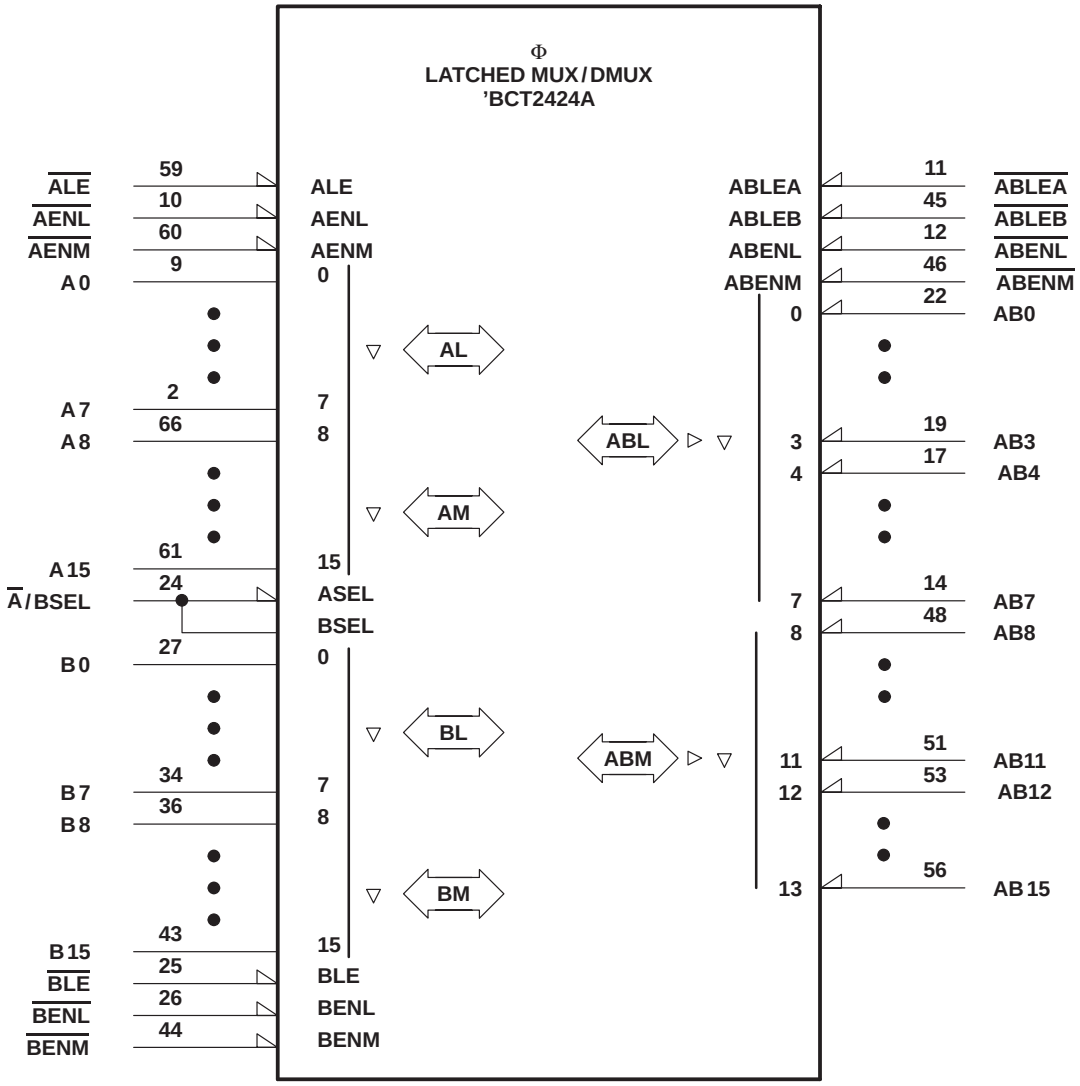
The SN74BCT2423A and SN74BCT2424A are characterized for operation from 0°C to 70°C.

logic symbol for the ’BCT2423A†



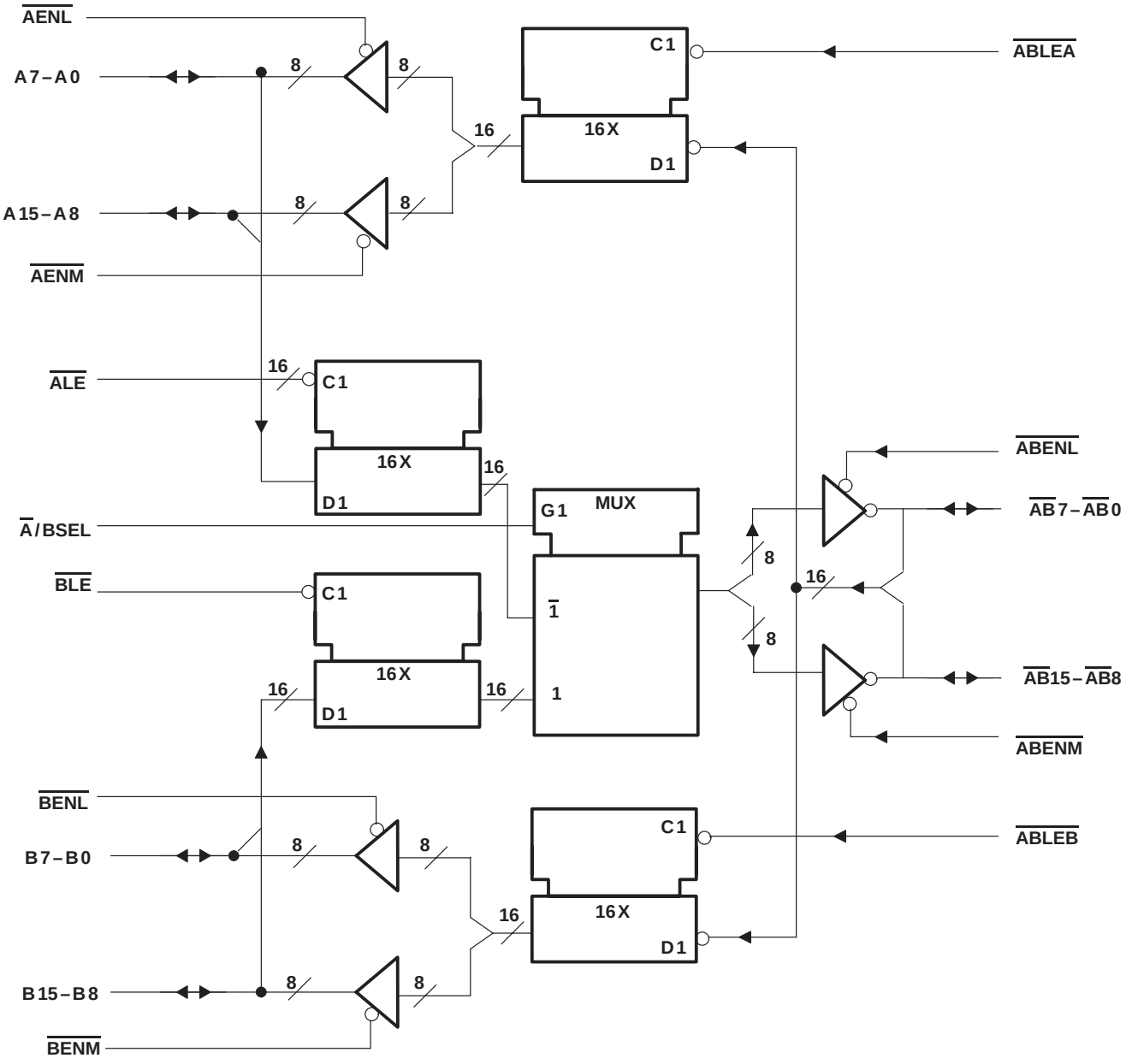
† These logic symbols are in accordance with ANSI/IEEE Std 91-1984.

logic symbol for the ’BCT2424A†

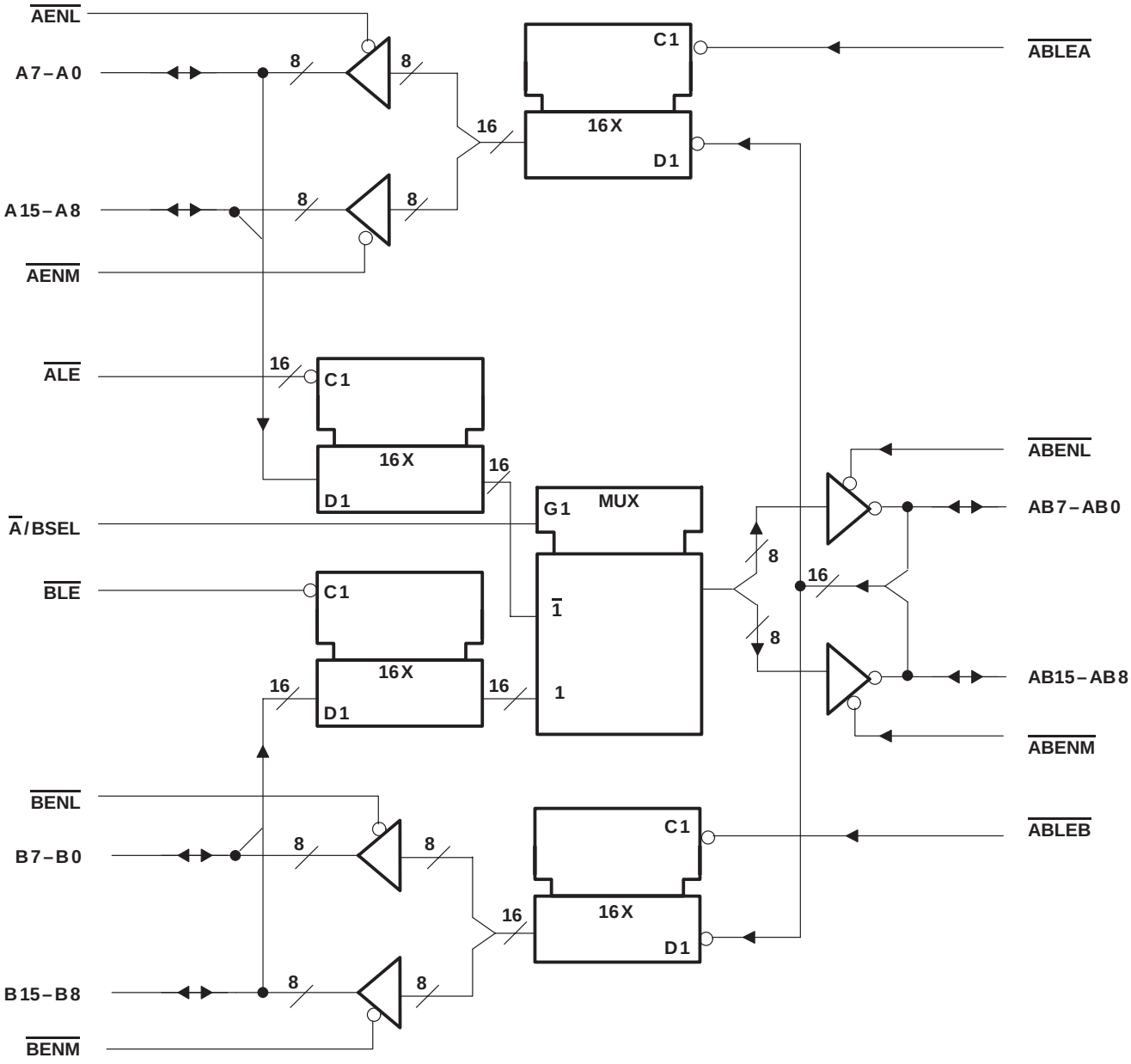


† These logic symbols are in accordance with ANSI/IEEE Std 91-1984.

logic diagram for ’BCT2423A (positive logic)



logic diagram for ’BCT2424A (positive logic)



Terminal Functions

TERMINAL PINS	DESCRIPTION
A15–A0	A bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the A bus and the AB bus is inverting for the ’BCT2423A and noninverting for the ’BCT2424A.
$\overline{AB}$15–$\overline{AB}$0 (’BCT2423A) AB15–AB0 (’BCT2424A)	AB Bus. This 16-bit i/o port allows for multiplexed transmission of data and/or address information to or from the A and B buses. Information transfer between the A, B, and AB buses is inverting for the ’BCT2423A and noninverting for the ’BCT2424A.
$\overline{ABENL}$	AB Bus Output Enable, Least Significant Byte. This active-low input is used to enable the AB7–AB0 outputs. When this input is high, the AB7–AB0 outputs are in the high-impedance state allowing for data input.
$\overline{ABENM}$	AB Bus Latch Enable, Most Significant Byte. This active-low input is used to enable the AB15–AB8 outputs. When this input is high, the AB15–AB8 outputs are in the high-impedance state allowing for data input.
$\overline{ABLEA}$	AB Bus Latch Enable to A Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15–AB0) to be transferred to the A bus (A15–A0). When $\overline{ABLEA}$ is low, the latch is transparent. When $\overline{ABLEA}$ transitions to the high level, the data present at the AB15 – AB0 inputs is latched, and it remains latched while $\overline{ABLEA}$ is high.
$\overline{ABLEB}$	AB Bus Latch Enable to B Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15–AB0) to be transferred to the B bus (B15–B0). When $\overline{ABLEB}$ is low, the latch is transparent. When $\overline{ABLEB}$ transitions to the high level, the data present at the AB15 – AB0 inputs is latched, and it remains latched while $\overline{ABLEB}$ is high.
$\overline{A}$/BSEL	A/B Select Control. This input controls the A/B multiplexer. When the input is low, the A15–A0 is selected as input to the AB15–AB0 outputs. When the input is high, B15–B0 is selected as input to the AB15–AB0 outputs.
$\overline{AENL}$	A Bus Output Enable, Least Significant Byte. This active-low input is used to enable the A7–A0 outputs. When this input is high, the A7–A0 outputs are in the high-impedance state allowing for data input.
$\overline{AENM}$	A Bus Output Enable, Most Significant Byte. This active-low input is used to enable the A15–A8 outputs. When this input is high, the A15–A8 outputs are in the high-impedance state allowing for data input.
$\overline{ALE}$	A Bus Latch Enable. This active-low input is used to control the latch that holds data received from the A bus (A15–A0). When $\overline{ALE}$ is low, that latch is transparent. When $\overline{ALE}$ transitions to the high level, the data present at the A15–A0 inputs is latched and remains latched while $\overline{ALE}$ is high.
B15–B0	B Bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the B bus and the AB bus is inverting for the ’BCT2423A and noninverting for the ’BCT2424A.
$\overline{BENL}$	B Bus Output Enable, Least Significant Byte. This active-low input is used to enable the B7–B0 outputs. When this input is high, the B7–B0 outputs are in the high-impedance state allowing for data input.
$\overline{BENM}$	B Bus Output Enable, Most Significant Byte. This active-low input is used to enable the B15–B8 outputs. When this input is high, the B15–B8 outputs are in the high-impedance state allowing for data input.
$\overline{BLE}$	B Bus Latch Enable. This active-low input is used to control the latch that holds data received from the B bus (B15–B0). When $\overline{BLE}$ is low, that latch is transparent. When $\overline{BLE}$ transitions to the high level, that data present at the B15–B0 inputs is latched and remains latched while $\overline{BLE}$ is high.

Function Tables

DIRECTION A OR B TO AB										
INPUTS							OUTPUTS			
							’BCT2423A		’BCT2424A	
Ax	Bx	$\overline{\text{ALE}}$	$\overline{\text{BLE}}$	A/$\overline{\text{B}}$SEL	$\overline{\text{ABENM}}$	$\overline{\text{ABENL}}$	$\overline{\text{AB}}$ 15–8	$\overline{\text{AB}}$ 7–0	AB 15–8	AB 7–0
H	X	L	X	L	L	L	L		H	
L	X	L	X	L	L	L	H		L	
X	X	H	X	L	L	L	$\overline{AB}_0$		AB_0	
X	H	X	L	H	L	L	L		H	
X	L	X	L	H	L	L	H		L	
X	X	X	H	H	L	L	$\overline{AB}_0$		AB_0	
X	X	X	X	X	L	L	Active	Active	Active	Active
X	X	X	X	X	L	H	Active	Z	Active	Z
X	X	X	X	X	H	L	Z	Active	Z	Active
X	X	X	X	X	H	H	Z	Z	Z	Z

DIRECTION AB TO A OR B								
INPUTS					OUTPUTS			
$\overline{\text{ABx}}$ ABx	ABLEA	ABLEB	$\overline{\text{AENL}}$† $\overline{\text{AENM}}$†	$\overline{\text{BENL}}$† $\overline{\text{BENM}}$†	’BCT2423A		’BCT2424A	
					Ax	Bx	Ax	Bx
H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	H	L	L
H	L	H	L	L	L	B_0	H	B_0
L	L	H	L	L	H	B_0	L	B_0
H	H	L	L	L	A_0	L	A_0	H
L	H	L	L	L	A_0	H	A_0	L
X	H	H	L	L	A_0	B_0	A_0	B_0
X	X	X	L	L	Active	Active	Active	Active
X	X	X	L	H	Active	Z	Active	Z
X	X	X	H	L	Z	Active	Z	Active
X	X	X	H	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance.

A_0, B_0, AB_0, $\overline{AB}_0$ = no change since the controlling latch enable went high

† The least significant bytes (A7-A0 and B7-B0) and the most significant bytes (A15-A8 and B15-B8) can be independently enabled and disabled, as was illustrated for the $\overline{\text{AB}}$ and AB bytes in the upper function table.

absolute maximum ratings over operating free-air temperature range(unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65° to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A_X, B_X outputs			–15	mA
		$\overline{AB}_X$ or AB_X outputs			–15	
I_{OL}	Low-level output current	A_X, B_X outputs			24	mA
		$\overline{AB}_X$ or AB_X outputs			48	
t_w	Pulse duration	$\overline{ABLEA}$, $\overline{ABLEB}$ high or low	12.5			ns
		$\overline{ALE}$, $\overline{BLE}$ high or low	12.5			
t_{su}	Setup time	Data before $\overline{xLEx}$ ↑	10			ns
t_h	Hold time	Data after $\overline{xLEx}$ ↑	2			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –400 μA	V_{CC} – 1.5			V
		V_{CC} = 4.75 V,	I_{OH} = –3 mA	2.8	3.6		
		V_{CC} = 4.75 V,	I_{OH} = –15 mA	2			
V_{OL}	A_X, B_X outputs	V_{CC} = 4.75 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	
	A_X, B_X outputs	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.25	0.4	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			100	μA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20 –100	μA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V			–200	μA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0	–60		–225	mA
I_{CC}	Enabled	V_{CC} = 5.25 V,	V_{IL} = 0.5 V,		110	170	mA
	Disabled	V_{IH} = 3 V,	Outputs open		20	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{IH} and I_{IL} include the offstate output current.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

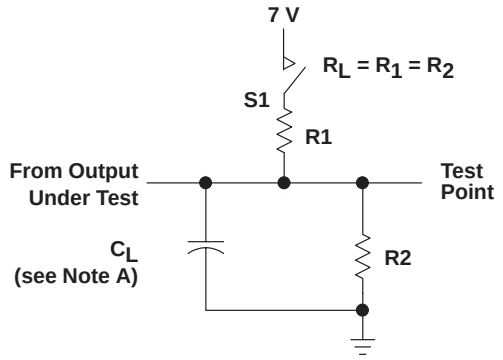
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
t_{pd}	$\overline{ABx}$, ABx	Ax	V_{CC} = 4.75 V to 5.25 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX		8	12	ns
t_{pd}	$\overline{ABx}$, ABx	Bx			8	12	ns
t_{pd}	Ax	$\overline{ABx}$, ABx			9	12	ns
t_{pd}	Bx	$\overline{ABx}$, ABx			9	12	ns
t_{pd}	$\overline{ALE}$ ↓	$\overline{ABx}$, ABx			10	13	ns
t_{pd}	$\overline{BLE}$ ↓	$\overline{ABx}$, ABx			10	13	ns
t_{pd}	$\overline{ABLEA}$ ↓	Ax			8	12	ns
t_{pd}	$\overline{ABLEB}$ ↓	Bx			8	12	ns
t_{pd}	$\overline{A}$/BSEL	$\overline{ABx}$, ABx			8	12	ns
t_{en}	$\overline{AENM}$, $\overline{AENL}$	Ax			10	13	ns
t_{en}	$\overline{BENM}$, $\overline{BENL}$	Bx			10	13	ns
t_{en}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{ABx}$, ABx			10	13	ns
t_{dis}	$\overline{AENM}$, $\overline{AENL}$	Ax			5	10	ns
t_{dis}	$\overline{BENM}$, $\overline{BENL}$	Bx			5	10	ns
t_{dis}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{ABx}$, ABx			5	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ See Parameter Measurement Information for load circuit and voltage waveforms.

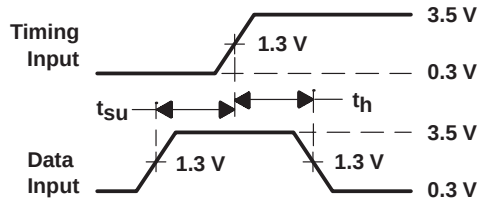
PARAMETER MEASUREMENT INFORMATION

SWITCH POSITION TABLE

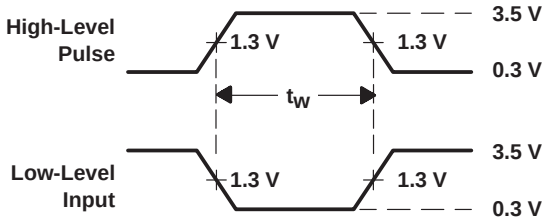
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



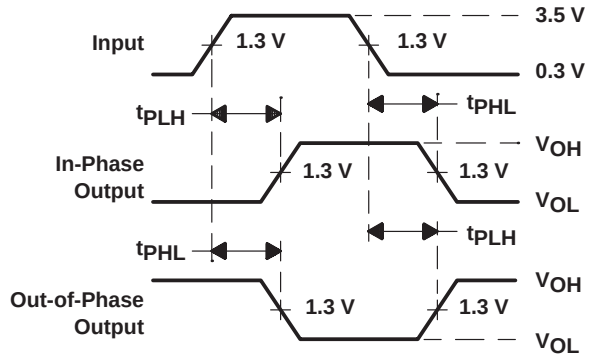
LOAD CIRCUIT



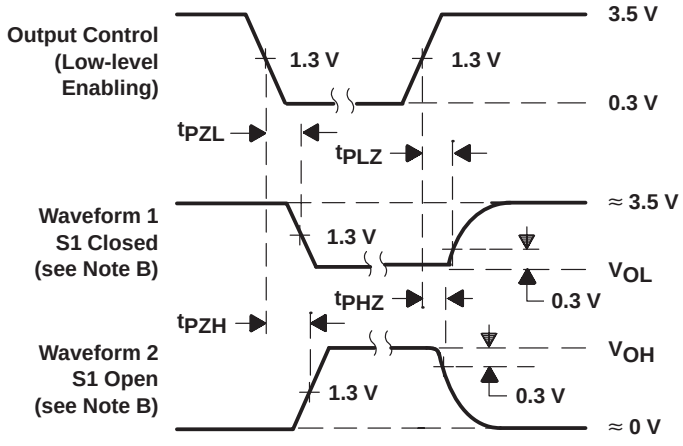
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

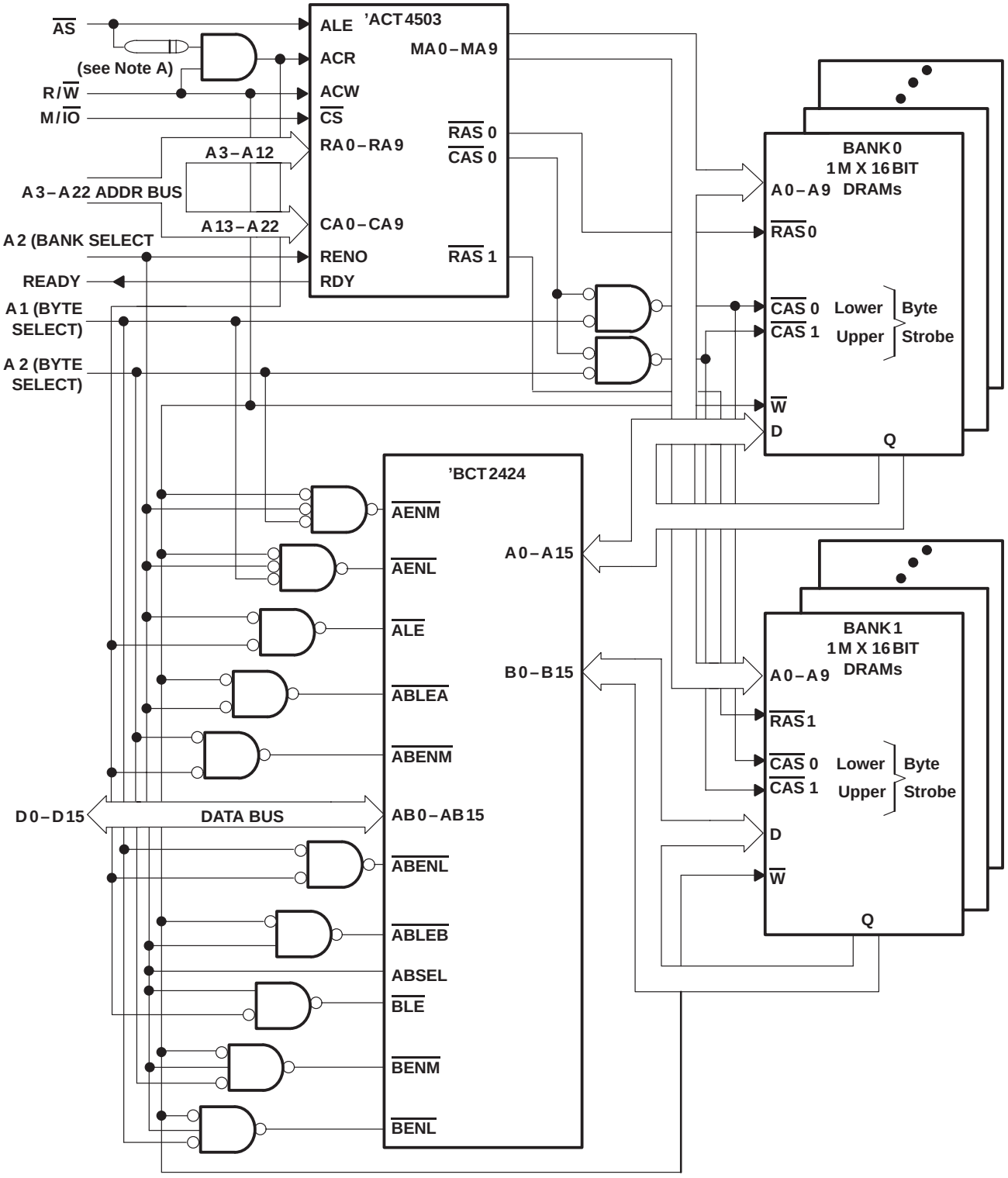


VOLTAGE WAVEFORMS
ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Wafeform 1 is for an output with internal conditions such that the output is low except when disabled by the current control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1

APPLICATION INFORMATION



NOTE A: The value of this delay element is dependent on the speed of the microprocessor.

Figure 2. Typical Memory Interleave Application

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