

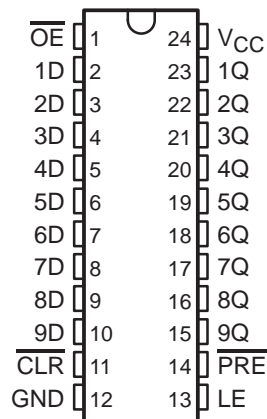
# SN74ALS843

## 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS232A – DECEMBER 1983 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



### description

This 9-bit bus-interface D-type latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches with noninverting data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input places the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS843 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUT Q
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

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Pin diagram of the 74VHC163 3-bit counter. The chip has 23 pins. Control pins on the left include OE (pin 1), PRE (pin 14), CLR (pin 11), and LE (pin 13). Data pins on the left include 1D (pin 2), 2D (pin 3), 3D (pin 4), 4D (pin 5), 5D (pin 6), 6D (pin 7), 7D (pin 8), 8D (pin 9), and 9D (pin 10). Control pins on the right include EN (pin 23) and S2 (pin 22). Data pins on the right include 1Q (pin 21), 2Q (pin 20), 3Q (pin 19), 4Q (pin 18), 5Q (pin 17), 6Q (pin 16), 7Q (pin 15), 8Q (pin 14), and 9Q (pin 13). The chip is labeled with 'EN', 'S2', 'R', 'C1', and '1D'.

The diagram illustrates the internal structure of a single channel of a 24-bit shift register. It features a 74164 shift register with the following inputs and outputs:

- Inputs:**
  - $\overline{OE}$  (Pin 1): Inverted output enable.
  - $\overline{PRE}$  (Pin 14): Inverted preset.
  - $\overline{CLR}$  (Pin 11): Inverted clear.
  - $LE$  (Pin 13): Latch enable.
  - $1D$  (Pin 2): Data input 1.
- Internal Structure:**
  - The shift register has four internal nodes:  $S$ ,  $C1$ ,  $1D$ , and  $R$ .
  - The  $1D$  input is connected to the  $1D$  node.
  - The  $LE$  input is connected to the  $S$  node.
  - The  $\overline{CLR}$  input is connected to the  $R$  node.
  - The  $\overline{PRE}$  input is connected to the  $C1$  node.
  - The  $\overline{OE}$  input is connected to the  $S$  node.
- Outputs:**
  - $Q$  (Pin 23): The output of the shift register, which is inverted and fed back to the  $1D$  input.
  - To Eight Other Channels:** A bus indicating that this channel is part of a larger 24-bit register.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–2.6	mA
$I_{OL}$	Low-level output current			24	mA
$t_w$	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low		35	ns
		LE high		20	
$t_{su}$	Setup time, data before LE↓	10			ns
$t_h$	Hold time, data after LE↓	5			ns
$T_A$	Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA	2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	V
		$I_{OL} = 24$ mA		0.35	
$I_{OZH}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			20	μA
$I_{OZL}$	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–20	μA
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.1	mA
$I_{O\$}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
$I_{CC}$	$V_{CC} = 5.5$ V	Outputs high		21	mA
		Outputs low		41	
		Outputs disabled		25	

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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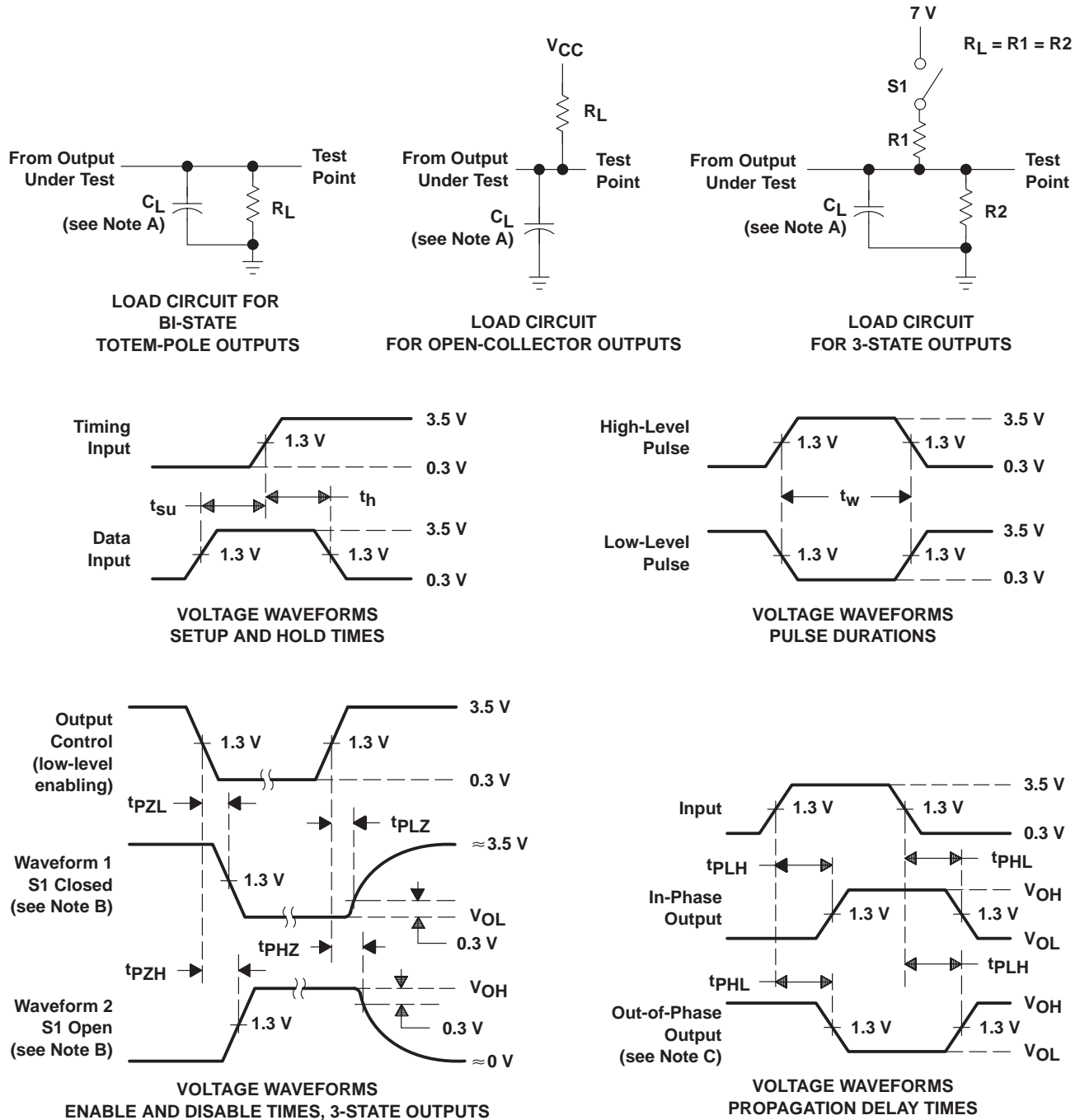
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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	MAX	
t <sub>PLH</sub>	D	Q	2	13	ns
t <sub>PHL</sub>			4	18	
t <sub>PLH</sub>	LE	Q	5	21	ns
t <sub>PHL</sub>			8	26	
t <sub>PLH</sub>	$\overline{\text{PRE}}$	Q	5	22	ns
t <sub>PHL</sub>	$\overline{\text{CLR}}$		6	23	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	2	12	ns
t <sub>PZL</sub>			4	14	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	2	10	ns
t <sub>PLZ</sub>			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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