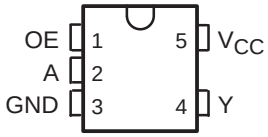
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline Transistor (DBV, DCK) Packages**

DBV OR DCK PACKAGE
(TOP VIEW)



description

The SN74AHC1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74AHC1G126 is characterized for operation from –40°C to 85°C.

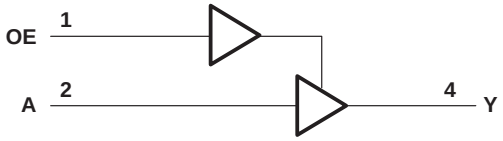
FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package . . . . . 347°C/W
DCK package . . . . . 389°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μA
I_{OZ}	$V_I = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1		10	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		10				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.6	8	1	9.5	ns
t_{PHL}					5.6	8	1	9.5	
t_{PZH}	OE	Y	C_L = 15 pF		5.4	8	1	9.5	ns
t_{PZL}					5.4	8	1	9.5	
t_{PHZ}	OE	Y	C_L = 15 pF		7	9.7	1	11.5	ns
t_{PLZ}					7	9.7	1	11.5	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	ns
t_{PHL}					8.1	11.5	1	13	
t_{PZH}	OE	Y	C_L = 50 pF		7.9	11.5	1	13	ns
t_{PZL}					7.9	11.5	1	13	
t_{PHZ}	OE	Y	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

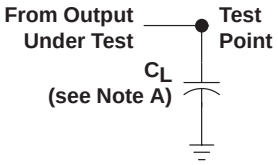
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PZH}	OE	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}					3.6	5.1	1	6	
t_{PHZ}	OE	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

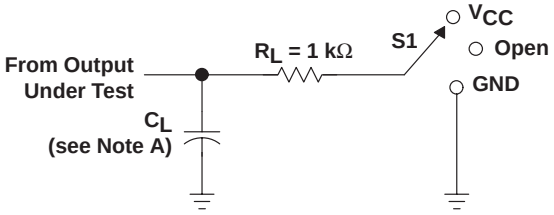
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

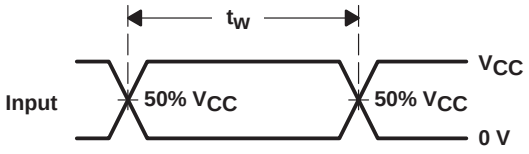


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

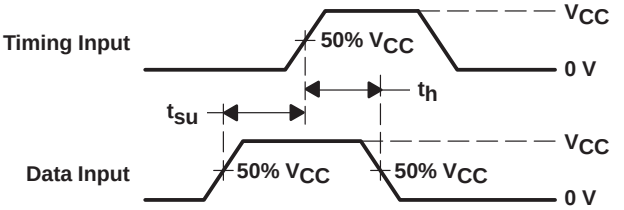


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

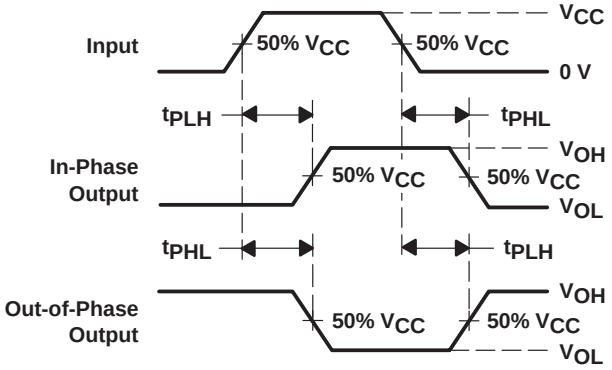
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



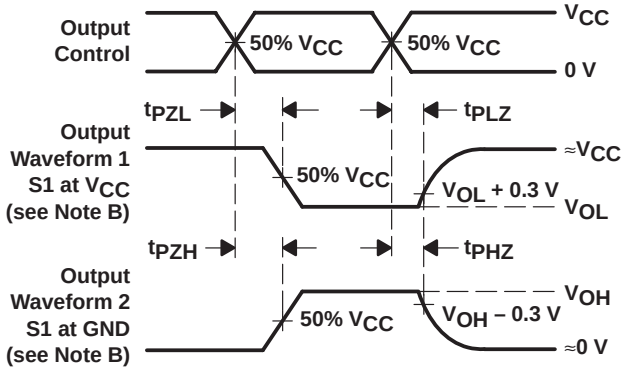
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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