

High Speed CMOS Logic 4-Bit Binary Full Adder with Fast Carry

Features

- Adds Two Binary Numbers
- Full Internal Lookahead
- Fast Ripple Carry for Economical Expansion
- Operates with Both Positive and Negative Logic
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC283 and 'HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

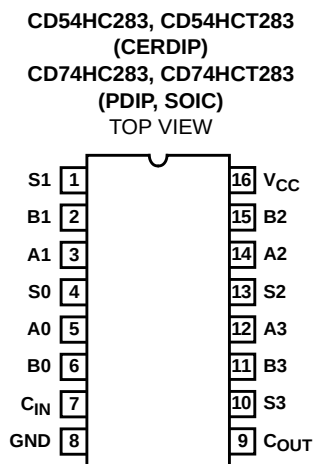
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC283F3A	-55 to 125	16 Ld CERDIP
CD74HC283E	-55 to 125	16 Ld PDIP
CD74HC283M	-55 to 125	16 Ld SOIC
CD54HCT283F3A	-55 to 125	16 Ld CERDIP
CD74HCT283E	-55 to 125	16 Ld PDIP
CD74HCT283M	-55 to 125	16 Ld SOIC

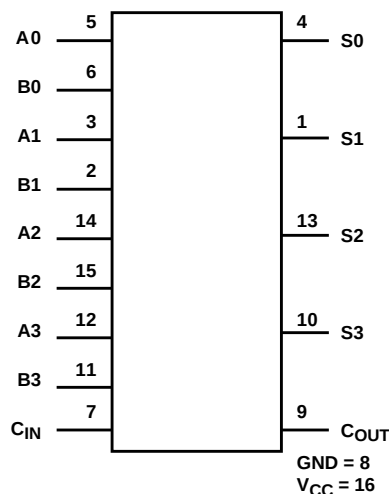
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout



Functional Diagram



CD54/74HC283, CD54/74HCT283

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
SOIC Package	160
Maximum Junction Temperature	$150^{\circ}C$
Maximum Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	$300^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T_A	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	$.2V$ to $6V$
DC Input or Output Voltage, V_I , V_O	$0V$ to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
-			-	-	-	-	-	-	-	-	V	
-			4.5	3.98	-	-	3.84	-	3.7	-	V	
-5.2			6	5.48	-	-	5.34	-	5.2	-	V	
High Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	µA

CD54/74HC283, CD54/74HCT283

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT Types												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IL} or V _{IH}	-	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads	V _{OH}	V _{IL} or V _{IH}	-	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	-	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	-	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	ICC	V _{CC} or GND	-	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
C _{IN}	1.5
B1, A1, A0	1
B0	0.4
B3, A3, A2, B2	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay C _{IN} to S0	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C _L = 15pF	5	-	13	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	27	-	34	-	41	ns

CD54/74HC283, CD54/74HCT283

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{IN} to S1	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	31	-	38	-	46	ns
C_{IN} to S2, C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	33	-	42	-	50	ns
C_{IN} to S3	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	230	-	290	-	345	ns
			4.5	-	-	46	-	58	-	69	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	39	-	49	-	59	ns
An, Bn to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	33	-	42	-	50	ns
An, Bn to Sn	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	-	5	-	70	-	-	-	-	-	pF

HCT TYPES

Propagation Delay C_{IN} to S0	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	13	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	31	-	39	-	47	ns
C_{IN} to S1	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	43	-	54	-	65	ns
C_{IN} to S2, C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	46	-	58	-	69	ns
C_{IN} to S3	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	22	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	53	-	66	-	80	ns
An, Bn to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	20	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	48	-	60	-	72	ns
An, Bn to Sn	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	49	-	61	-	74	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns

CD54/74HC283, CD54/74HCT283

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	-	5	-	82	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

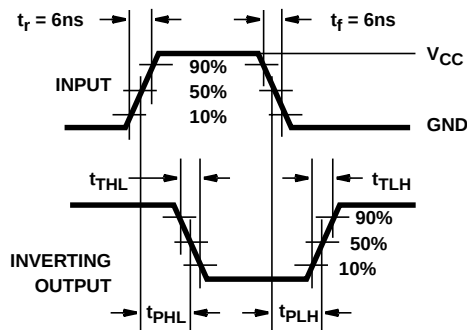


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

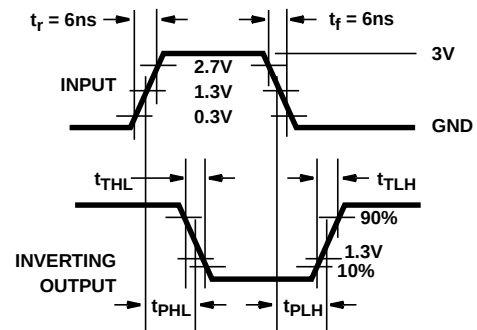


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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