INT202

Low-side Driver IC

Low-side Drive and High-side Control for Simultaneous Conduction

Product Highlights

5 V CMOS Compatible Control Inputs

- Combines logic inputs for low and high-side drives
- Schmidt-triggered inputs for noise immunity

Built-in High-voltage Level Shifters

- Integrated level shifters simplify high-side interface
- Can withstand up to 800 V for direct interface to the INT201 high-side driver
- Pulsed high-voltage level shifters reduce power consumption

Gate Drive Output for an External MOSFET

- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Features

- UV lockout

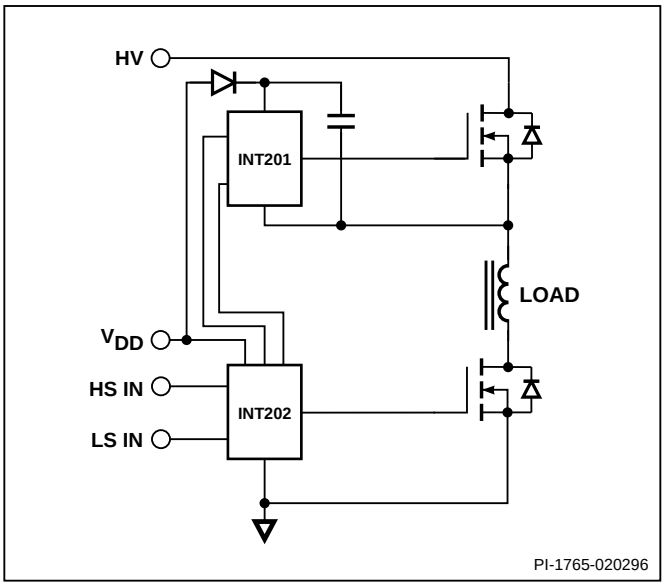


Figure 1. Typical Application

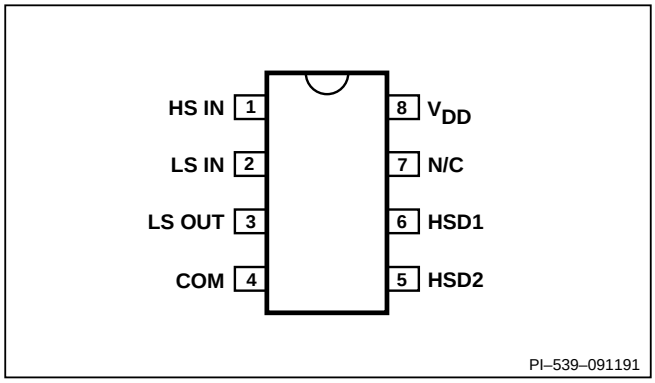


Figure 2. Pin Configuration.

Description

The INT202 Low-side driver IC provides gate drive for an external low-side MOSFET switch and high-side level shifting. When used in conjunction with the INT201 high-side driver, the INT202 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads. The INT202 is designed to be used with rectified 110 V or 220 V supplies. Both high side and low side switches can be controlled independently from ground-referenced 5 V logic inputs on the low side driver.

Pulsed level shifting saves power and provides enhanced noise immunity. The circuit is powered from a nominal 15 V supply to provide adequate gate drive for external N-channel MOSFETs.

Applications include switched reluctance motor drives. The INT202 can also be used to implement multi-phase configurations.

The INT202 is available in 8-pin plastic DIP and SOIC packages.

ORDERING INFORMATION		
PART NUMBER	**PACKAGE OUTLINE**	**ISOLATION VOLTAGE**
INT202PFI1	PO8A	600 V
INT202TFI1	TO8A	600 V
INT202PFI2	PO8A	800 V
INT202TFI2	TO8A	800 V

Pin Functional Description

Pin 1:
Active-high logic-level input **HS IN** controls the pulse circuit which signals the INT201 high-side driver.

Pin 2:
Active-high logic level input **LS IN** controls the low side driver output.

Pin 3:
LS OUT is the driver output which controls the low-side MOSFET.

Pin 4:
COM connection; analog reference point for the circuit.

Pin 5:
Level shift output **HSD 2** signals the high-side driver to turn off. One short, precise pulse is sent on each positive transition of HS IN.

Pin 6:
Level shift output **HSD 1** signals the high-side driver to turn on. Two short, precise pulses are sent on each negative transition of HS IN.

Pin 7:
N/C for creepage distance.

Pin 8:
V_{DD} supplies power to the logic, high-side interface, and low-side driver.

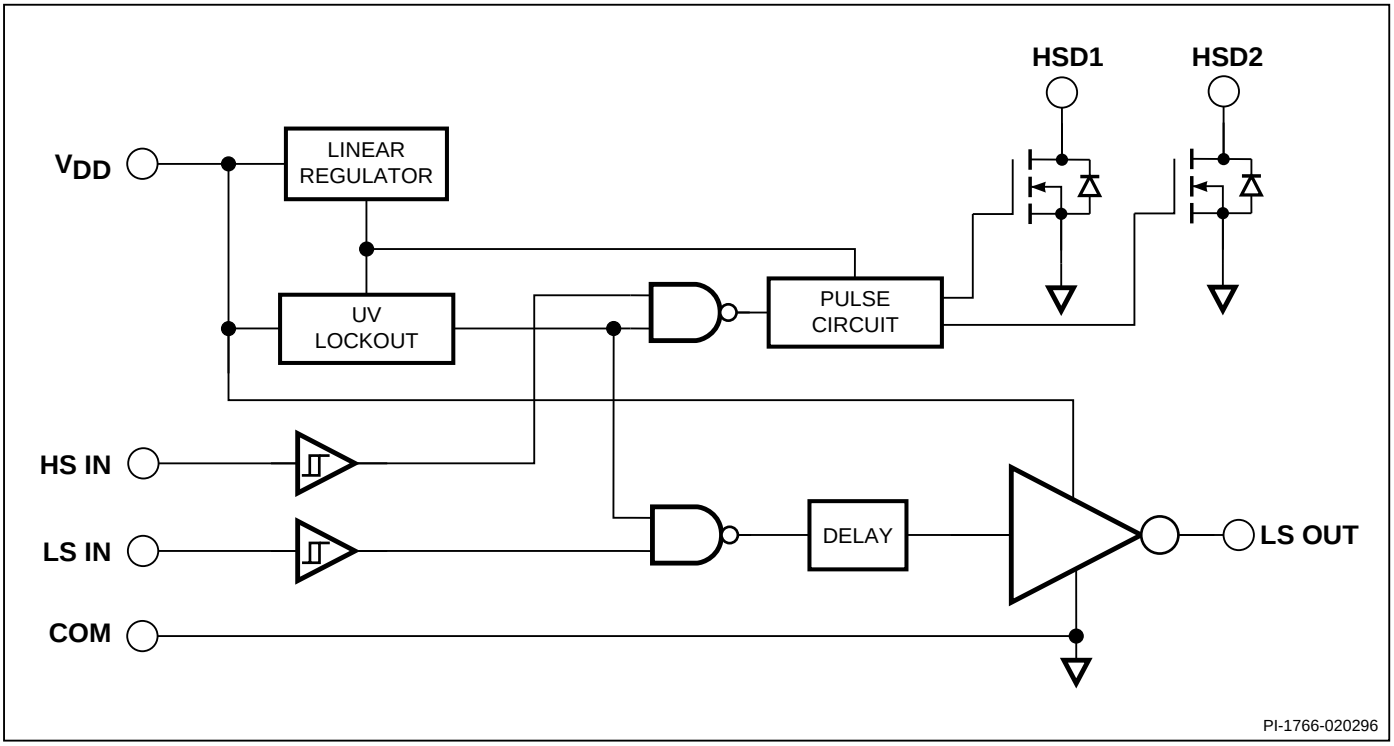


Figure 3. Functional Block Diagram of the INT202

INT202 Functional Description

5 V Regulator
The 5 V linear regulator circuit provides the supply voltage for the control logic and high-voltage level shift circuit. This allows the logic section to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

Undervoltage Lockout
The undervoltage lockout circuit disables the LS OUT pin and both HSD pins whenever the V_{DD} power supply falls below typically 9.0 V, and maintains this condition until the V_{DD} power supply rises above typically 9.35 V. This guarantees that both MOSFETs will remain off during power-up or fault conditions.

HSD1/HSD2
The HSD1 and HSD2 outputs are connected to integrated high-voltage N-channel MOSFET transistors which perform the level-shifting function for communication to the high-side driver. Controlled current capability allows the drain voltage to float with the high-side driver. Two individual channels produce a true differential communication channel for accurately controlling the high-side driver in the presence of fast moving high-voltage waveforms.

Pulse Circuit
The pulse circuit provides the two high-voltage level shifters with precise timing signals. Two pulses are sent over HSD1 to signal the high-side driver to turn on. One pulse is sent over HSD2 to signal the high-side driver to turn off. The combination of differential communication with the precise timing provides maximum immunity to noise.

Driver
The CMOS drive circuit provides drive power to the gate of the MOSFET used on the low side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving an external transistor gate at up to 15 V.

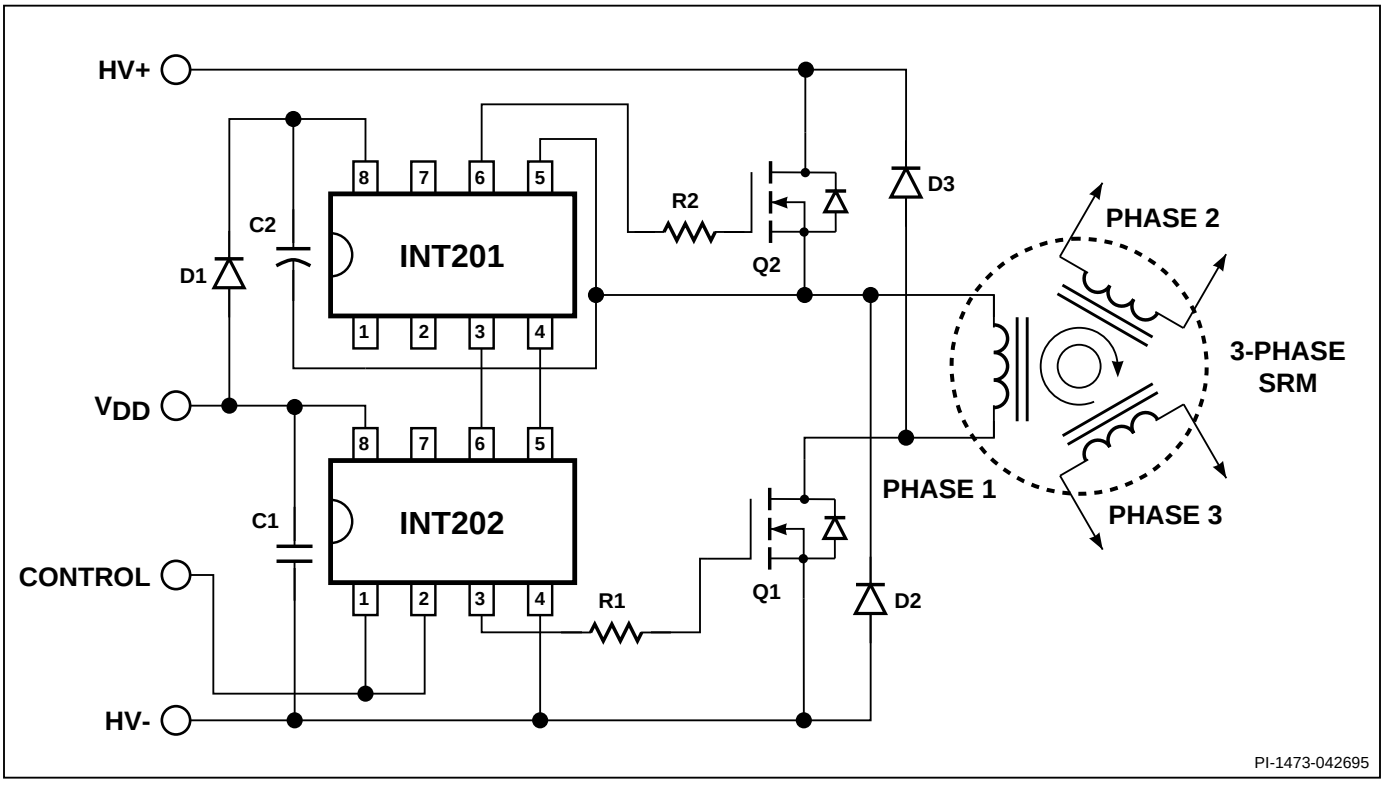


Figure 4. Using the INT202 and INT201 to Drive a Switched Reluctance Motor.

General Circuit Operation

The three-phase switched reluctance motor drive circuit shown in Figure 4 illustrates a typical application for the INT202/201. The LS IN signal directly controls MOSFET Q1. The $\overline{\text{HS IN}}$ signal causes the INT202 to command the INT201 to turn MOSFET Q2 on or off as required.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+. V_{DD} should be supplied from a low impedance voltage source.

The length of time that the high-side can remain on is limited by the size of the bootstrap capacitor. Applications with extremely long high-side on times require special techniques discussed in AN-10.

Maximum frequency of operation is limited by power dissipation due to high-voltage switching, gate charge, and bias power. Figure 5 indicates the maximum switching frequency as a function of input voltage and gate charge. For higher ambient temperatures, the switching frequency should be derated linearly.

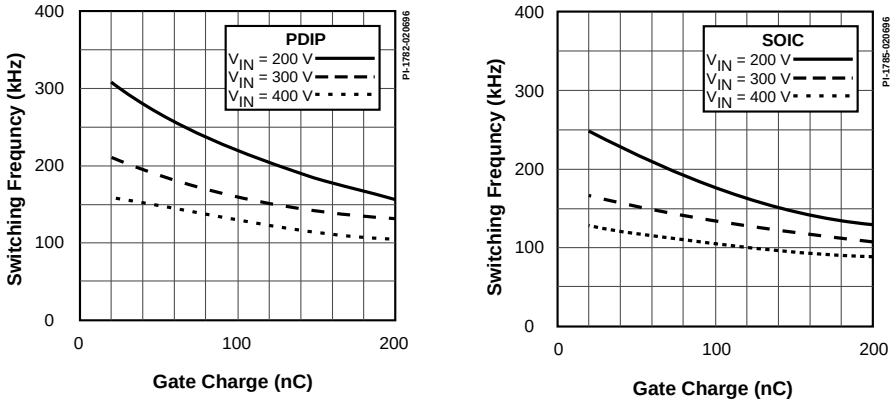


Figure 5. Switching Frequency versus Gate Charge for a) PDIP and b) SOIC.

ABSOLUTE MAXIMUM RATINGS[1]

HSD1/HSD2 Voltage (1 Suffix) ..... 600 V
(2 Suffix) ..... 800 V
HSD1/HSD2 Slew Rate ..... 10 V/ns
V_{DD} Voltage ..... 16.5 V
Logic Input Voltage ..... -0.3 V to 5.5 V
LS OUT Voltage ..... -0.3 V to V_{DD} + 0.3 V
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature ..... 150°C
Lead Temperature(2). ..... 260°C

Power Dissipation
PF Suffix (T_A = 25°C) ..... 1.25 W
(T_A = 70°C) ..... 800 mW
TF Suffix (T_A = 25°C) ..... 1.04 W
(T_A = 70°C) ..... 667 mW
Thermal Impedance (θ_{JA})
PF Suffix ..... 100°C/W
TF Suffix ..... 120°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 1/16" from case for 5 seconds.

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{DD} = 15 V, COM = 0V T_A = -40 to 85°C	Min	Typ	Max	Units
LOGIC						
Input Current, High or Low	I_{IH}, I_{IL}	V_{IH} = 4.0 V	0	10	150	µA
		V_{IL} = 1.0 V	-20	0	20	
Input Voltage High	V_{IH}		4.0			V
Input Voltage Low	V_{IL}				1.0	V
Input Voltage Hysteresis	V_{HY}		0.3	0.7		V
HSD OUTPUTS						
Breakdown Voltage	BV_{DSS}	1 Suffix	600	700		V
		2 Suffix	800	900		
Off-State Output Current	$I_{HSD(OFF)}$	V_{HSD1}, V_{HSD2} = 500 V		0.1	15	µA
On-State Output Current	$I_{HSD(ON)}$	V_{HSD1}, V_{HSD2} = 10 V	5	25		mA
On-State Pulse Width	$t_{HSD(ON)}$				156	ns
Output Capacitance	C_{OSS}	V_{HSD1}, V_{HSD2} = 25 V		10		pF

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{DD}= 15 V, COM = 0V T_A = -40 to 85°C		Min	Typ	Max	Units
LS OUT							
Output Voltage High	V_{OH}	I_o= -20 mA		V_{DD}-1.0	V_{DD}-0.5		V
Output Voltage Low	V_{OL}	I_o= 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_o= 0V			-150	mA
			V_o= V_{DD}	300			
Turn-on Delay Time	$t_{d(on)}$	See Figure 6			0.6	1.0	µs
Rise Time	t_r	See Figure 6			80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 6			0.5	1	µs
Fall Time	t_f	See Figure 6			50	100	ns
SYSTEM RESPONSE							
Matching (Low On to High On)	Mt_{P+}	See Figure 7			0.3	1	µs
Matching (Low Off to High Off)	Mt_{P-}	See Figure 7			0.3	1	µs
UNDERVOLTAGE LOCKOUT							
Input UV Trip-off Voltage	$V_{DD(UV)}$			8.5	9.0	10	V
Input UV Hysteresis				175	350		mV
SUPPLY							
Supply Current	I_{DD}	See Note 2			1.5	3.0	mA
Supply Voltage	V_{DD}			10		16	V

NOTES:

1. Applying a short circuit to the LS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.
2. V_{DD} supply must have less than 30 Ω output impedance.

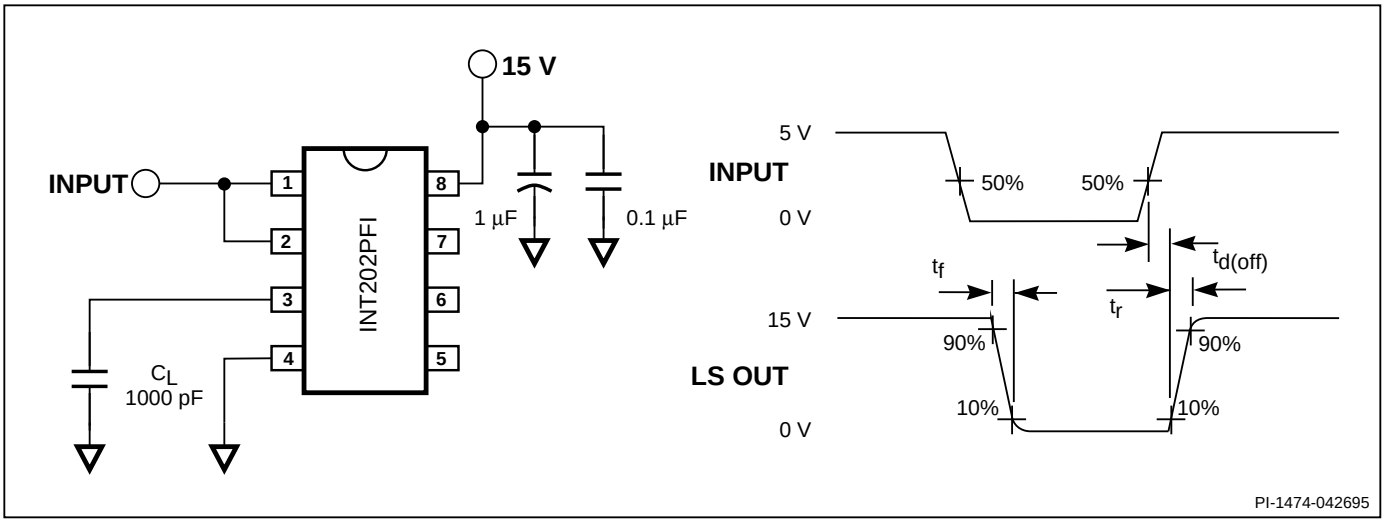


Figure 6. Switching Time Test Circuit.

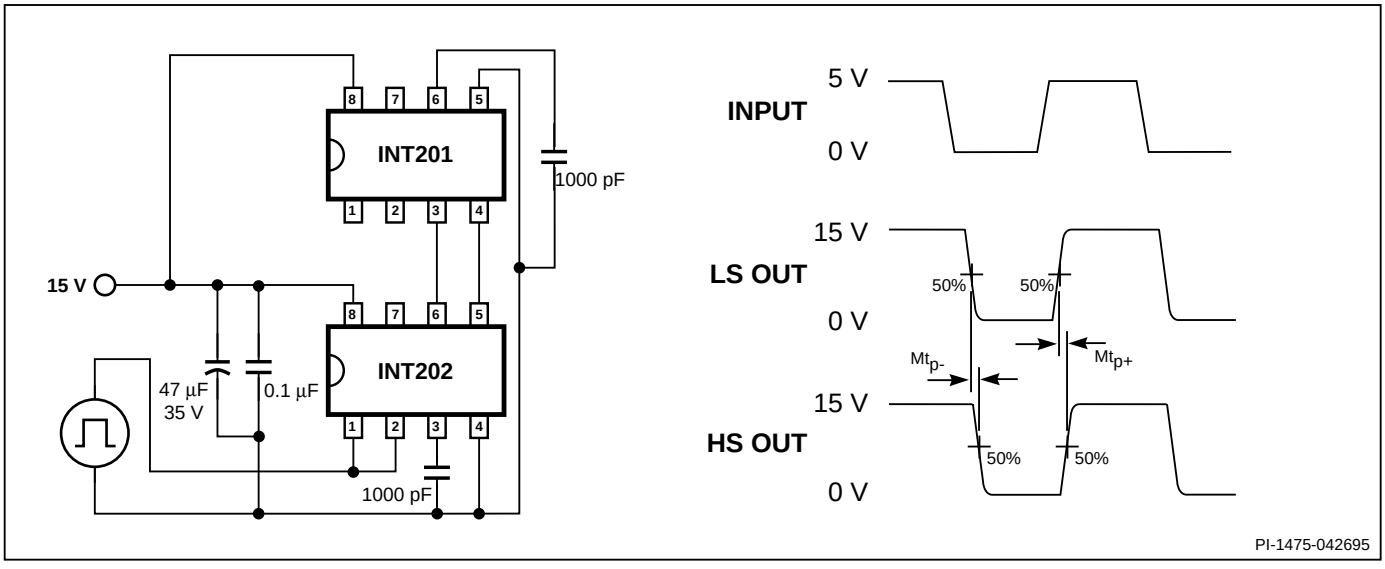
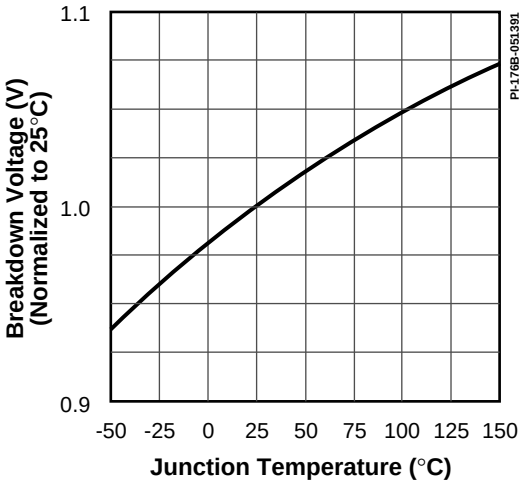
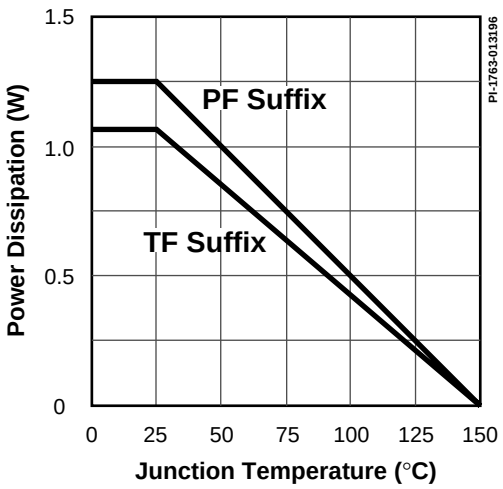


Figure 7. Matching Test Circuit.

BREAKDOWN vs. TEMPERATURE

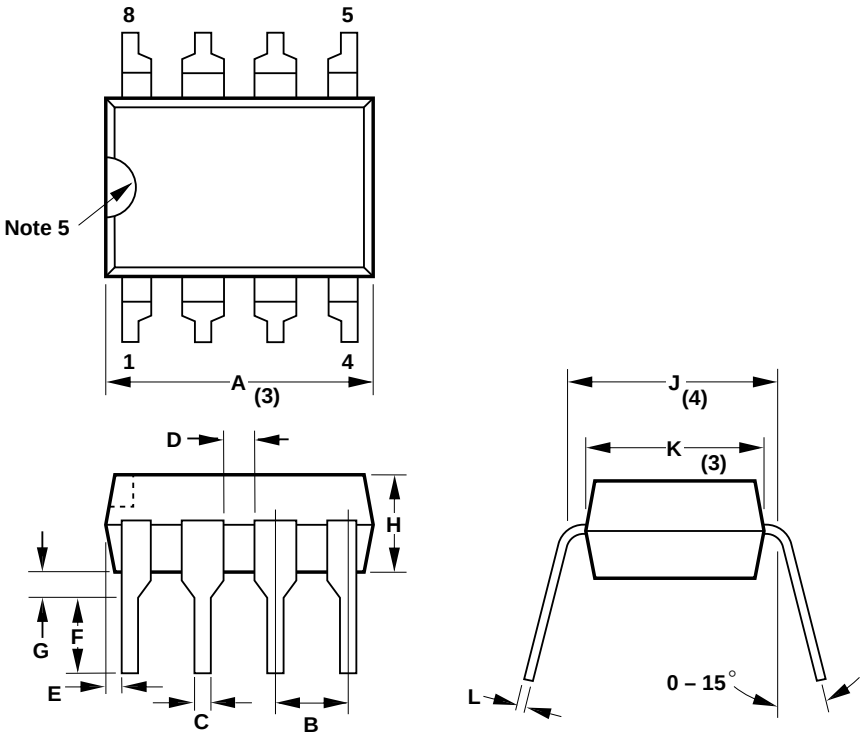


PACKAGE POWER DERATING



P08A — Plastic DIP-8

Dim.	inches	mm
A	.395 MAX	10.03 MAX
B	.090-.110	2.29-2.79
C	.015-.021	0.38-0.53
D	.040 TYP	1.02 TYP
E	.015-.030	0.38-0.76
F	.125 MIN	3.18 MIN
G	.015 MIN	0.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	0.23-0.38

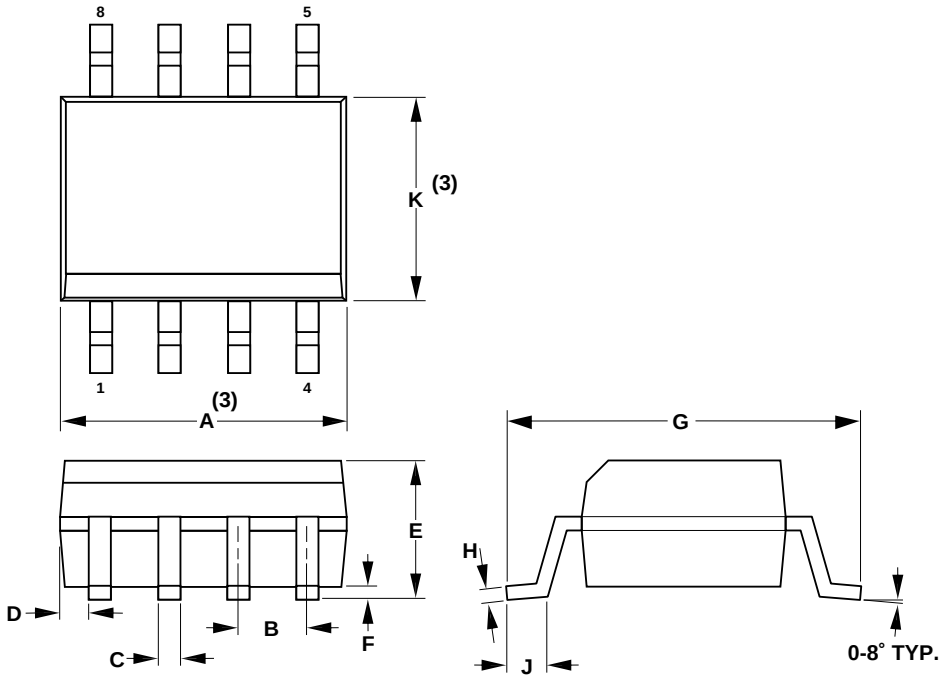


Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions: inches.
3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

PI-1842-050196

T08A — Plastic SO-8

DIM	inches	mm
A	0.189-0.197	4.80-5.00
B	0.050 TYP	1.27 TYP
C	0.014-0.019	0.35-0.49
D	0.012 TYP	0.31 TYP
E	0.053-0.069	1.35-1.75
F	0.004-0.010	0.10-0.25
G	0.228-0.244	5.80-6.20
H	0.007-0.010	0.19-0.25
J	0.021-0.045	0.51-1.14
K	0.150-0.157	3.80-4.00



Notes:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75 mm (.150 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified edge by chamfer on top of the package body or indent on Pin 1 end.

PI-1845-050196

Notes

Notes

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