M5M51016BTP,RT-10VL-I, -10VLL-I

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51016BTP, RT are a 1048576-bit CMOS static RAM organized as 65536 word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016BTP,RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51016BTP(normal lead bend type package), M5M51016BRT (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

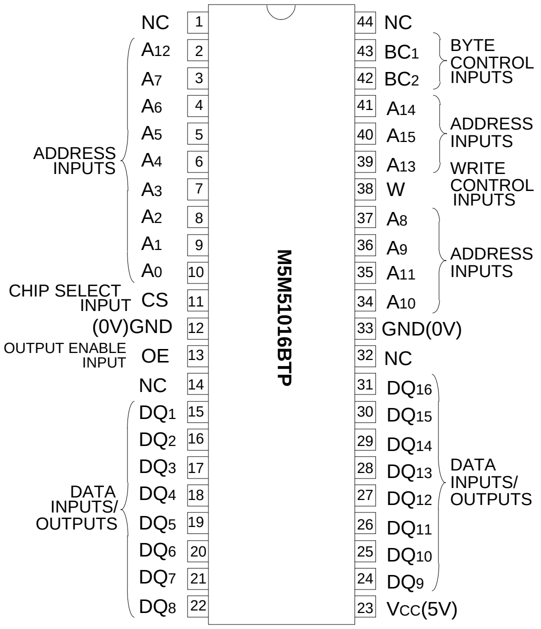
Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M51016BTP,RT-10VL	100ns	12mA (1MHz)	120µA (V_{CC} = 3.6V)
M5M51016BTP,RT-10VLL	100ns		24µA (V_{CC} = 3.6V) 0.3µA (V_{CC} = 3.0V, typ)

- ● Single +3.3V power supply
- ● Low stand-by current 0.3µA (typ.)
- ● Directly TTL compatible : All inputs and outputs
- ● Easy memory expansion and power down by CS, $\overline{BC_1}$ & $\overline{BC_2}$
- ● Data hold on +2V power supply
- ● Three-state outputs : OR-tie capability
- ● $\overline{OE}$ prevents data contention in the I/O bus
- ● Common data I/O
- ● Package
  - M5M51016BTP,RT ······························ 44pin 400mil TSOP(II)

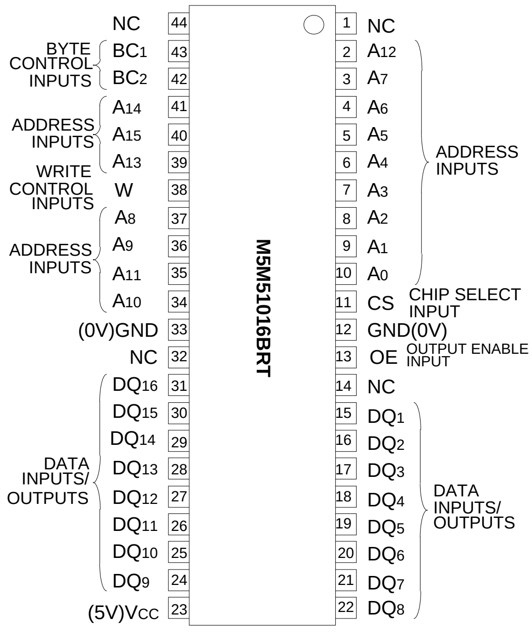
APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W - H (400mil TSOP Normal Bend)



Outline 44P3W - J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51016B series are determined by a combination of the device control inputs $\overline{\mathrm{BC}}_1$, $\overline{\mathrm{BC}}_2$, CS, $\overline{\mathrm{W}}$ and $\overline{\mathrm{OE}}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level W overlaps with the low level $\overline{\mathrm{BC}}_1$ and/or $\overline{\mathrm{BC}}_2$ and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{\mathrm{W}}$, $\overline{\mathrm{BC}}_1$, $\overline{\mathrm{BC}}_2$ or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{\mathrm{OE}}$ directly controls the output stage. Setting the $\overline{\mathrm{OE}}$ at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{\mathrm{W}}$ at a high level and $\overline{\mathrm{OE}}$ at a low level while $\overline{\mathrm{BC}}_1$ and/or $\overline{\mathrm{BC}}_2$ and CS are in an active state. ($\overline{\mathrm{BC}}_1$ and/or $\overline{\mathrm{BC}}_2$=L,CS=H)

When setting $\overline{\mathrm{BC}}_1$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode.And when setting $\overline{\mathrm{BC}}_2$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper -Byte are in a non-selectable mode.

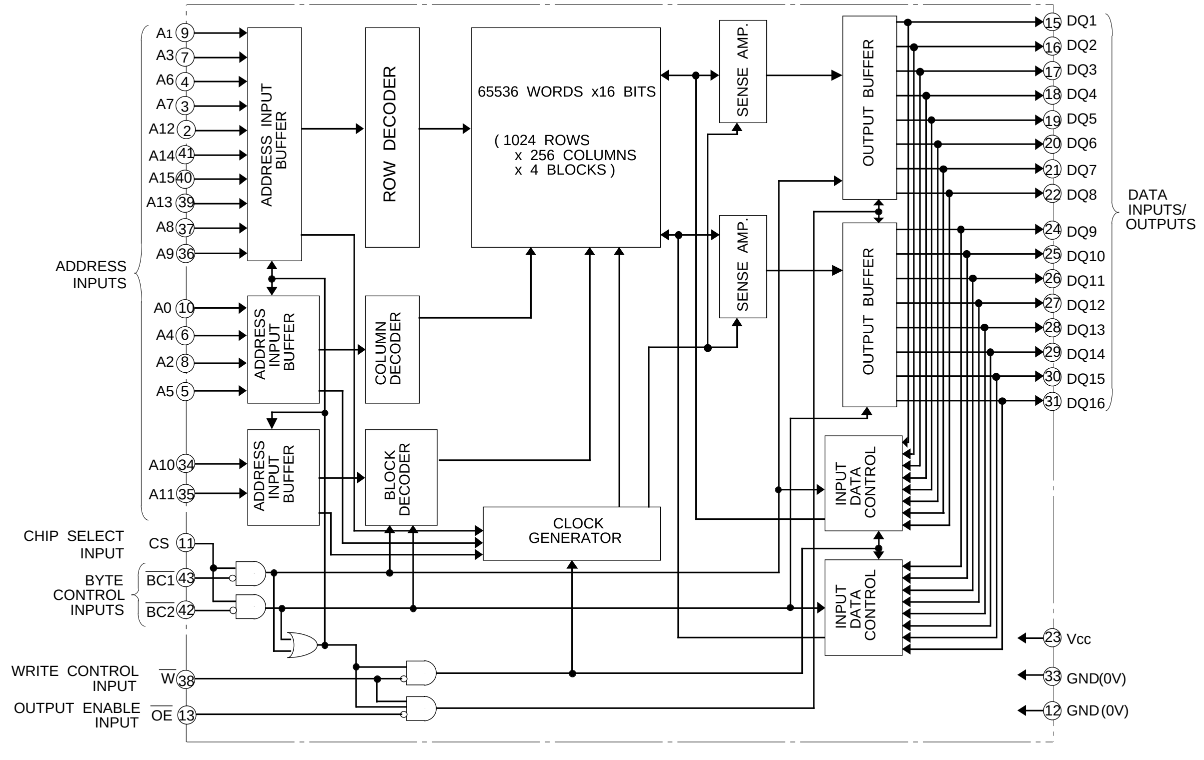
When setting $\overline{\mathrm{BC}}_1$ and $\overline{\mathrm{BC}}_2$ at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{\mathrm{BC}}_1$, $\overline{\mathrm{BC}}_2$ and CS. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during powerfailure or power-down operation in the non-selected mode.

CS	$\overline{\mathrm{BC}}_1$	$\overline{\mathrm{BC}}_2$	$\overline{\mathrm{W}}$	$\overline{\mathrm{OE}}$	Mode	$DQ_{1\sim8}$	$DQ_{9\sim16}$	I_{CC}
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	Upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	Upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	————	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	————	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	————	High-Z	High-Z	Active

(High-Z=High-impedance)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	– 0.3 ~ 4.6	V
V_I	Input voltage		– 0.3* ~ Vcc + 0.3	V
V_O	Output voltage		0 ~ Vcc	V
P_d	Power dissipation	Ta=25 °C	1	W
T_{opr}	Operating temperature		– 40 ~ 85	°C
T_{stg}	Storage temperature		– 65 ~ 150	°C

* –3.0V in case of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta= -40 ~85 °C, Vcc=3.3V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage			– 0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = – 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = – 0.1mA		Vcc–0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I =0 ~ Vcc				±1	µA
I_O	Output current in off-state	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IH} or CS = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 ~ Vcc				±1	µA
I_{CC1W}	Word operation (16bit) Active supply current (AC,TTL level)	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IL}, CS = V_{IH} other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle			50	mA
I_{CC2W}			1MHz			12	mA
I_{CC1B}	Byte operation (8bit) Active supply current (AC,TTL level)	($\overline{BC}_1$ = V_{IH} and $\overline{BC}_2$ = V_{IL}) or ($\overline{BC}_1$ = V_{IL} and $\overline{BC}_2$ = V_{IH}), CS = V_{IH} other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle			30	mA
I_{CC2B}			1MHz			10	mA
I_{CC3}	Stand-by current	1) CS ≦ 0.2V, other inputs = 0~Vcc 2) $\overline{BC}_1$,$\overline{BC}_2$ ≧ Vcc - 0.2V, CS ≧ Vcc - 0.2V other inputs = 0~Vcc	-VL			120	µA
			-VLL			24	µA
I_{CC4}	Stand-by current	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IH} or CS = V_{IL}, other inputs = 0~Vcc				1	mA

* –3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta= -40 ~ 85°C , Vcc=3.3V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance (except $\overline{BC}_1$,$\overline{BC}_2$)	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_{IBC}	Input capacitance ($\overline{BC}_1$,$\overline{BC}_2$)	V_I=GND, V_I=25mVrms, f=1MHz			9	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 3.3V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~ 85°C , V_{CC} = 3.3V ± 0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ······················ V_{IH} = 2.2V, V_{IL} = 0.4V
Input rise and fall time ·············· 5ns
Reference level ························ V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads ···························· Fig.1,C_L = 30pF
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

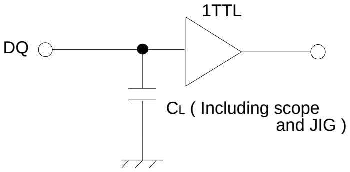


Fig.1 Output load

(2) READ CYCLE

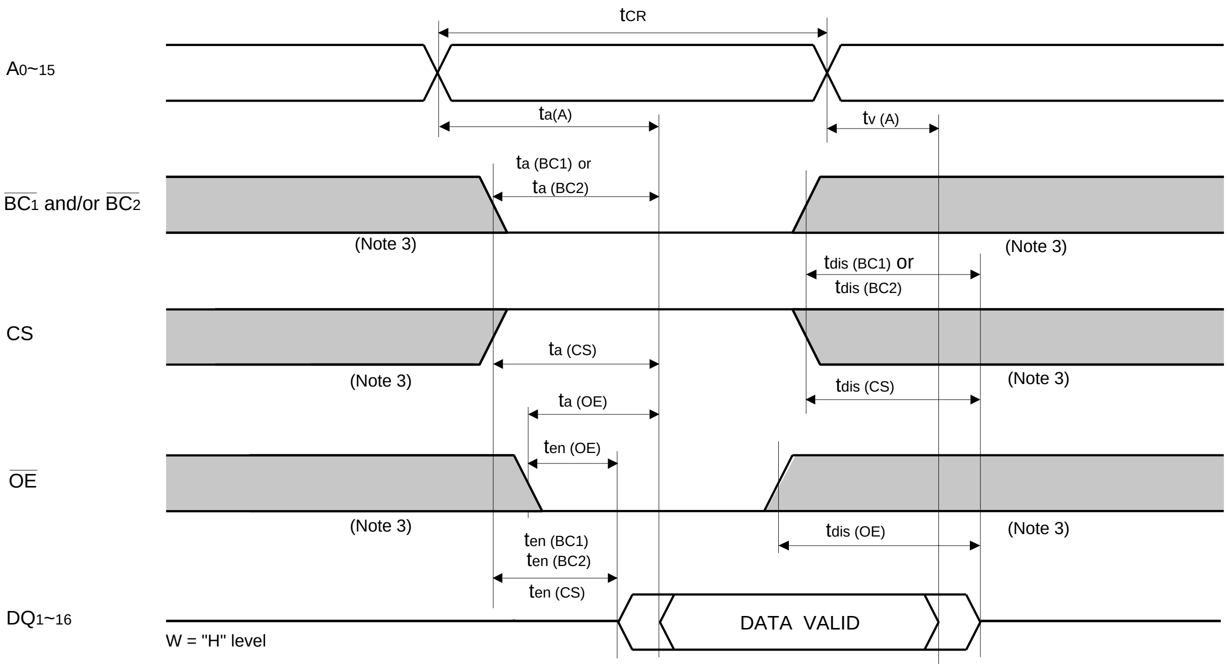
Symbol	Parameter	Limits M5M51016B -10VL,-10VLL Min	 Typ	 Max	Unit
t_{CR}	Read cycle time	100			ns
$t_{a(A)}$	Address access time			100	ns
$t_{a(BC1)}$	Byte control 1 access time			100	ns
$t_{a(BC2)}$	Byte control 2 access time			100	ns
$t_{a(CS)}$	Chip select access time			100	ns
$t_{a(OE)}$	Output enable access time			50	ns
$t_{dis(BC1)}$	Output disable time after $\overline{BC_1}$ high			35	ns
$t_{dis(BC2)}$	Output disable time after $\overline{BC_2}$ high			35	ns
$t_{dis(CS)}$	Output disable time after CS low			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35	ns
$t_{en(BC1)}$	Output enable time after $\overline{BC_1}$ low	10			ns
$t_{en(BC2)}$	Output enable time after $\overline{BC_2}$ low	10			ns
$t_{en(CS)}$	Output enable time after CS high	10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			ns
$t_{v(A)}$	Data valid time after address	10			ns

(3) WRITE CYCLE

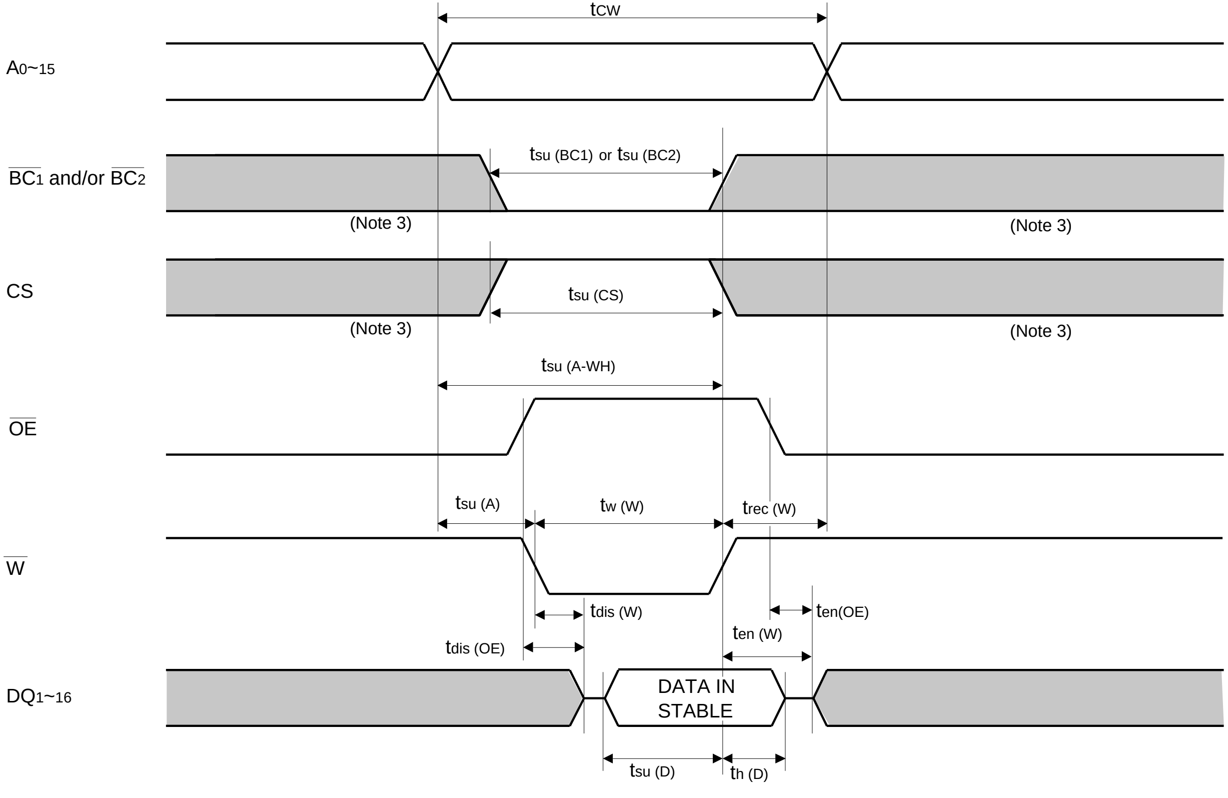
Symbol	Parameter	Limits M5M51016B -10VL,-10VLL Min	 Typ	 Max	Unit
t_{CW}	Write cycle time	100			ns
$t_{w(W)}$	Write pulse width	75			ns
$t_{su(A)}$	Address set up time	0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	85			ns
$t_{su(BC1)}$	Byte control 1 setup time	85			ns
$t_{su(BC2)}$	Byte control 2 setup time	85			ns
$t_{su(CS)}$	Chip select set up time	85			ns
$t_{su(D)}$	Data set up time	40			ns
$t_{h(D)}$	Data hold time	0			ns
$t_{rec(W)}$	Write recovery time	0			ns
$t_{dis(W)}$	Output disable time from W low			35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high			35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			ns

(4) TIMING DIAGRAMS

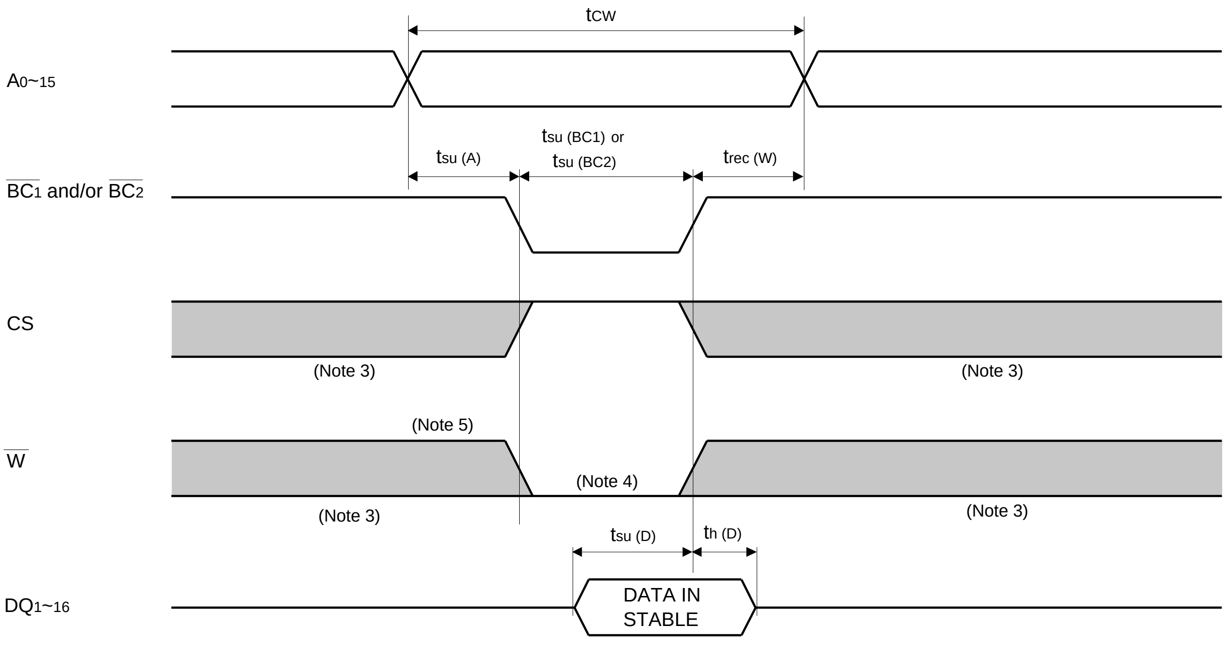
Read cycle



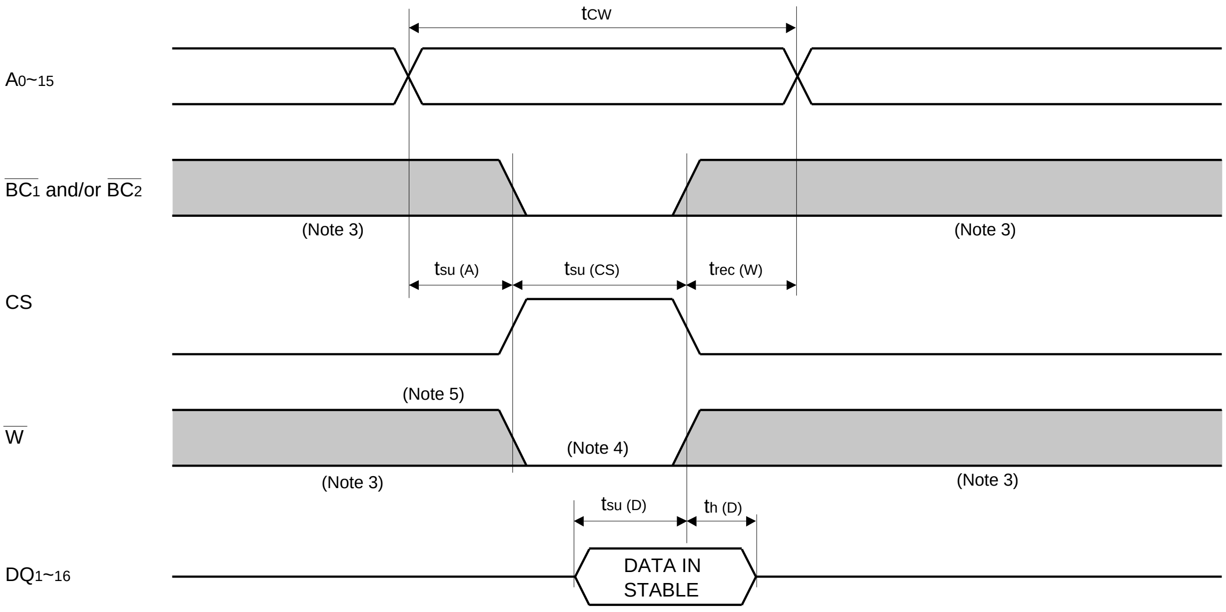
Write cycle (W control mode)



Write cycle ($\overline{\text{BC}}$ control mode)



Write cycle (CS control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while CS high overlaps $\overline{BC_1}$ and/or $\overline{BC_2}$ low and $\overline{W}$ low.
5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC_1}$ and/or $\overline{BC_2}$ or rising edge of CS, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = -40 ~ 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (BC)}$	Byte control input $\overline{BC}_1$ & $\overline{BC}_2$			2.0			V
$V_{I\ (CS)}$	Chip select input CS	3.0V ≦ $V_{CC(PD)}$				0.6	V
		$V_{CC(PD)}$ < 3.0V				0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1) CS ≦ 0.2V other inputs = 0 ~ 3V 2) BC_1 & BC_2 ≧ V_{CC} − 0.2V, CS ≧ V_{CC} − 0.2V,other inputs=0~3V	-VL			100	µA
			-VLL		0.3	20 (Note 7)	

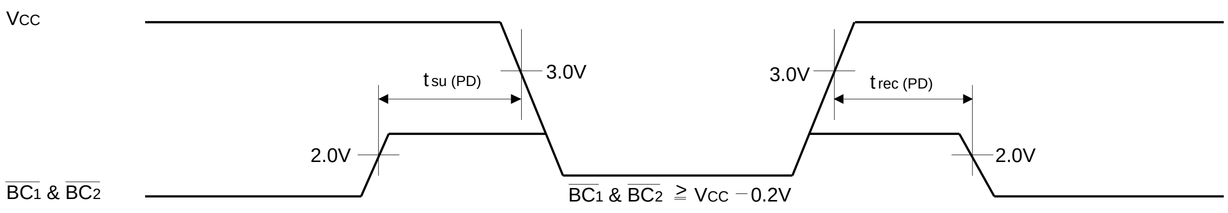
Note7. $I_{CC\ (PD)}$ = 1µA in case of Ta = 25°C

(2) TIMING REQUIREMENTS (Ta = -40 ~ 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{BC}$ control mode



CS control mode