MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

100/80MHz Video Processor

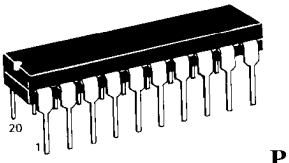
The MC13281FY / MC13280FY is a three channels wideband amplifiers designed for use as a video pre-amplifier in high resolution RGB color monitor.

Features :
- 4Vp-p Output with 100/80MHz Bandwidth
- 3.5ns Rise/Fall Time for MC13281FY
- 4.3ns Rise/Fall Time for MC13280FY
- Subcontrast Control
- Contrast Control
- Package: NDIP 20

MC13281FY
MC13280FY

100/80MHz Video Processor

Silicon Monolithic Integrated Circuit



P SUFFIX
PLASTIC PACKAGE
CASE 738

DEVICE	TEMPERATURE RANGE	PACKAGE
MC13281FYP	0 TO +70 °C	Plastic DIP
MC13280FYP	0 TO +70 °C	Plastic DIP

PIN ASSIGNMENT (TOP VIEW)

R Channel Subcontrast	1		20	Blank
R Channel I/P	2		19	Clamp
G Channel Subcontrast	3		18	R Channel Emitter O/P
G Channel I/P	4		17	R Channel Clamp Cap
B Channel Subcontrast	5	NDIP20	16	V5
B Channel I/P	6		15	G Channel Emitter O/P
GND	7		14	G Channel Clamp Cap
Vcc	8		13	Video Vcc
Contrast	9		12	B Channel Clamp Cap
NC	10		11	B Channel Emitter O/P

ABSOLUTE MAXIMUM RATING

Table 1

Parameter	Pin	Value	Unit
Power Supply Voltage	8	-0.5,10	Vdc
	13	-0.5,10	Vdc
Voltage at Video Amplifier Inputs	2,4,6	-0.5,+5.0	Vdc
Voltage at Video Amplifier Output Collectors	13	-0.5,10	Vdc
Collector-Emitter Current (Three Channels)	13	120	mA
Storage Temperature		-65 to +150	˚C
Junction Temperature		150	˚C
Operating Temperature		0 to +70	˚C

Device should not be operated at these limits. Refer to "Recommended Operating Conditions" section for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Table 2

Parameter	Pin	Min	Typ	Max	Unit
Power Supply Voltage	8,13	7.6	8	8.4	Vdc
Power Supply Current	8,13		70		mA
Contrast Control	9	0		5	Vdc
Sub-Contrast Control	1,3,5	0		5	Vdc
Blanking Input Threshold	20		1.25		V
Clamping Input Threshold	19		3.75		V
Video Signal Amplitude	2,4,6		0.7		Vpp
Collector-Emitter Current (Three Channels)	13	0		50	mA
Operating Ambient Temperature		0	25	70	˚C

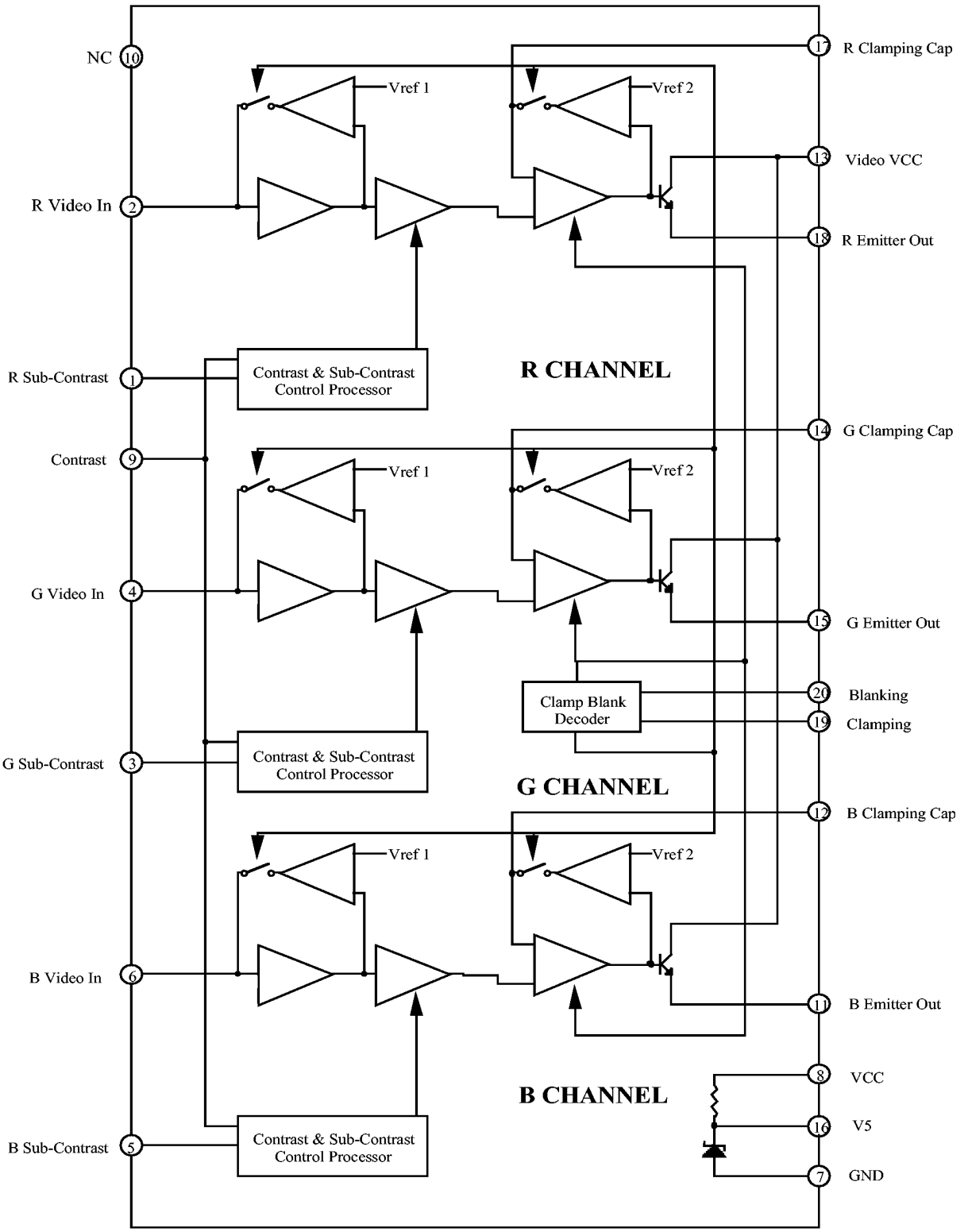
ELECTRICAL CHARACTERISTICS (Refer to test circuit figure 1, TA=25˚C, Vcc=8.0Vdc)

Table 3

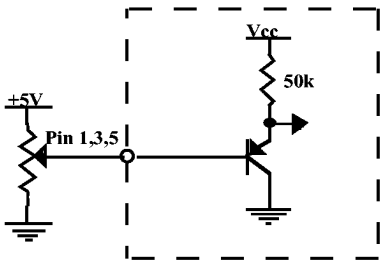
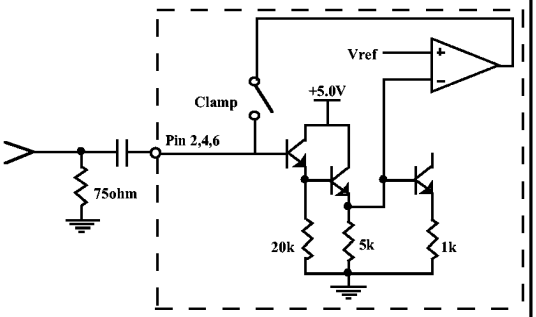
Parameter	Condition	Pin	Min	Typ	Max	Unit
Input Impedance		2,4,6	100			KΩ
Internal DC Bias Voltage				2.7		Vdc
Input Signal Amplitude	with 75 Ω resistor termination at input	2,4,6		0.7	1.0	Vpp
Output Signal Amplitude	V2,V4,V6 = 0.7Vpp V1,V3,V5,V9 = 5V	11,15,18	3.6	4		Vpp
Voltage Gain	V10 = 0V			5.6		V/V
Contrast Control	V9 = 5 to 0V V1,V3,V5 = 5V	9		-26		dB
Sub-contrast Control	V1,V3,V5 = 5 to 0V V9=5V	1,3,5		-26		dB
Emitter DC Level		11,15,18	1.0	1.2	1.4	Vdc
Clamping Pulse Width		19	500			nS
Blanking Input Threshold		20		1.25		V
Clamping Input Threshold		19		3.75		V
	V2,V4,V6 = 0.7Vpp	11,15,18				
Video Rise Time	Vout = 4Vpp	MC13281FY		3.5		
	RL > 300Ω, CL < 5pF	MC13280FY		4.3		nS
Video Fall Time		MC13281FY		3.5		
		MC13280FY		4.3		
Video Bandwidth	V2,V4,V6 = 0.7Vpp	11,15,18				
	V1,V3,V5,V9 = 5V	MC13281FY		100		MHz
	V10 = 0V	MC13280FY		80		
	RL > 300Ω, CL < 5pF					

It is recommended to use double sided PCB layout for high frequency measurement. (eg. rise/fall time, bandwidth.)

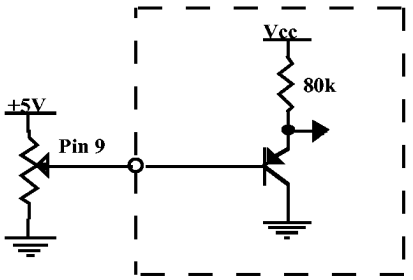
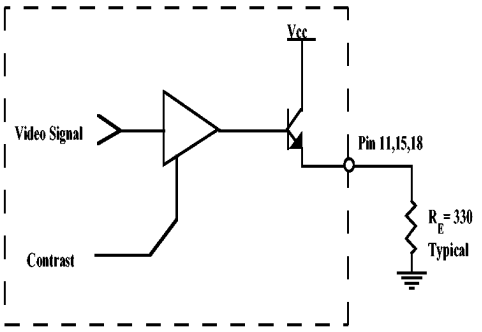
INTERNAL BLOCK DIAGRAM



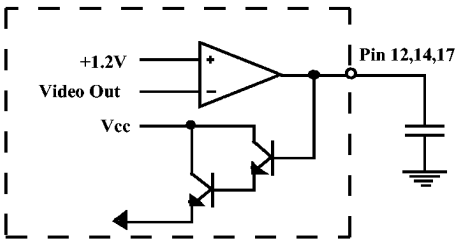
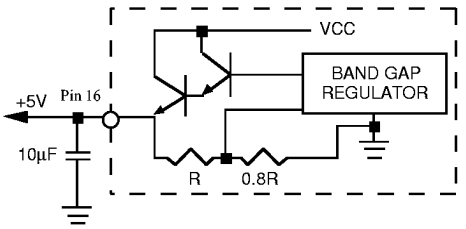
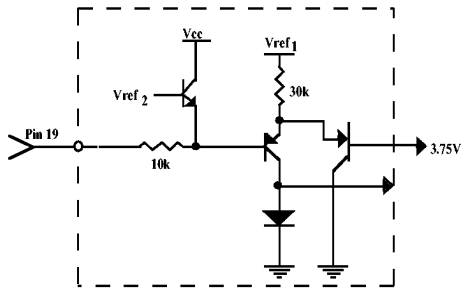
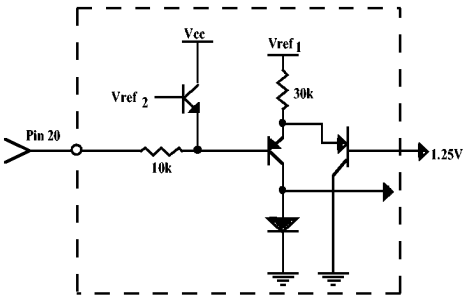
PIN OUT DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
1 3 5	R Subcontrast Control G Subcontrast Control B Subcontrast Control		These pins provides a max. of 26dB attentuation to vary the gain of each video amplifier separately. Input voltage from 0 to 5V. Increase the voltage will increase contrast level.
2 4 6	R Input G Input B Input		The input coupling capacitor is used for input clamping storage. The maximum source impedance is 100 Ω. Input polarity of the video signal is positive. Norminal 0.7Vpp input signal is recommended. (max. 1Vpp)
7	Video Ground		Ground for the video section (video amplifiers, RGB channels and overall contrast/subcontrast controls and video reference voltage)
8	Vcc		Connect to +8V dc supply. Decoupling is required at this pin.

PIN OUT DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
9	Contrast		Overall Contrast Control. The input range is from 0V to 5V. An increase of voltage increases contrast.
10	NC		This pin should be connected to ground.
11 15 18	B Emitter Output G Emitter Output R Emitter Output		The video outputs are configured as emitter-followers with driving capability of about 15mA. The DC voltage at these three emitters is set to 1.2V (Black level). The DC current through the output stage is determined by the emitter resistors (typically 330Ω).

PIN OUT DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
12 14 17	B Clamp Capacitor G Clamp Capacitor R Clamp Capacitor		Normally a 100nF capacitor is connected to these pins. The capacitor is used for video outputs DC restoration.
13	Video VCC		Connect to +8V dc supply. This VCC is for video output stage. It is internally connected to collectors of the ouput transistors.
16	5Vref		+5 volt regulator. Minimum 10µF capacitor is required for noise filtering and compensation. It can source up to 20mA but not sink current. Output impedance is ≈ 10Ω. Recommend for voltage reference only.
19	Clamp		This pin is used for video clamping. The threshold clamping level is 3.75V
20	Blank		This pin is used for video blanking. The threshold blanking level is 1.25V

FUNCTIONAL DESCRIPTION

The MC13281FY / MC13280FY composes of three video amplifiers, clamping & blanking circuitries with contrast & sub-contrast controls. Each video amplifier is designed to have a -3dB bandwidth of 100/80MHz with a gain of up to about 5.6V/V or 15dB.

Video Input

Video input stages are high impedance and designed to accept a maximum signal of 1Vp-p with 75Ω termination (typically) provided externally. During the clamping period, a current is provided to the input capacitor by the clamping circuit which brings the input to a proper DC level (nominal 2.7 volts). The blanking and clamping signals are to be provided externally with threshold sitting at 1.25V and 3.75V respectively.

Video Output

Video output stages are configured as emitter-follower with driving capability of about 15mA for each channel. The DC voltage at these three emitters are set to 1.2 volts (black level). The DC current through each output stage is determined by the emitter resistor (typically 330Ω).

Contrast Control

The contrast control varies the gain of three video amplifiers from a minimum of 0.3 V/V to a maximum of 5.6V/V when all sub-contrast levels set to 5 volts.

Sub-Contrast Control

Each sub-contrast control provides a maximum of 26dB attenuation on each video amplifier separately.

FUNCTIONAL DESCRIPTION

Clamp Pulse Input

The clamping pulse should be provided externally and the pulse width should be no less than 500ns.

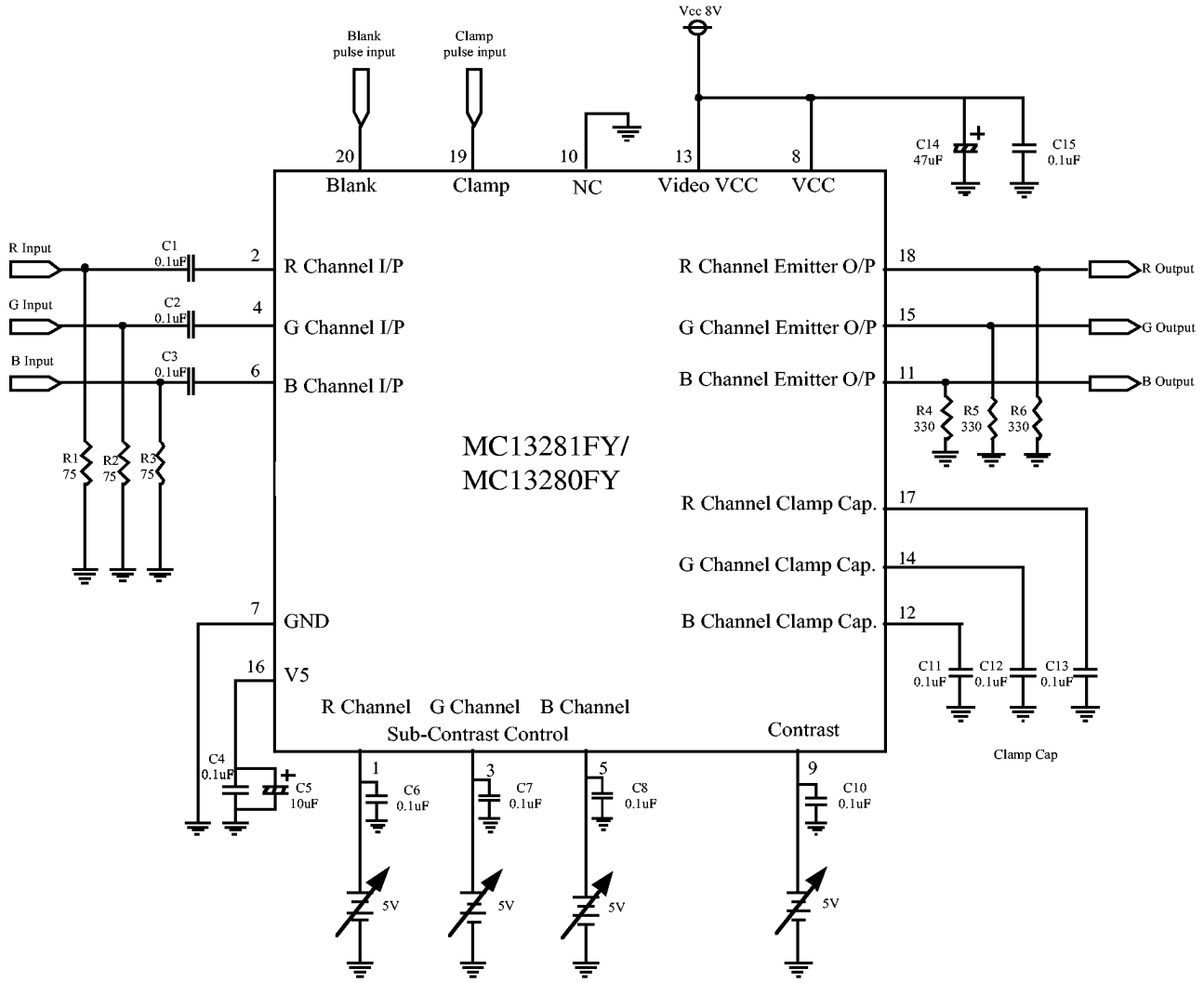
Blank Pulse Input

The blanking pulse is used to blank the video signal during the horizontal sync period or used as a control pin for video mute function.

Power Supplies

Vcc and Video Vcc supplies are to be 8 volts +/-5%

Figure 1: Test Circuit of MC13281FY / MC13280FY



APPLICATION INFORMATION

PCB Layout

Care should be taken in the PCB layout to minimize the noise effect. The most sensitive pins are Vcc(8), Video Vcc (13), V5(16), Clamp Cap (12,14,17). It is prefer to make a ground plane and connect Vcc/Video Vcc & ground trace to power supply directly. Separate decoupling capacitors should be used for Vcc and video Vcc and connected as close as possible to the device. Multi-layer ceramic & tantalum capacitors are recommended for optimum performance. Pin 16 V5 is designed as a +5V voltage reference for contrast, RGB subcontrast control, so same precaution for Vcc should be also applied at this pin. It is necessary to put the ground connection of three clamp capacitors close to IC ground pin.

The copper trace of video signal input and output should be as short as possible and separated by ground trace to avoid any RGB cross-interference. A single side PCB layout is shown in Figure 9 for reference. A double sided PCB should be used to optimize device's performance.

RGB Input & Output

The RGB output stages are designed as emitter-followers to drive the CRT driver circuitry directly. The emitter resistor used is 330Ω typically and the driving current is 15mA for each channel. The loading impedance connected to output stages should be greater than 330Ω & less than 5pF for optimum performance. (rise/fall time, bandwidth) Typical value for the loading capacitance is 3-5pF. Figure 2 show a typical CRT driver interface.

Each RGB input video signal with is normally terminated by a 75Ω resistor for impedance matching and is ac coupled to the video input. For high resolution color monitor application, it is recommended to use coaxial cable or shielded cable for input signal connection.

APPLICATION INFORMATION

Clamp & Blank Input

The clamping input is normally (except Sync on Green) direct connected to a positive horizontal sync pulse with threshold level of 3.75V. It is used as a timing reference for the DC restoration process, so it should not be open circuit. If Sync on Green timing mode is used, the clamping pulse should be located at horizontal back porch period instead of horizontal sync tip period. Otherwise, the black level will be clamped at a wrong DC level.

The blanking input is used as a video mute or horizontal blanking control pin and is connected to a blanking pulse generated from flyback or MCU with threshold level of 1.25V. The blanking pulse width should be equal to the flyback retrace period to make sure that the video signal is blanked properly during retrace period. It is necessary to limit the amplitude and avoid any negative value occur if flyback pulse is used. The blanking input pin cannot accept a negative voltage input. This pin should be grounded if it is not using the blanking function.

Figure 2: Interfacing with Video Output Driver

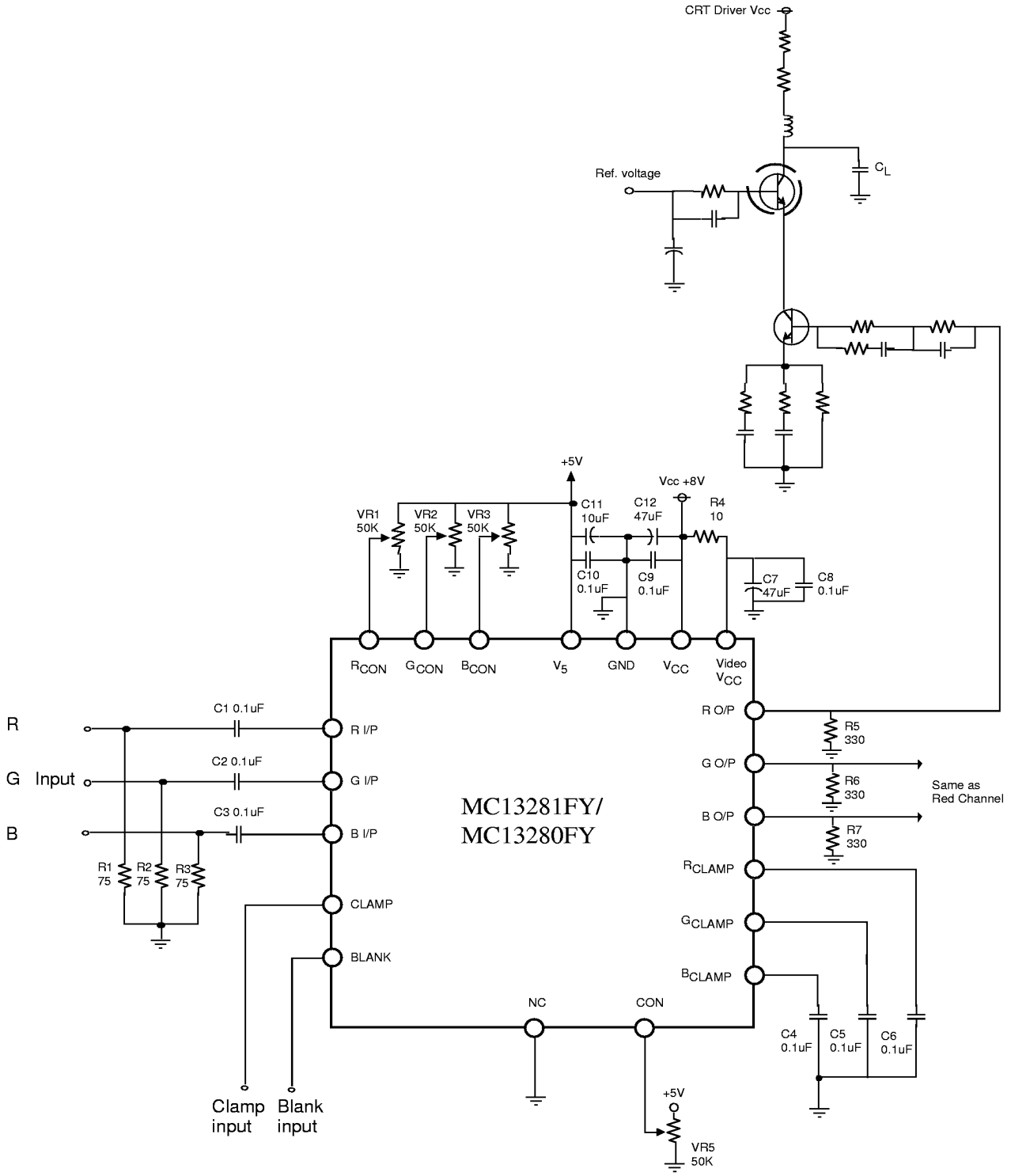


Figure 3: RGB In/Out Linearity

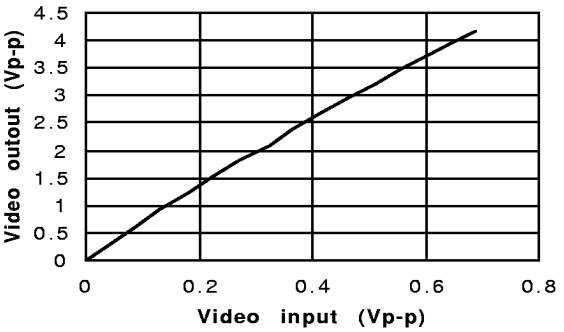


Figure 4: Contrast Control

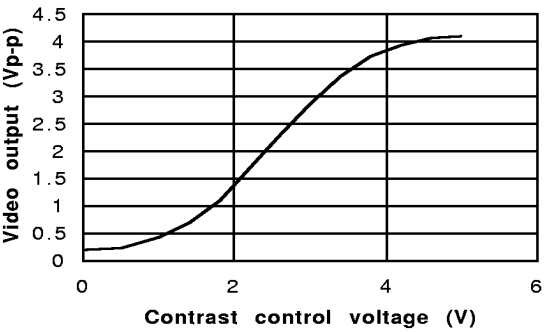


Figure 5: Sub-Contrast Control

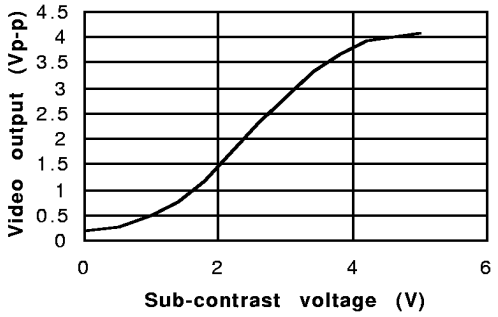


Figure 6: Crosstalk from Green to Red & Blue Channels

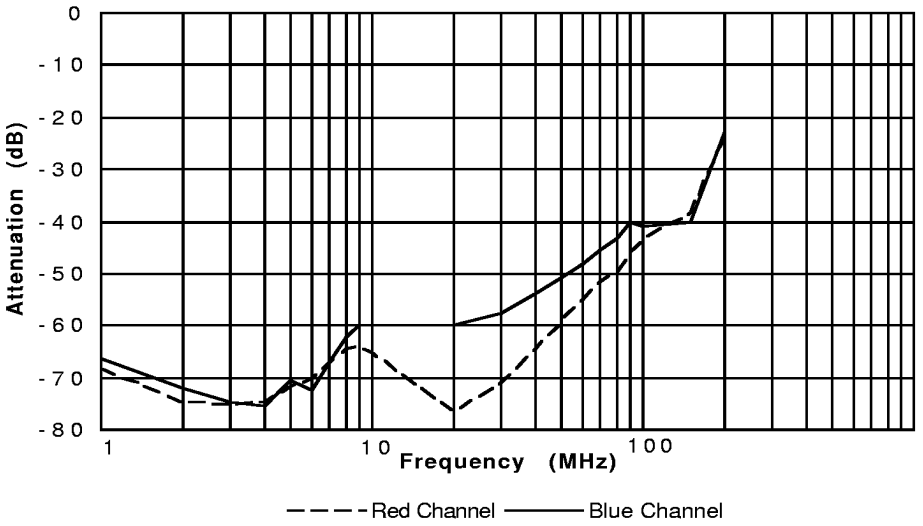
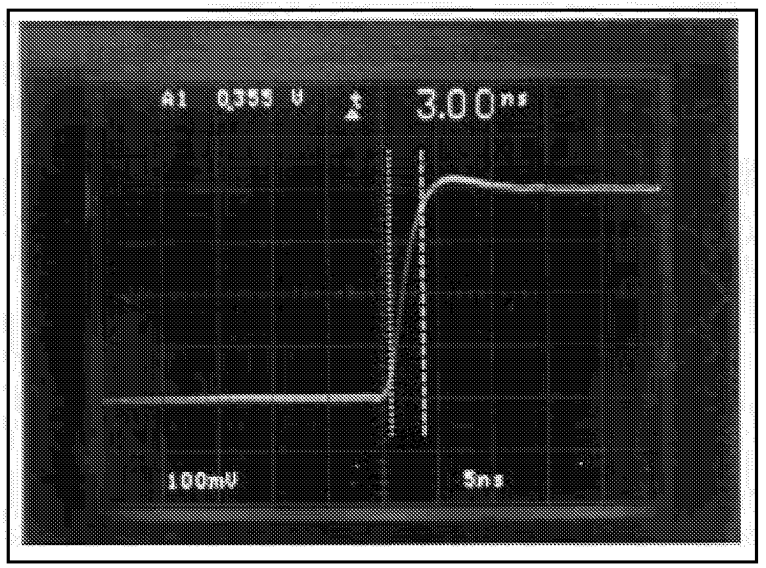
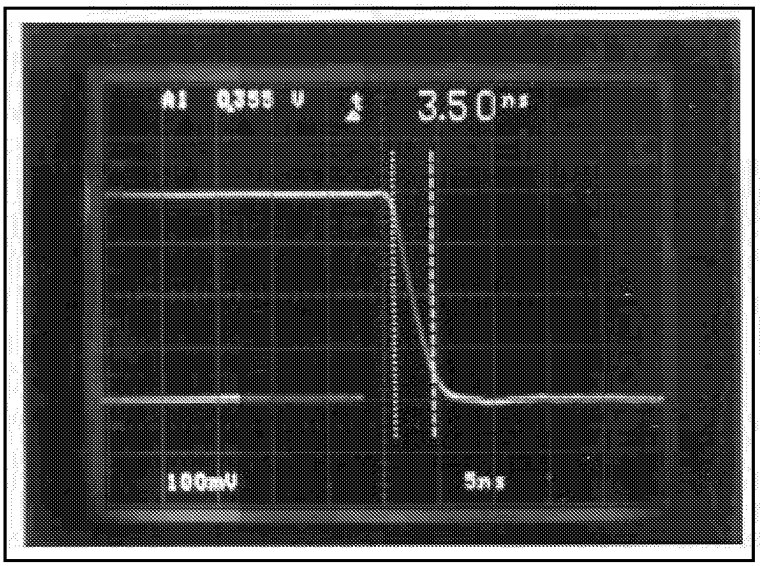


Figure 7: Rise Time for MC13281FY



100mV/div
5ns/div
10x probe

Figure 8: Fall Time for MC13281FY



100mV/div
5ns/div
10x probe

Recommend to use double sided PCB without any socket for rise/fall time measurement. Using a input pulse with 1.5ns rise time and a active probe with 1.7pF capacitance loading.

Figure 9: Single sided PCB layout. (component side, 1:1 scale)