National Semiconductor

MICROCIRCUIT DATA SHEET

CN54F240-X REV 0A0

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OCTAL BUFFERS/LINE DRIVERS WITH TRI-STATE OUTPUTS

General Description

The F240 is an octal buffer and line driver designed to be employed as a memory and address driver, clock driver and bus oriented transmitter/receiver which provides improved PC and board density.

Industry Part Number

54F240

NS Part Numbers

54F240DC

Prime Die

M240

Processing

Quality Conformance Inspection

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

Features

- Guaranteed 4000V minimum ESD protection
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA (48 mA mil)
- 12 mA source current
- Input clamp diodes limit high-speed termination effects

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Supply Voltage	
Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIH	Input HIGH Voltage	Recognized as a HIGH Signal	1	INPUTS	2.0		V	1, 2, 3
VIL	Input LOW Voltage	Recognized as a LOW Signal	1	INPUTS		0.8	V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IIN=-18mA	2, 3	INPUTS		-1.2	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, IOH=-3.0mA	2, 3	OUTPUTS	2.5		V	1, 2, 3
		VCC=4.75V, IOH=-3.0mA	2, 3	OUTPUTS	2.7		V	1, 2, 3
		VCC=4.5V, IOH=-15.0mA	2, 3	OUTPUTS	2.0		V	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, IOL=64mA	2, 3	OUTPUTS		0.5	V	1, 2, 3
IIH	Input HIGH Current	VCC=5.5V, VIN=2.7V	2, 3	INPUTS		5.0	uA	1, 2, 3
IBVI	Input HIGH Current Breakdown Test	VCC=5.5V, VIN=7.0V	2, 3	INPUTS		7.0	uA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VOUT = VCC	2, 3	OUTPUTS		100	uA	1, 2, 3
VID	Input Leakage Test	VCC = 0.0V, IID = 1.9uA, All other pins grounded	2, 3	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC = 0.0V, VIOD = 150mV, All other pins grounded	2, 3	OUTPUTS		4.75	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VIN=0.5V ($\overline{OE1}$,$\overline{OE2}$,OE2,Dn)	2, 3	INPUTS		-0.6	mA	1, 2, 3
IOZH	Output Leakage Current	VCC=5.5V, VOUT=2.7V	2, 3	OUTPUTS		50	uA	1, 2, 3
IOZL	Output Leakage Current	VCC=5.5V, VOUT=0.5V	2, 3	OUTPUTS		-50	uA	1, 2, 3
IOS	Output Short Circuit Current	VCC=5.5V, VOUT = 0V	2, 3	OUTPUTS	-100	-150	mA	1, 2, 3
IZZ	Bus Drainage Test	VCC=0.0V, VOUT=5.25V	2, 3	OUTPUTS		500	uA	1, 2, 3
ICCH	Power Supply Current	VCC=5.5V, VO = HIGH	2, 3	VCC		29	mA	1, 2, 3
ICCL	Power Supply Current	VCC=5.5V, VO = LOW	2, 3	VCC		75	mA	1, 2, 3
ICCZ	Power Supply Current	VCC=5.5V, VO = HIGH Z	2, 3	VCC		63	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS. Temp Range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to $\overline{On}$/On	3.0	7.0	ns	9
			2, 3	In to $\overline{On}$/On	3.0	8.0	ns	10, 11
tpHL(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to $\overline{On}$/On	2.0	4.7	ns	9
			2, 3	In to $\overline{On}$/On	2.0	5.7	ns	10, 11
tpZH(1)	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	$\overline{OE}$/OE to $\overline{On}$/On	2.0	4.7	ns	9
			2, 3	$\overline{OE}$/OE to $\overline{On}$/On	2.0	5.7	ns	10, 11
tpZL	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	$\overline{OE}$/OE to $\overline{On}$/On	4.0	9.0	ns	9
			2, 3	$\overline{OE}$/OE to $\overline{On}$/On	4.0	10.0	ns	10, 11
tpHZ	Disable Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	$\overline{OE}$/OE to $\overline{On}$/On	2.0	5.3	nS	9
			2, 3	$\overline{OE}$/OE to $\overline{On}$/On	2.0	6.3	nS	10, 11

Note 1: Guaranteed by applying specific input condition and testing VOL & VOH.
Note 2: Screen tested 100% on each device at +75C temperature only, subgroups A2 & A10.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature only, subgroups A2 & A10.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001724	07/08/97	Linda Collins	Legal issue with Fairchild, due to the Fairchild/National split, is forcing the change from CN74F which is 'Fairchilds' product code to CN54F which is 'Nationals' product code.