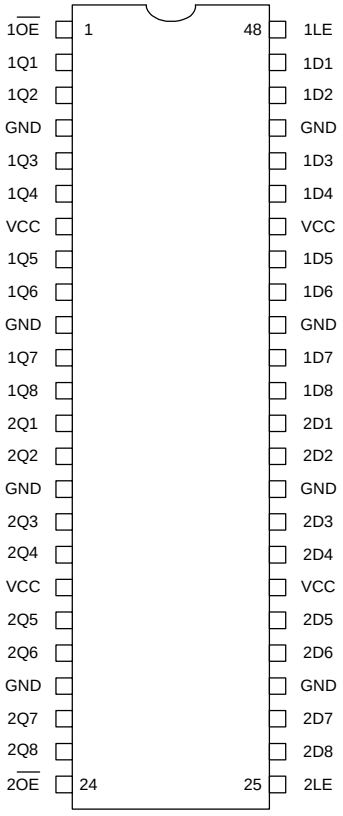
PRELIMINARY

SPACE ELECTRONICS INC.

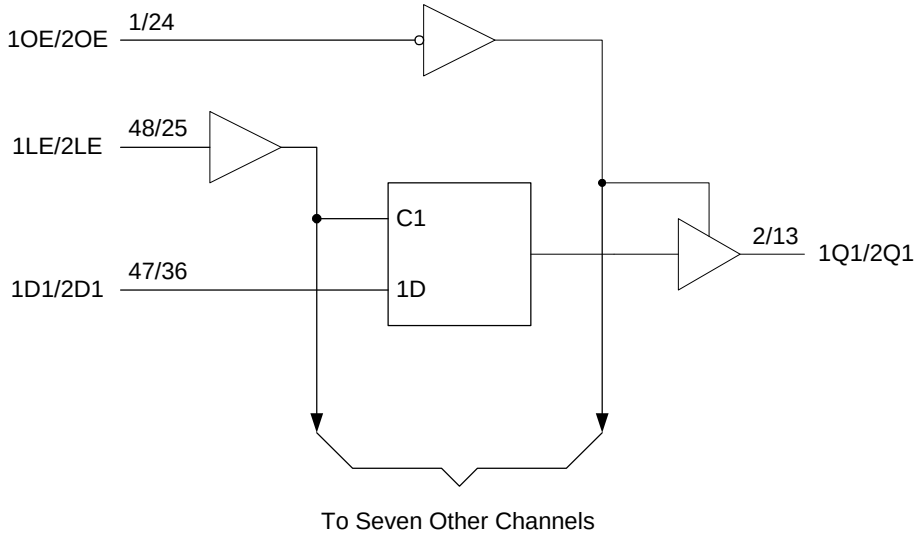
SPACE PRODUCTS

3.3V 16-BIT TRANSPARENT D-TYPE LATCHES

54LVT16373RP



Logic Diagram (PositiveLogic)



To Seven Other Channels

FEATURES:

- 3.3V low voltage advanced BiCMOS technology (LVT) 16-bit transparent D-type latches with 3-state outputs
- Total dose hardness typical 100 krad (Si); dependent upon orbit
- Single event effect:
  - SEL_{TH} : No LU > 119 MeV/mg/cm^2
- Package: 48 pin RAD-PAK® flat package
- Operating temperature range:
  - 55 °C to 125 °C
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise
- Supports mixed-mode signal operation
  - 5V input and output voltages with 3.3V V_{CC}
- Supports unregulated battery operation down to 2.7V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC}=3.3V, T_A=25 °C
- Latch-up performance exceeds 500mA per JEDEC standard
- Supports live insertion
- Bus-hold data inputs eliminate the need for external pullup resistors

DESCRIPTION:

Space Electronics' 54LVT16373RP (RP for RAD-PAK®) 16-bit transparent D-type latches with 3-state output features a minimum 100 kilorad (Si) total dose tolerance; dependent upon orbit. The 54LVT16373RP is designed for low voltage (3.3V) V_{CC} operation, but with the capability to provide a TTL interface to a 5V system environment. It is suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The 54LVT16373RP can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is low, the Q output are latched at the levels set up at the data (D) inputs. When LE is high, the Q outputs follow the D inputs. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without the need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high impedance state. The 54LVT16373RP is available with packaging and screening up to Class S.

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TABLE 1. 54LVT16373RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage range	V_{CC}	-0.5	4.6	V
Input voltage range [1]	V_I	-0.5	7	V
Voltage range applied to any output in the high state or power-off state [1]	V_O	-0.5	7	V
Current into any output in the low state	I_O	--	128	mA
Current into any output in the high state [2]	I_O	--	64	mA
Input clamp current ($V_I < 0$)	I_{IK}	--	-50	mA
Output clamp current ($V_O < 0$)	I_{OK}	--	-50	mA
Maximum power dissipation at TA = 55 °C [3]	P_D	--	0.85	W
Storage temperature range	T_{STG}	-65	150	°C

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils.

TABLE 2. 54LVT16373RP RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage	V_{CC}	2.7	3.6	V
High-level input voltage	V_{IH}	2	--	V
Low-level input voltage	V_{IL}	--	0.8	V
Input voltage	V_I	--	5.5	V
High-level output current	I_{OH}	--	-32	mA
Low-level output current	I_{OL}	--	64	mA
Input transition rise or fall rate (outputs enabled)	$\Delta t/\Delta v$	--	10	ns/V
Operating free-air temperature	T_A	-55	125	°C

1. Unused control inputs must be held high or low to prevent them from floating.

TABLE 3. 54LVT16373RP DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP [1]	MAX	UNIT
Input clamp voltage	V_{IK}	V_{CC} = 2.7V, I_I = -18 mA		--	--	-1.2	V
Output voltage high	V_{OH}	V_{CC} = MIN to MAX [2], I_{OH} = -100 µA		V_{CC} -0.2	--	--	V
		V_{CC} = 2.7V, I_{OH} = -8 mA		2.4	--	--	
		V_{CC} = 3V	I_{OH} = -32 mA	2	--	--	

TABLE 3. 54LVT16373RP DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP [1]	MAX	UNIT
Output voltage low	V_{OL}	V_{CC} = 2.7V	I_{OL} = 100 µA	--	--	0.2	V
			I_{OL} = 24 mA	--	--	0.5	
		V_{CC} = 3V	I_{OL} = 16 mA	--	--	0.4	
			I_{OL} = 32 mA	--	--	0.5	
			I_{OL} = 64 mA	--	--	0.55	
Input current	I_I	V_{CC} = 0 or MAX [2], V_I = 5.5V		--	--	10	µA
Control inputs		V_{CC} = 3.6V, V_I = V_{CC} or GND		--	--	±1	
Data inputs		V_{CC} = 3.6V	V_I = V_{CC}	--	--	1	
			V_I = 0V	--	--	-5	
Current when supply voltage is off	I_{OFF}	V_{CC} = 0, V_I or V_O = 0 to 4.5V		--	--	±100	µA
Data inputs	$I_{I(HOLD)}$	V_{CC} = 3V	V_I = 0.8V	75	--	--	µA
			V_I = 2V	-75	--	--	
Output current high-Z	I_{OZH}	V_{CC} = 3.6V, V_O = 3V		--	--	5	µA
Output current low-Z	I_{OZL}	V_{CC} = 3.6V, VO = 0.5V		--	--	-5	µA
Supply Current	I_{CC}	V_{CC} = 3.6V, I_O = 0, V_I = V_{CC} or GND		--	--	--	mA
Outputs high				--	--	0.09	
Outputs low				--	--	5	
Outputs disabled				--	--	0.09	
Increase in supply current for each input that is a specified TTL voltage level rather than V_{CC} or GND	ΔI_{CC} [3]	V_{CC} = 3V to 3.6V, One input at V_{CC} - 0.6V, Other inputs at V_{CC} or GND		--	--	0.2	mA
Input capacitance	C_I	V_I = 3V or 0		--	5	--	pF
Output capacitance	C_O	V_O = 3V or 0		--	9.5	--	pF

1. All typical values are at V_{CC} = 3.3V, T_A = 25 °C.
2. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TABLE 4. 54LVT16373RP AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		UNIT
		MIN	MAX	MIN	MAX	
Pulse duration, LE high	t_W	3.3	--	3.3	--	ns
Setup time, data before LE↓	t_{SU}	0.5	--	0.5	--	ns
Hold time, data after LE↓	t_H	1.8	--	2	--	ns

TABLE 5. 54LVT16373RP SWITCING CHARACTERISTICS

(C_L = 50 pF, -55 °C ≤ T_A ≤ 125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V		UNIT
			MIN	TYP [1]	MAX	MIN	MAX	
t_{PLH}	D	Q	1.3	2.7	5	--	5.7	ns
t_{PHL}			1.4	2.9	4.9	--	5.7	
t_{PLH}	LE	Q	2.1	3.6	6	--	6.8	ns
t_{PHL}			3	4.7	6.9	--	8.8	
t_{PZH}	$\overline{OE}$	Q	1	2.9	5.3	--	6.3	ns
t_{PZL}			1.3	3	5.1	--	5.9	
t_{PHZ}	$\overline{OE}$	Q	2.7	4.3	6.8	--	7.6	ns
t_{PLZ}			2.6	4	5.8	--	5.9	

1. All typical values are at V_{CC} = 3.3V, T_A = 25 °C.

FIGURE 1. LOAD CIRCUIT FOR OUTPUTS

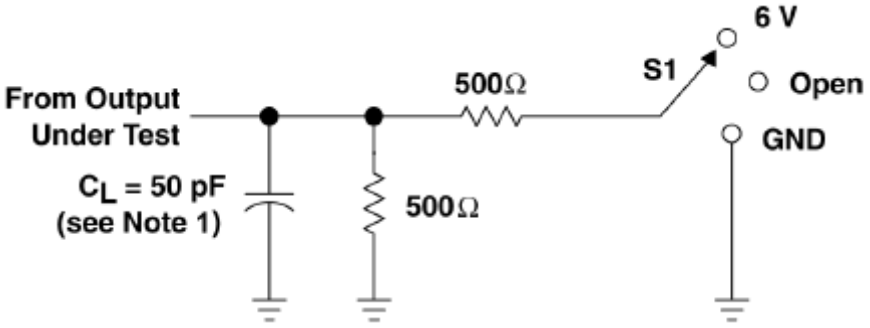


FIGURE 2. VOLTAGE WAVEFORMS PULSE DURATION

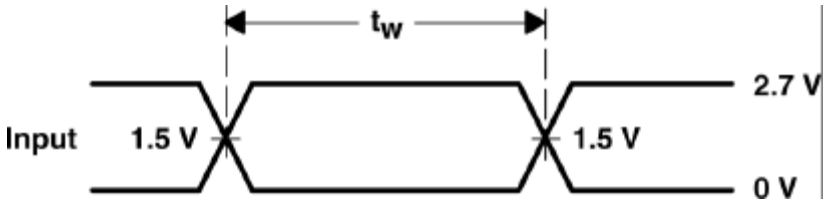


FIGURE 3. VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

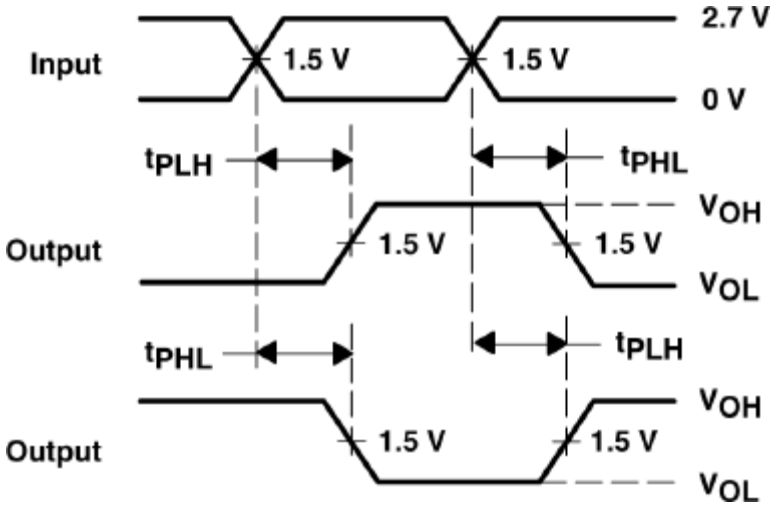


FIGURE 4. VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

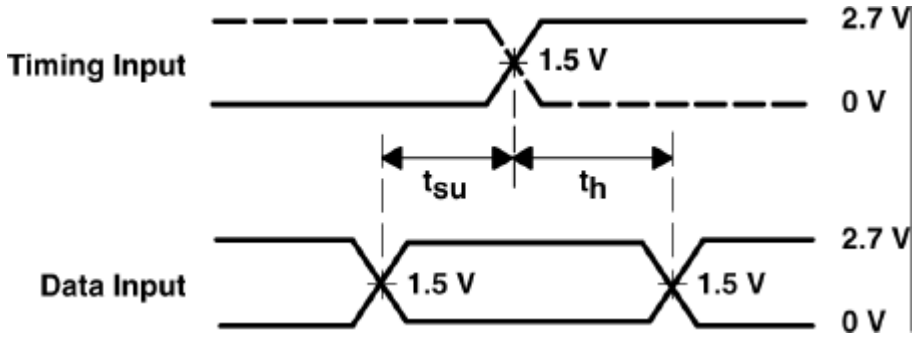
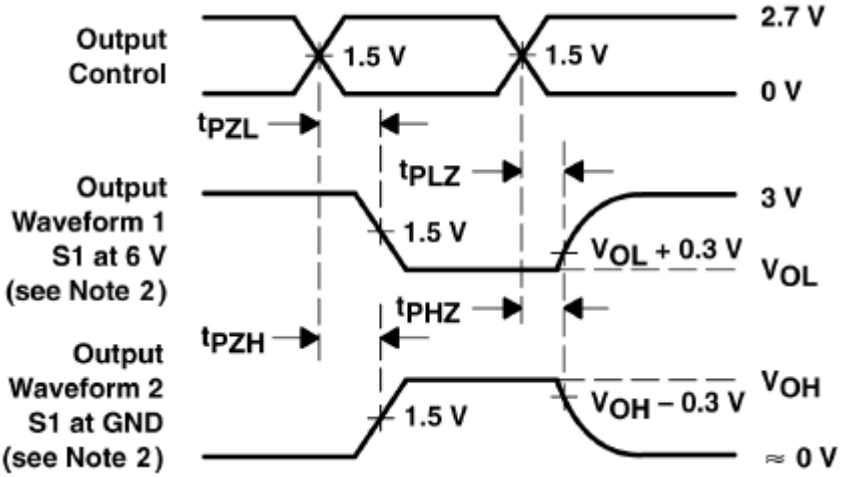


FIGURE 5. VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, ZO = 5W, tr $\leq$ 2.5 ns, tf $\leq$ 2.5 ns.
4. The outputs are measured one at a time with one transition per measurement.