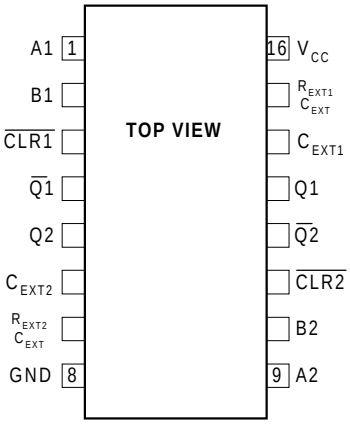
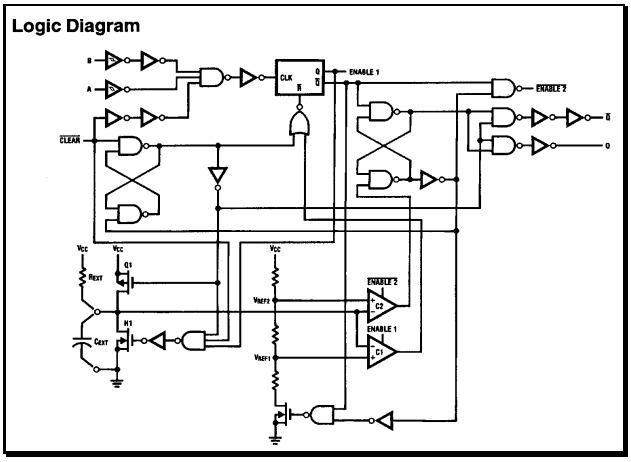
SEi - Radiation Hardened 54HC123RP

Dual Retriggerable Monostable Multivibrator





Features

- RAD-PAK® Technology Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Typical Propagation Delay: 25ns
- Package:
  -16 Pin RAD-PAK® Flat Package
  -16 Pin RAD-PAK® DIP
- Wide Power Supply Range: 2V - 6V
- Low Input Current: 1 uA maximum
- Simple Pulse Width formula T = RC
- Wide Pulse Range: 400 ns to ∞
- Fanout of 10 LS-TTL Loads
- Schmitt Trigger A & B Inputs Enable Infinite Signal Input Rise and Fall Times
- Screening per TM 5004
- QCI per TM5005

SEi's 54HC123RP (RP for RAD-PAK®) high speed monostable multivibrators features a 100 kilorad (Si) total dose tolerance. Using advanced CMOS technology, the 54HC123RP features speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristics. Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. A clear input that when taken low resets the one shot. The 54HC123RP can be triggered on the positive transition of the clear while A is held low and B is held high. It may be triggered repeatedly while their outpus are generating a pulse and the pulse will be extended. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It provides a 100 krad or better (Si) total dose survivability, based on a GEO type orbit. Actual TID tolerance is dependent upon orbit and mission duration. Capable of surviving space environments, the 54HC123RP is ideal for many satellite, spacecraft, and space probe missions. The radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. The 54HC123RP is available in Class S packaging and screening.

SPACE ELECTRONICS INC.
4031 Sorrento Valley Blvd.
San Diego, CA 92121
(619) 452-4167 Fax (619) 452-5499
Email: sales@spaceelectronics.com
http:\\www.spaceelectronics.com

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Dual Retriggerable Monostable Multivibrator

54HC123RP ABSOLUTE MAXIMUM RATINGS 1/ 2/

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	-0.5	+7.0	V
DC Input Voltage	V_{IN}	-1.5	V_{CC}+1.5	V
DC Output Voltage	V_{OUT}	-0.5	V_{CC}+0.5	V
Clamp Diode Current	I_{IK}, I_{OK}		±20	mA
DC Output Current, per pin	I_{OUT}		±25	mA
DC V_{CC} or GND Current, per pin	I_{CC}		±50	mA
Storage Temperature Range	T_{STG}	-65	+150	°C
Power Dissipation	P_D		500	mW

Note:
1/ Maximum Ratings are those values beyond which damage to the device may occur.
2/ All voltages are referenced to ground, unless otherwise specified.

54HC123RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	+2.0	+6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_A	-55	+125	°C
Input Rise or Fall Times	t_r t_f			
V_{CC} = 2.0V		0	1000	ns
V_{CC} = 4.5V		0	500	
V_{CC} = 6.0V		0	400	

54HC123RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	TYP	MAX	UNIT
Minimum High Level Input Voltage	V_{IH}			
V_{CC} = 2.0V			1.5	V
V_{CC} = 4.5V			3.15	
V_{CC} = 6.0V			4.2	
Maximum Low Level Input Voltage	V_{IL}			
V_{CC} = 2.0V			0.3	V
V_{CC} = 4.5V			0.9	
V_{CC} = 6.0V			1.2	
Minimum High Level Output Voltage	V_{OH}			
V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq$ 20uA				
V_{CC}=2.0V		2.0	1.9	V
V_{CC}=4.5V		4.5	4.4	
V_{CC}=6.0V		6.0	5.9	
V_{IN} = V_{IH} or V_{IL}				
$\|I_{OUT}\| \leq$ 4.0mA @V_{CC} = 4.5V		4.2	3.7	
$\|I_{OUT}\| \leq$ 5.2mA @V_{CC} = 6.0V		5.7	5.2	
Maximum Low Level Output Voltage	V_{OL}			
V_{IN} = V_{IH} or V_{IL}				
$\|I_{OUT}\| \leq$ 20uA				
V_{CC} = 2.0V		0	0.1	V
V_{CC} = 4.5V		0	0.1	
V_{CC} = 6.0V		0	0.1	
V_{IN}=V_{IH} or V_{IL}				
$\|I_{OUT}\| \leq$ 4.0mA @V_{CC} = 4.5V		0.2	0.4	
$\|I_{OUT}\| \leq$ 5.2mA @V_{CC} = 6.0V		0.2	0.4	
Maximum Input Current (Pins 7,15)	I_{IN}		±5.0	uA
V_{IN} = V_{CC} @V_{CC} = 6.0V				
(All Other Pins)			±1.0	uA
V_{IN} = V_{CC} @V_{CC} = 6.0V				
Maximum Quiescent Supply Current (standby)	I_{CC}			
V_{IN} = V_{CC} or GND @V_{CC} = 6.0V			160	uA
$\|I_{OUT}\|$ = 0uA				
Maximum Active Supply Current (per monostable)				
V_{IN} = V_{CC} or GND , R/C_{EXT} = 0.5VCC				
V_{CC}=2.0V		36	130	uA
V_{CC}=4.5V		0.33	1.6	mA
V_{CC}=6.0V		0.7	3.2	mA

Note:
1. For a power supply of 5V±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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SEi - Radiation Hardened **54HC123RP**

Dual Retriggerable Monostable Multivibrator

54HC123RP AC ELECTRICAL CHARACTERISTICS V_{CC}=5V,T_A =25°C,C_l =15pF, t_r = t_f = 6ns

PARAMETER	SYMBOL	TYP	MAX	UNIT
Maximum Trigger Propagation Delay A, B or Clear to Q	T_{PLH}	22	33	ns
Maximum Trigger Propagation Delay A, B or Clear to Q\	T_{PHL}	25	42	ns
Maximum Propagation Delay, Clear to Q	T_{PHL}	20	27	ns
Maximum Propagation Delay, Clear to Q\	T_{PLH}	22	33	ns
Minimum Pulse Width, A, B or Clear	T_W	14	26	ns
Minimum Clear Removal Time	T_{REM}		0	ns
Minimum Output Pulse Width C_{EXT} = 28pF, R_{EXT} = 2kΩ	$T_{WQ(MIN)}$	400		ns
Output Pulse Width C_{EXT} = 1000pF, R_{EXT} = 10kΩ	T_{WQ}	10		us

54HC123RP AC ELECTRICAL CHARACTERISTICS C_l = 50pF, t_r = t_f = 6ns (unless otherwise specified)

PARAMETER	SYMBOL	VCC	TYP	LIMIT	UNIT
Maximum Trigger Propagation Delay A, B or Clear to Q	T_{PLH}	2.0V 4.5V 6.0V	77 26 21	210 57 44	ns
Maximum Trigger Propagation Delay A, B or Clear to Q\	T_{PHL}	2.0V 4.5V 6.0V		250 67 51	ns
Maximum Propagation Delay, Clear to Q	T_{PHL}	2.0V 4.5V 6.0V		143 45 36	ns
Maximum Propagation Delay, Clear to Q\	T_{PLH}	2.0V 4.5V 6.0V		147 46 37	ns
Minimum Pulse Width, A, B or Clear	T_W	2.0V 4.5V 6.0V		157 42 30	ns
Minimum Clear Removal Time	T_{REM}	2.0V 4.5V 6.0V		0 0 0	ns
Minimum Output Pulse Width C_{EXT} = 28pF, R_{EXT} = 2kΩ, R_{EXT} = 6kΩ (V_{CC} = 2V)	$T_{WQ(MIN)}$	2.0V 4.5V 6.0V	1.5 450 380		us ns ns
Output Pulse Width C_{EXT} = 0.1uF, R_{EXT} = 10kΩ: min max	T_{WQ}	 5.0V 5.0V	 1 1	 0.85 1.15	ms
Maximum Output Rise and Fall Time	T_{TLH}, T_{THL}	2.0V 4.5V 6.0V	30 8 7	110 22 19	ns
Maximum Input Capacitance (Pins 7,15)	C_{IN}		12	20	pF
Maximum Input Capacitance (All Other Pins)			6	10	pF
Power Dissipation Capacitance 1/	C_{PD}		70		pF

Note:
1/ C_{PD} determines the no lead dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

54HC123RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-16	16 Pin Dual In Line Package (0.840 x 0.310)
F	F-16A	16 Pin Flat Package (0.423 x 0.285)

Note:
1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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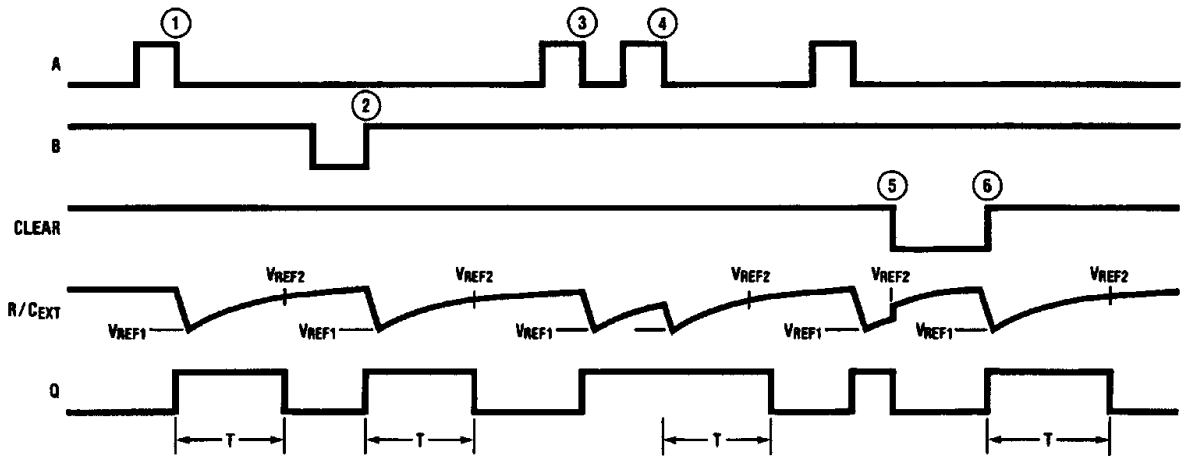
Theory of Operation



54HC123RP TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} Completely charged to Vcc. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N channel transistor N1. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this pointthe output of comparator Cl changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward Vcc. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger. A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}). The 'HCl 23A can also be triggered when clear goes from GND to VOC (while A is at GND and B is at Vcc).

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC}; causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value Of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The 54HC123RP is retriggered if a valid trigger occurs followed by another trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at the R/C_{EXT} pin has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated, the voltage at the R/C_{EXT} pin will again drop to V_{REF1}, before progressing along the RC charging curve toward Vcc. The Q output will remain high until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr} \approx 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256V_{CC})C_X}{(V_{CC} - 0.7)^2}$$

Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

$$t_{rr} \approx 196 + \frac{640}{V_{CC} - 0.7} + \frac{522 + (0.3V_{CC})C_X}{(V_{CC} - 0.7)^2} \text{ns}$$

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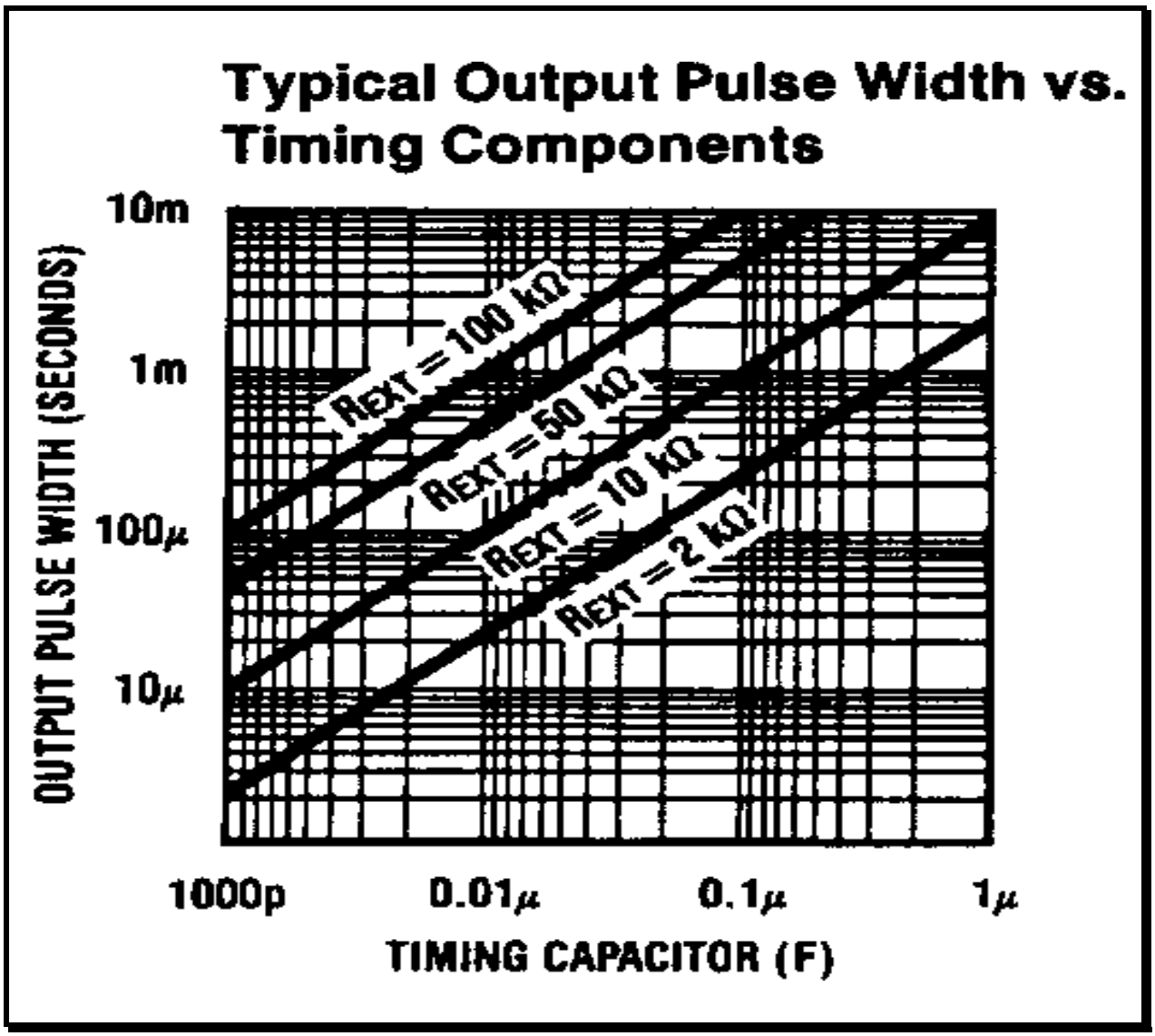
RESET OPERATION

These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1. When the voltage on the capacitor reaches VREF2, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and Q\ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.



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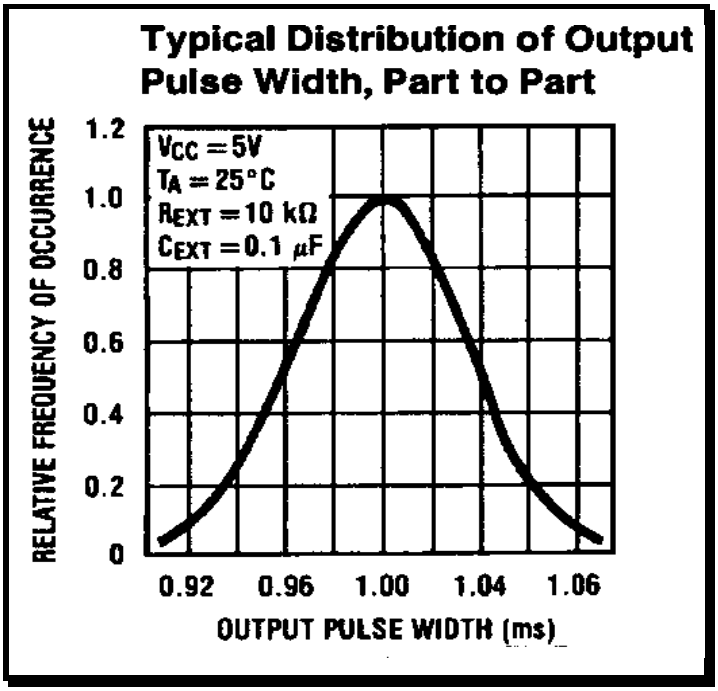

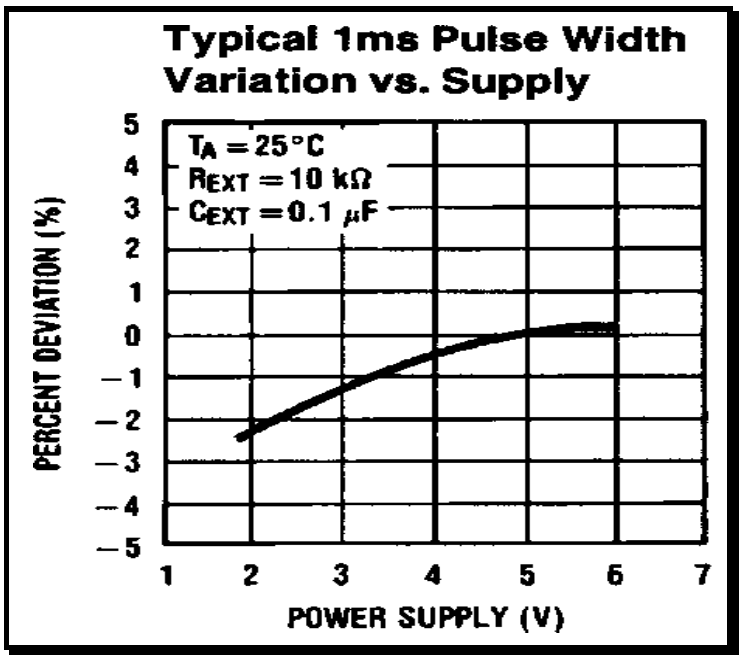

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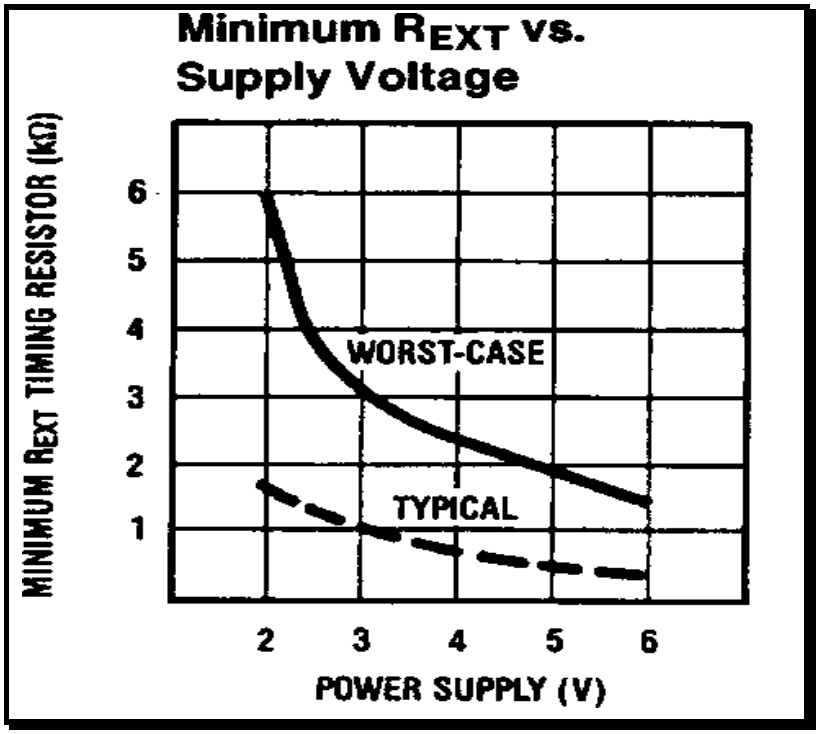

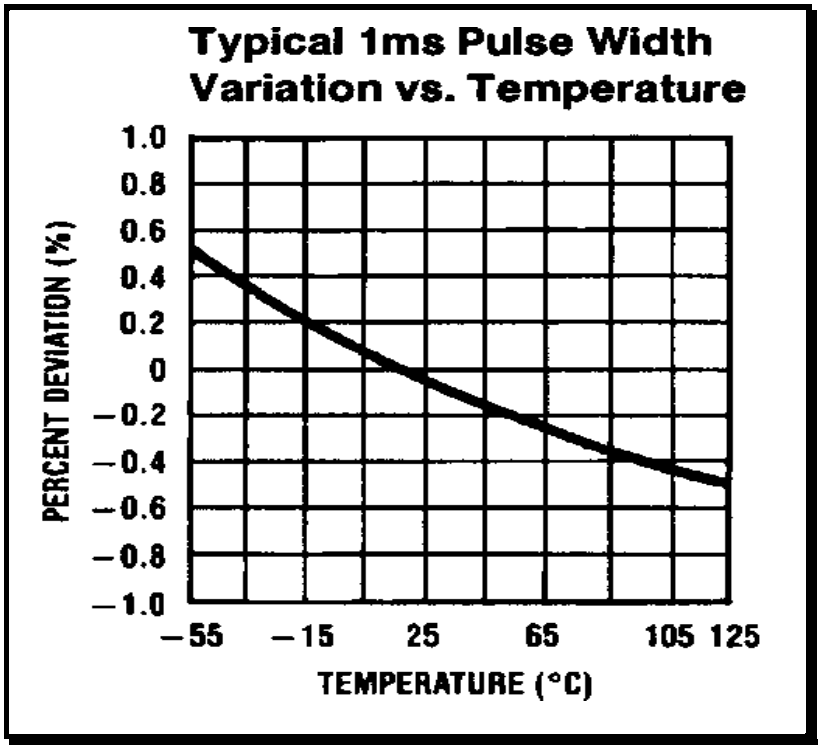

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