V_{DSM} = 5200 V
I_{TAVM} = 2760 A
I_{TRMS} = 4340 A
I_{TSM} = 42000 A
V_{T0} = 1.00 V
r_T = 0.225 mΩ

Phase Control Thyristor

5STP 25L5200

Doc. No. 5SYA1008-03 Sep. 01

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

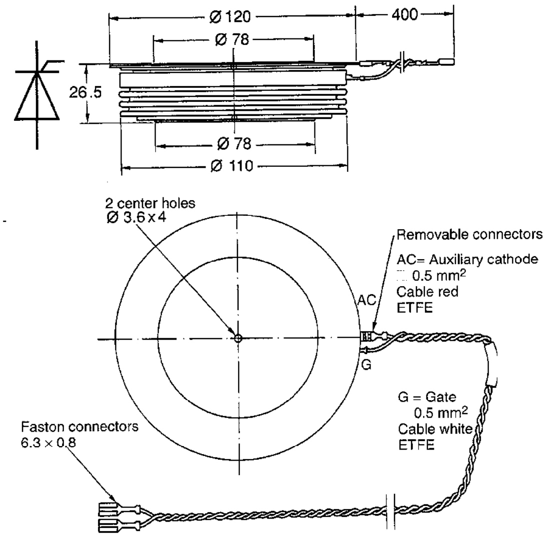
Blocking

Part Number	**5STP 25L5200**	**5STP 25L5000**	**5STP 25L4600**	Conditions	
V_{DSM} V_{RSM}	5200 V	5000 V	4600 V	f = 5 Hz, t_p = 10ms	
V_{DRM} V_{RRM}	4400 V	4200 V	4000 V	f = 50 Hz, t_p = 10ms	
V_{RSM1}	5700 V	5500 V	5100 V	t_p = 5ms, single pulse	
I_{DSM}	≤ 400 mA			V_{DSM}	T_j = 125°C
I_{RSM}	≤ 400 mA			V_{RSM}	
dV/dt_{crit}	2000 V/µs			Exp. to 0.67 x V_{DRM}, T_j = 125°C	

V_{DRM}/ V_{RRM} are equal to V_{DSM}/ V_{RSM} values up to T_j = 110°C

Mechanical data

F_M	Mounting force	nom.	70 kN
		min.	63 kN
		max.	84 kN
a	Acceleration Device unclamped Device clamped		 50 m/s^2 100 m/s^2
m	Weight		1.45 kg
D_S	Surface creepage distance		36 mm
D_a	Air strike distance		15 mm



On-state

I_{TAVM}	Max. average on-state current	2760 A	Half sine wave, T_C = 70°C	
I_{TRMS}	Max. RMS on-state current	4340 A		
I_{TSM}	Max. peak non-repetitive	42000 A	tp = 10 ms	T_j = 125°C
	surge current	45000 A	tp = 8.3 ms	After surge:
I^2t	Limiting load integral	8820 kA^2s	tp = 10 ms	$V_D = V_R$ = 0V
		8404 kA^2s	tp = 8.3 ms	
V_T	On-state voltage	1.70 V	I_T = 3000 A	T_j = 125°C
V_{T0}	Threshold voltage	1.00 V	I_T = 1300 - 4000 A	
r_T	Slope resistance	0.225 mΩ		
I_H	Holding current	50-125 mA	T_i = 25°C	
		15-60 mA	T_i = 125°C	
I_L	Latching current	100- mA	T_i = 25°C	
		75-250 mA	T_i = 125°C	

Switching

di/dt_{crit}	Critical rate of rise of on-state current		250 A/µs	Cont. f = 50 Hz	$V_D \le 0.67 \cdot V_{DRM}$, T_j = 125°C I_{TRM} = 3000 A I_{FG} = 2 A, t_r = 0.5 µs
			500 A/µs	60 sec. f = 50Hz	
t_d	Delay time		≤ 3.0 µs	$V_D = 0.4 \cdot V_{DRM}$	I_{FG} = 2 A, t_r = 0.5 µs
t_q	Turn-off time		≤ 700 µs	$V_D \le 0.67 \cdot V_{DRM}$ dv_D/dt = 20V/µs	I_{TRM} = 3000 A, T_j = 125°C V_R > 200 V, di_T/dt = -5 A/µs
Q_{rr}	Recovery charge	min	5500 µAs		
		max	7500 µAs		

Triggering

V_{GT}	Gate trigger voltage	2.6 V	T_j = 25°
I_{GT}	Gate trigger current	400 mA	T_j = 25°
V_{GD}	Gate non-trigger voltage	0.3 V	V_D =0.4 x V_{DRM}
I_{GD}	Gate non-trigger current	10 mA	V_D = 0.4 x V_{DRM}
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Gate power loss	3 W	

Thermal

T_{jmax}	Max. operating junction temperature range	125 °C	
T_{stg}	Storage temperature range	-40…140 °C	
R_{thJC}	Thermal resistance junction to case	14 K/kW	Anode side cooled
		14 K/kW	Cathode side cooled
		7 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	3 K/kW	Single side cooled
		1.5 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	4.7	0.853	1.07	0.49
τ_i(s)	0.4787	0.0824	0.0104	0.0041

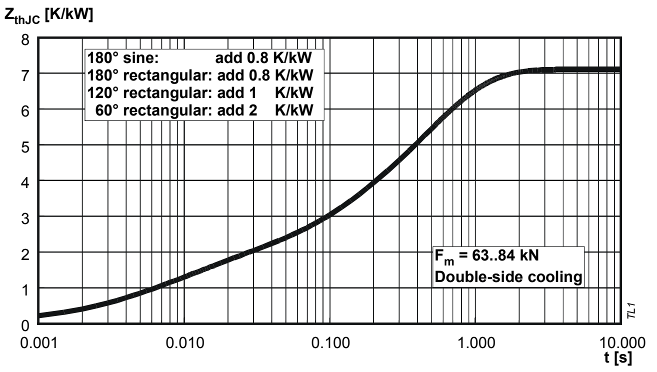


Fig. 1 Transient thermal impedance junction to case.

On-state characteristic model:

$$VT = A + B \cdot iT + C \cdot \ln(iT + 1) + D \cdot \sqrt{IT}$$

Valid for i_T = 500 – 10000 A

A	B	C	D
-0.006184	0.00022	0.173291	-0.006405

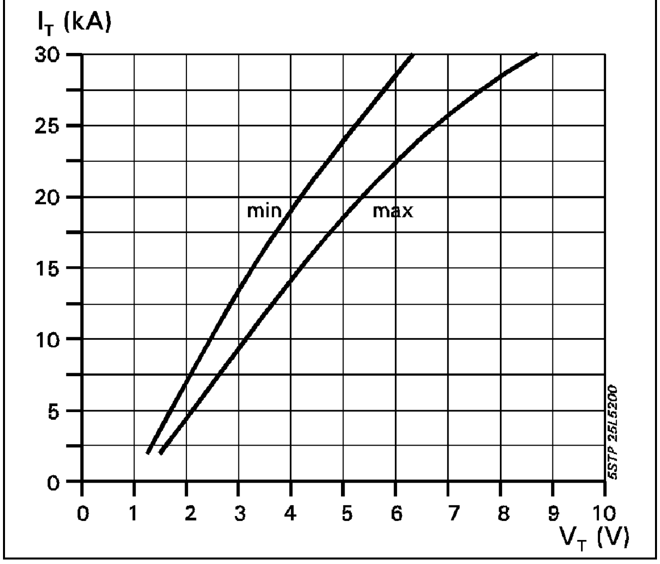


Fig. 2 On-state characteristics.
T_j=125°C, 10ms half sine

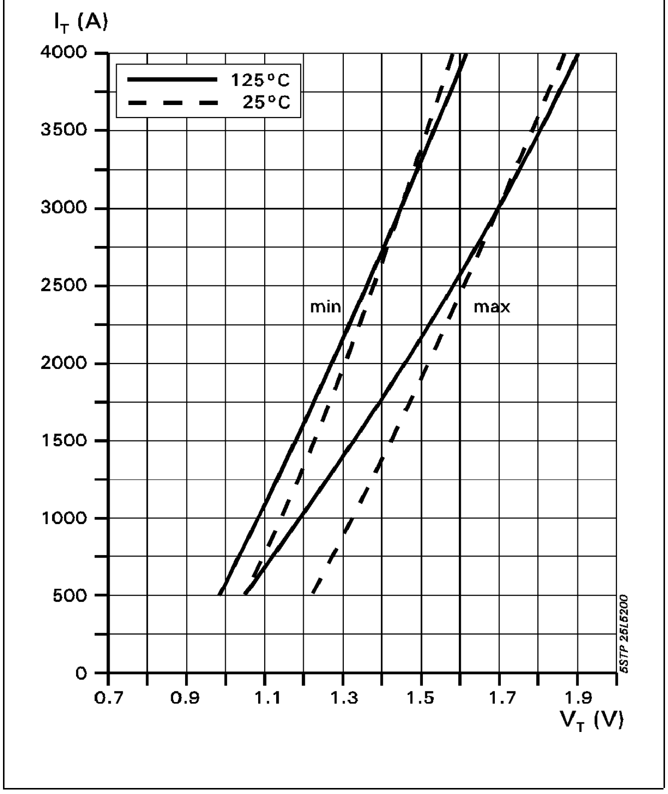


Fig. 3 On-state characteristics.

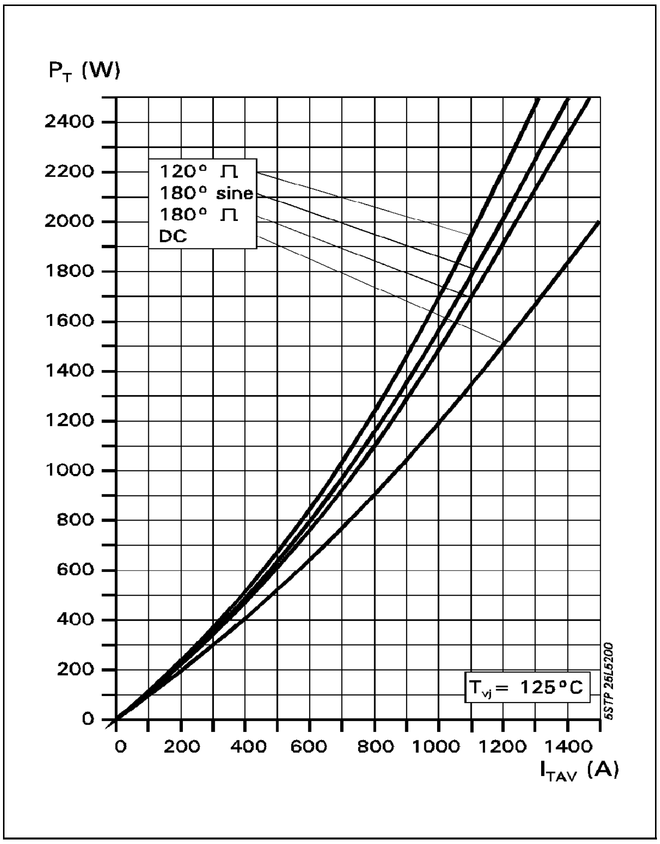


Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.

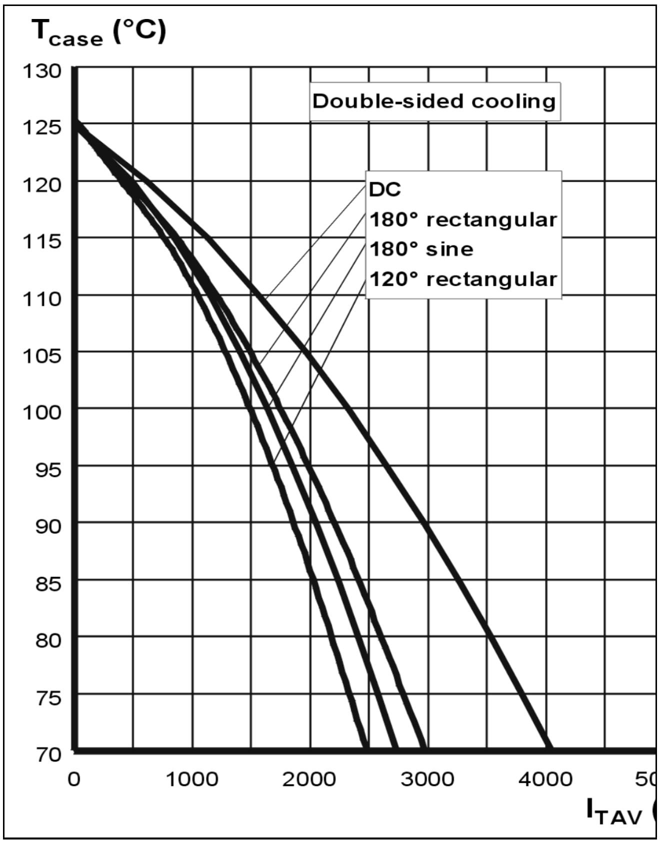


Fig. 5 Max. permissible case temperature vs. mean on-state current.

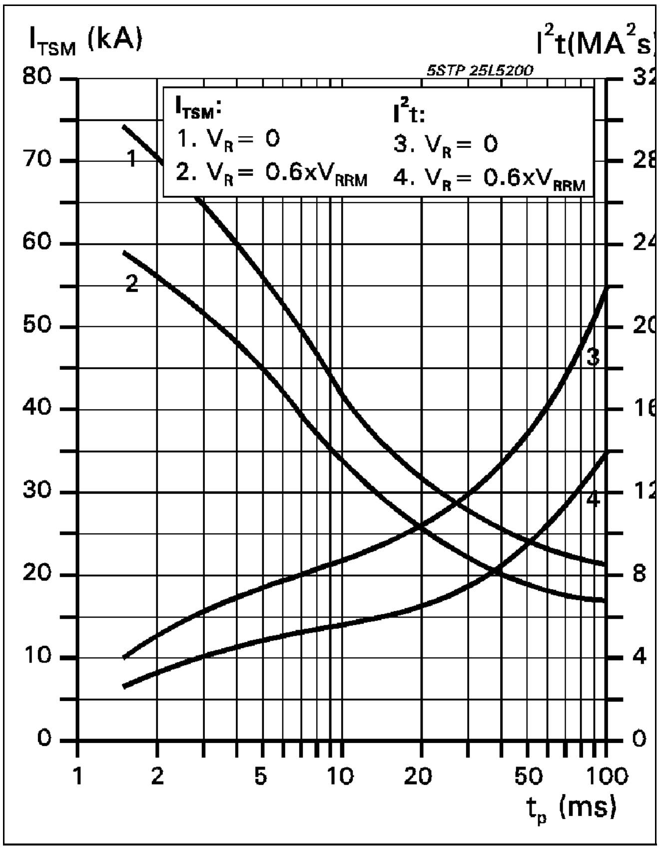


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

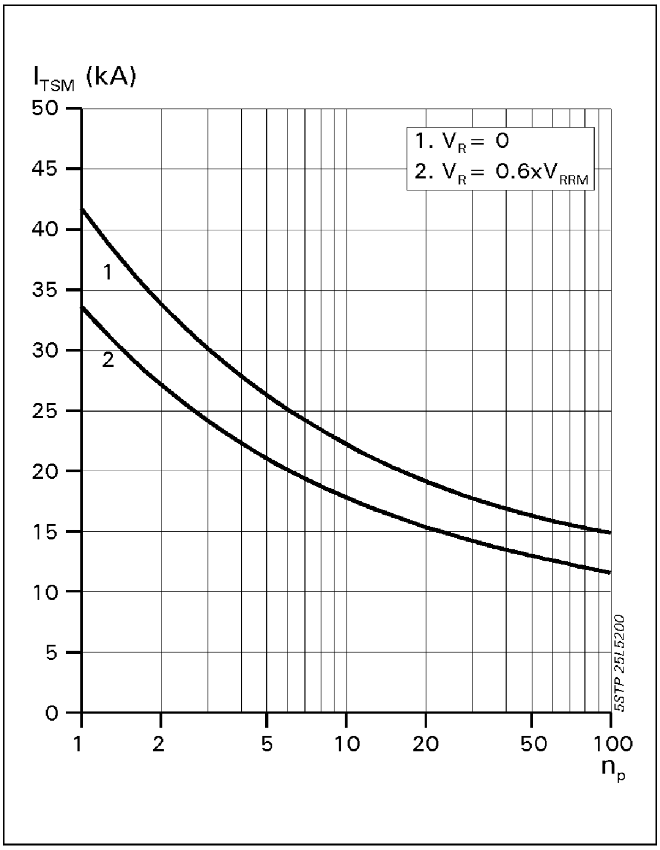


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

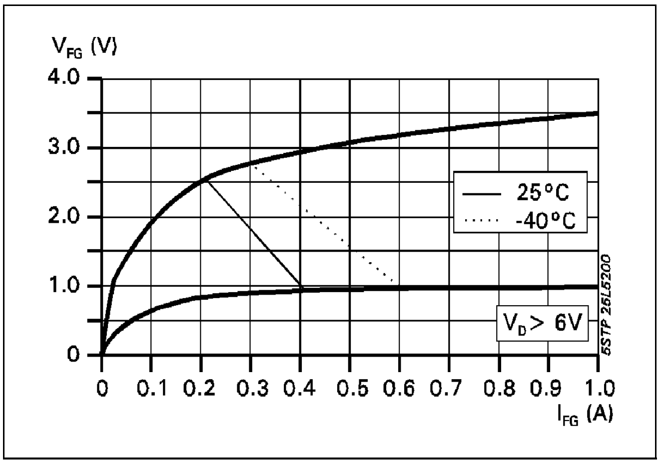


Fig. 8 **Gate trigger characteristics.**

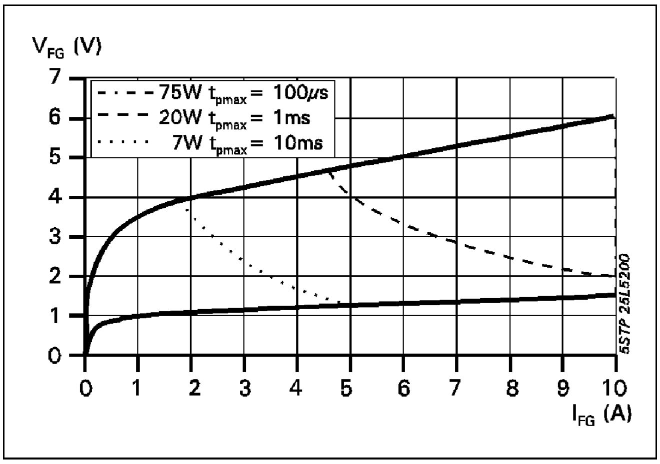


Fig. 9 **Max. peak gate power loss.**

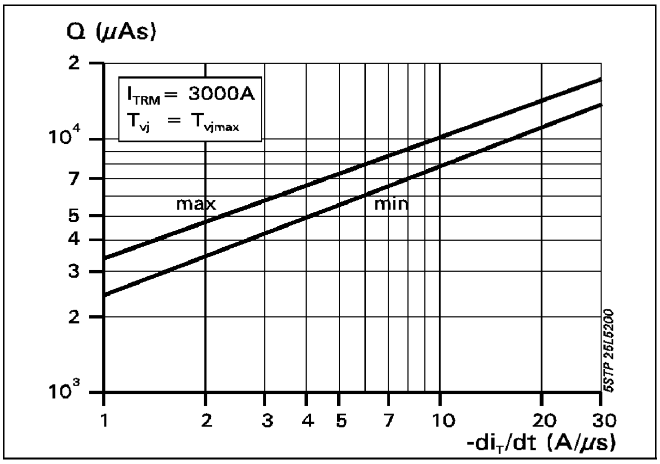


Fig. 10 **Recovery charge vs. decay rate of on-state current.**

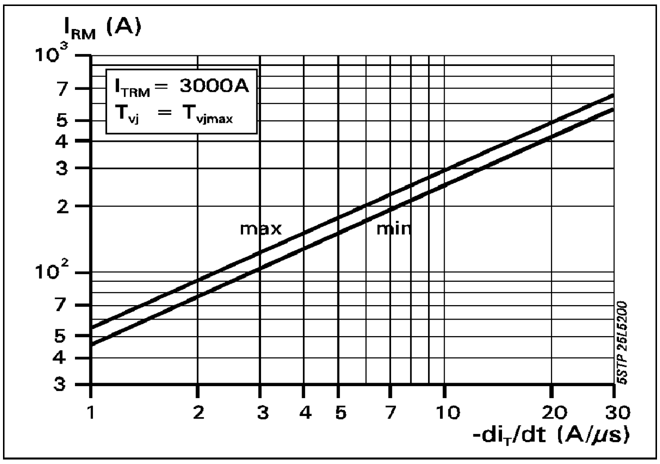


Fig. 11 **Peak reverse recovery current vs. decay rate of on-state current.**

Turn - off time, typical parameter relationship.

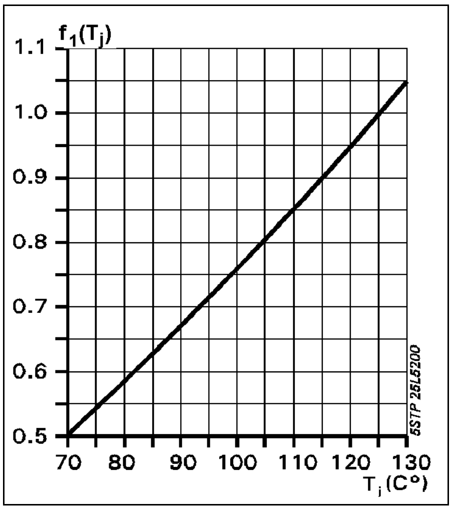


Fig. 12 **$t_q/t_{q1} = f_1(T_j)$**

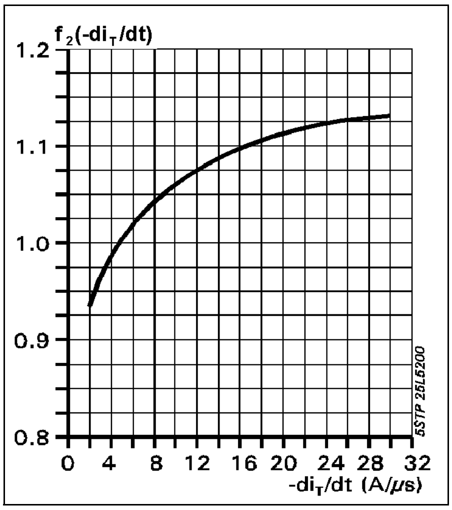


Fig. 13 **$t_q/t_{q1} = f_2(-di_T/dt)$**

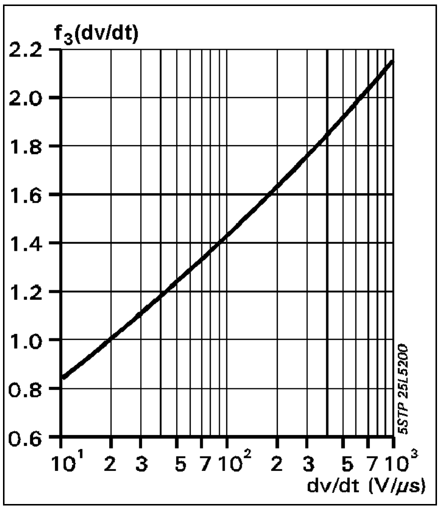


Fig. 14 **$t_q/t_{q1} = f_3(dv/dt)$**

$t_q = t_{q1} \bullet f_1(T_j) \bullet f_2(-di_T/dt) \bullet f_3(dv/dt)$

t_{q1} :at normalized values (see page 2)
t_q : at varying conditions

Turn-on and Turn-off losses

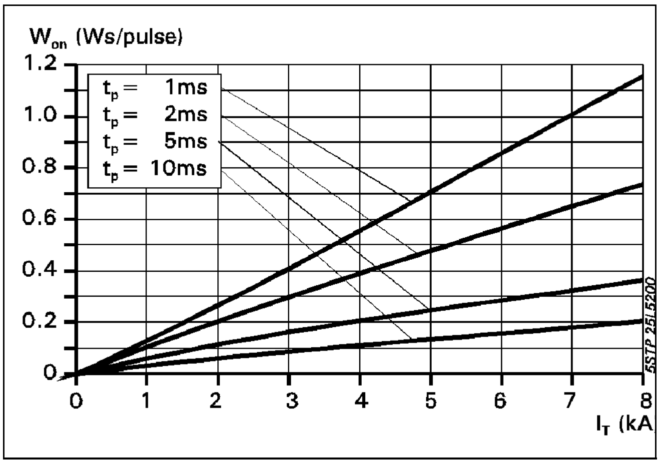


Fig. 15 $W_{on} = f(I_T, t_P)$, $T_j = 125°C$.
Half sinusoidal waves.

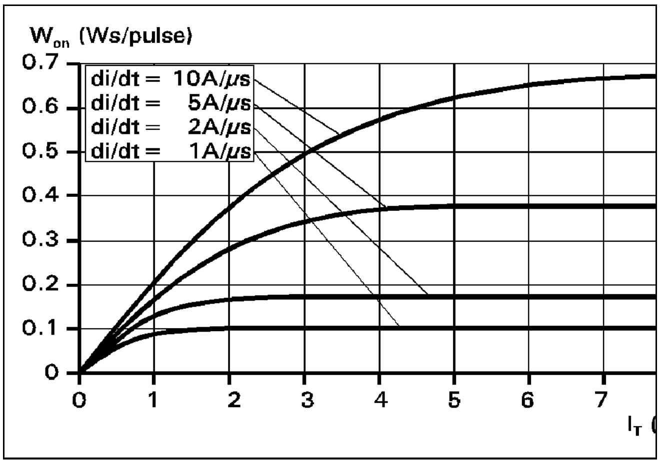


Fig. 16 $W_{on} = f(I_T, di/dt)$, $T_j = 125°C$.
Rectangular waves.

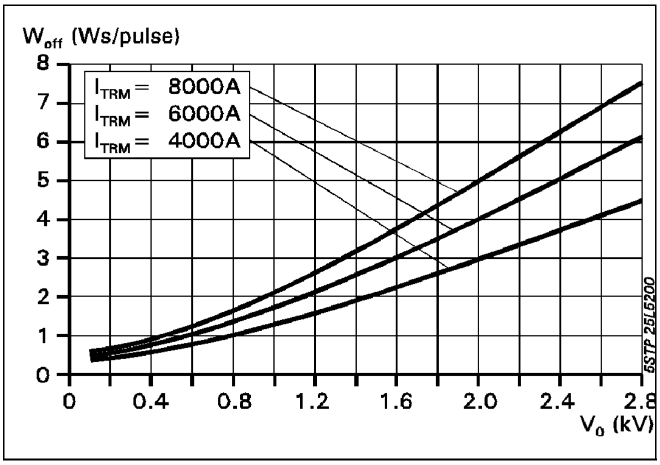


Fig. 17 $W_{off} = f(V_0, I_T)$, $T_j = 125°C$.
Half sinusoidal waves. $t_P = 10$ **ms.**

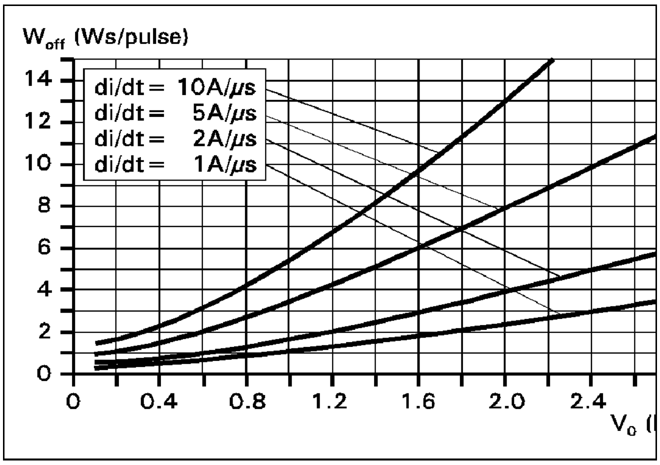
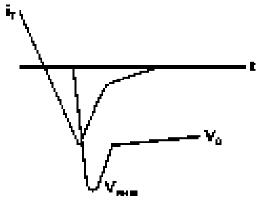


Fig. 18 $W_{off} = f(V_0, di/dt)$, $T_j = 125°C$.
Rectangular waves.



$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

W_{off} at $V_{RRM}/V_0 = 1.3-1.5$

$$P_T = \frac{1}{T}\int_0^T i_T \cdot v_T \, dt$$

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