

$V_{DSM} = 1800 \text{ V}$
 $I_{TAVM} = 3000 \text{ A}$
 $I_{TRMS} = 4710 \text{ A}$
 $I_{TSM} = 47000 \text{ A}$
 $V_{T0} = 0.88 \text{ V}$
 $r_T = 0.103 \text{ m}\Omega$

Phase Control Thyristor

5STP 27H1800

Doc. No. 5SYA1048-02 Sep. 01

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability

Blocking

Part Number	5STP 27H1800	5STP 27H1600	5STP 27H1200	Conditions
V_{DSM} V_{RSM}	1800 V	1600 V	1200 V	$f = 5 \text{ Hz}$, $t_p = 10 \text{ ms}$
V_{DRM} V_{RRM}	1800 V	1600 V	1200 V	$f = 50 \text{ Hz}$, $t_p = 10 \text{ ms}$
V_{RSM1}	2000 V	1800 V	1400 V	$t_p = 5 \text{ ms}$, single pulse
I_{DRM}	$\leq 200 \text{ mA}$			V_{DRM} $T_j = 125^\circ\text{C}$
I_{RRM}	$\leq 200 \text{ mA}$			V_{RRM}
dV/dt_{crit}	1000 V/ μs			@ Exp. to $0.67 \times V_{DRM}$ $T_j = 125^\circ\text{C}$

Mechanical data

F_M	Mounting force	nom.	50 kN
		min.	45 kN
		max.	60 kN
a	Acceleration		
	Device unclamped		50 m/s ²
	Device clamped		100 m/s ²
m	Weight		0.9 kg
D_S	Surface creepage distance		36 mm
D_a	Air strike distance		15 mm

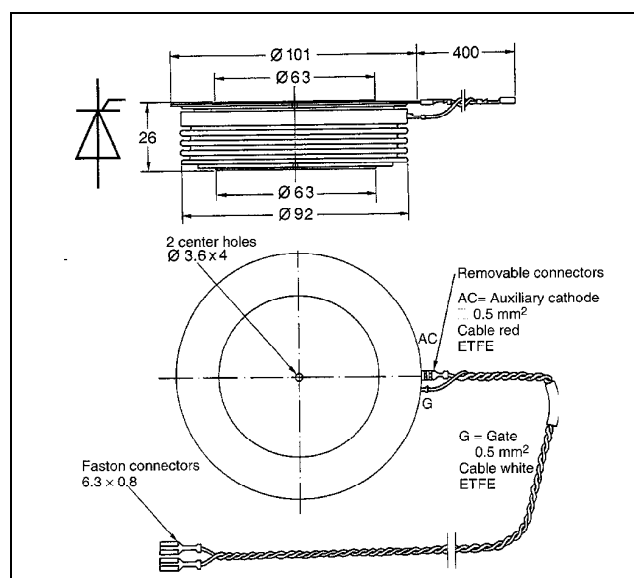


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On-state

I _{TAVM}	Max. average on-state	3000 A	Half sine wave, T _C = 70°C	
I _{TRMS}	Max. RMS on-state current	4710 A		
I _{TSM}	Max. peak non-repetitive	47000 A	tp = 10 ms	T _j = 125°C
	surge current	50000 A	tp = 8.3 ms	After surge:
I ² t	Limiting load integral	11045 kA ² s	tp = 10 ms	V _D = V _R = 0V
		10375 kA ² s	tp = 8.3 ms	
V _T	On-state voltage	1.21 V	I _T = 3000 A	T _j = 125°C
V _{T0}	Threshold voltage	0.88 V	I _T = 2000 - 6000 A	
r _T	Slope resistance	0.103 mΩ		
I _H	Holding current	20-70 mA	T _j = 25°C	
		15-60 mA	T _j = 125°C	
I _L	Latching current	150-600 mA	T _j = 25°C	
		50-200 mA	T _j = 125°C	

Switching

di/dt_{crit}	Critical rate of rise of on-state current	150 A/ μs	Cont. $f = 50\text{ Hz}$	$V_D \leq 0.67 \cdot V_{DRM}$, $T_j = 125^\circ\text{C}$ $I_{TRM} = 3000\text{ A}$ $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$
		300 A/ μs	60 sec. $f = 50\text{ Hz}$	
t_d	Delay time	$\leq 3.0\text{ }\mu\text{s}$	$V_D = 0.4 \cdot V_{DRM}$	$I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$
t_q	Turn-off time	$\leq 400\text{ }\mu\text{s}$	$V_D \leq 0.67 \cdot V_{DRM}$ $dv_D/dt = 20\text{ V}/\mu\text{s}$	$I_{TRM} = 3000\text{ A}$, $T_j = 125^\circ\text{C}$ $V_R > 200\text{ V}$, $di_T/dt = -20\text{ A}/\mu\text{s}$
Q_{rr}	Recovery charge	min 1800 μAs		
		max 4500 μAs		

Triggering

V_{GT}	Gate trigger voltage	2.6 V	$T_j = 25^\circ\text{C}$	
I_{GT}	Gate trigger current	400 mA	$T_j = 25^\circ\text{C}$	
V_{GD}	Gate non-trigger voltage	0.3 V	$V_D = 0.4 \cdot V_{DRM}$	$T_j = 125^\circ\text{C}$
I_{GD}	Gate non-trigger current	10 mA	$V_D = 0.4 \cdot V_{DRM}$	$T_j = 125^\circ\text{C}$
V_{FGM}	Peak forward gate voltage	12 V		
I_{FGM}	Peak forward gate current	10 A		
V_{RGM}	Peak reverse gate voltage	10 V		
P_G	Gate power loss	3 W		

Thermal

T_j	Operating junction temperature range	-40...125 °C	Anode side cooled
T_{stg}	Storage temperature range	-40...150 °C	
R_{thJC}	Thermal resistance junction to case	20 K/kW	
		20 K/kW	
		10 K/kW	Cathode side cooled
R_{thCH}	Thermal resistance case to heat sink	4 K/kW	Double side cooled
		2 K/kW	Single side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	6.52	1.55	1.67	0.49
τ_i (s)	0.4562	0.0792	0.0088	0.0037

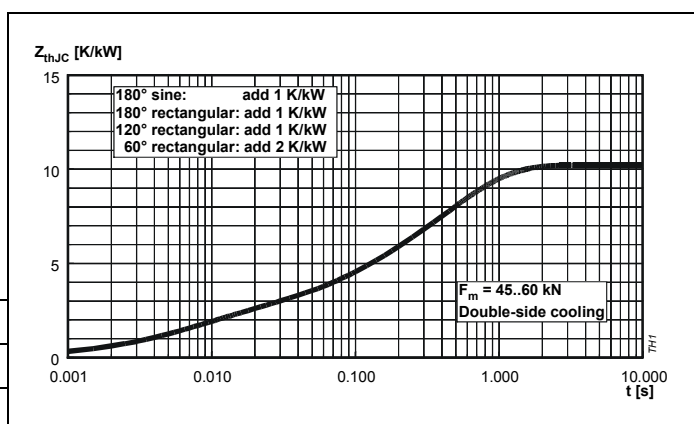


Fig. 1 Transient thermal impedance junction to case.

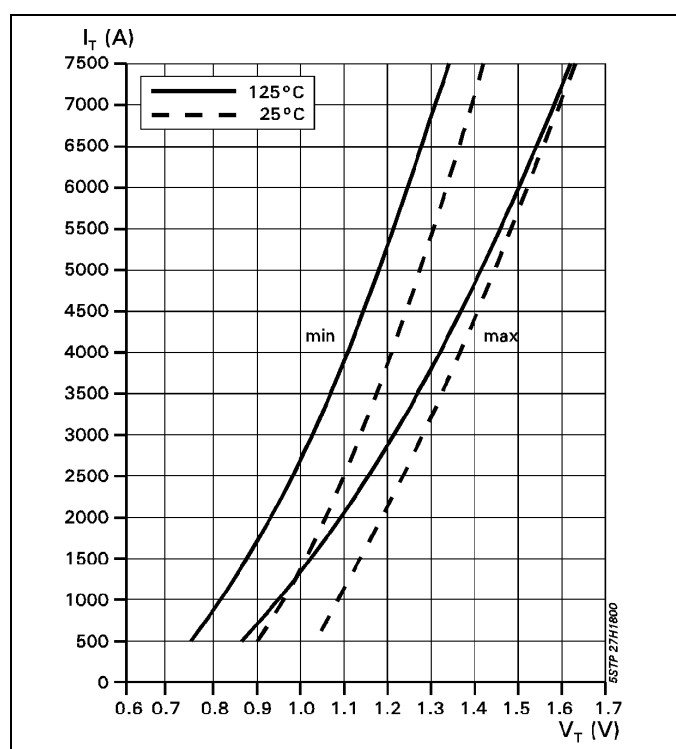


Fig. 2 On-state characteristics.
 $T_j=125^\circ\text{C}$, 10ms half sine

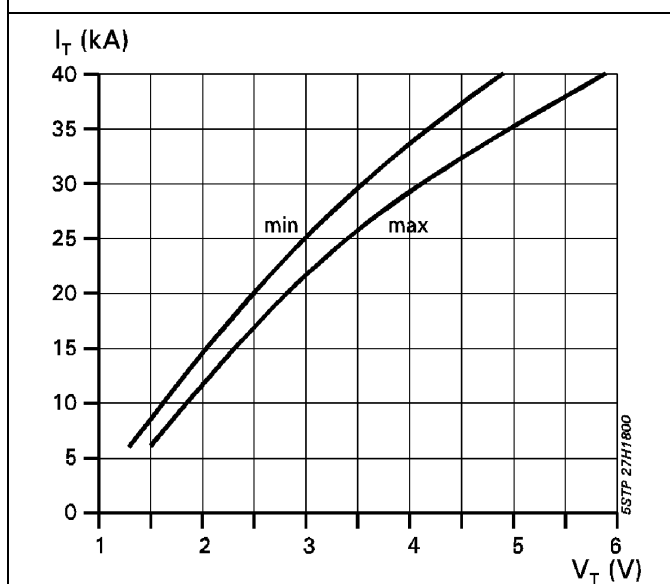


Fig. 3 On-state characteristics.

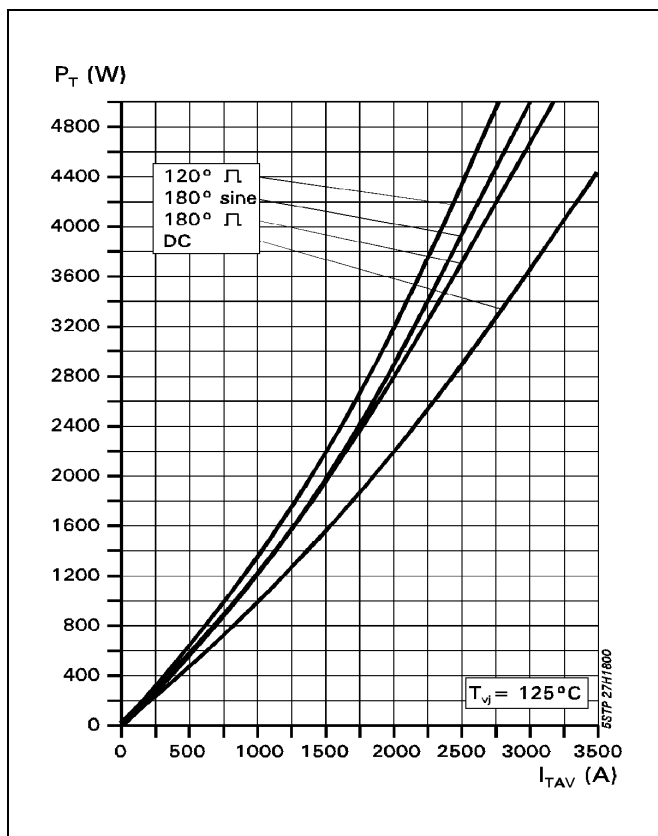


Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

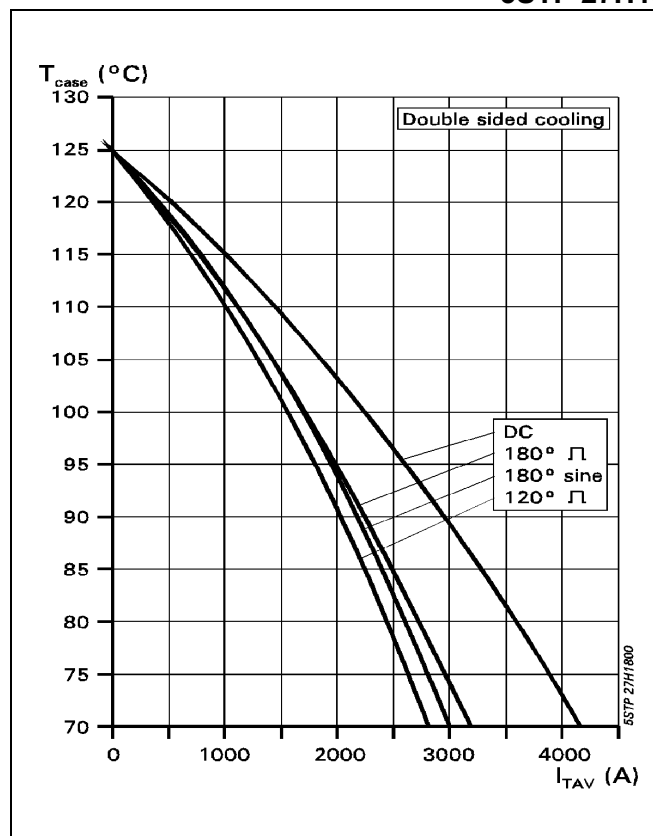


Fig. 5 Max. permissible case temperature vs. mean on-state current.

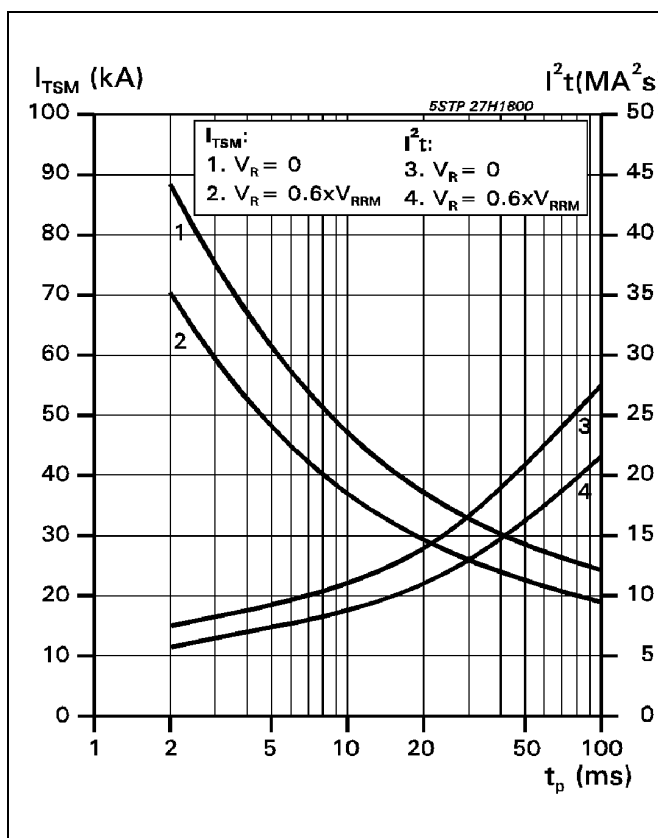


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

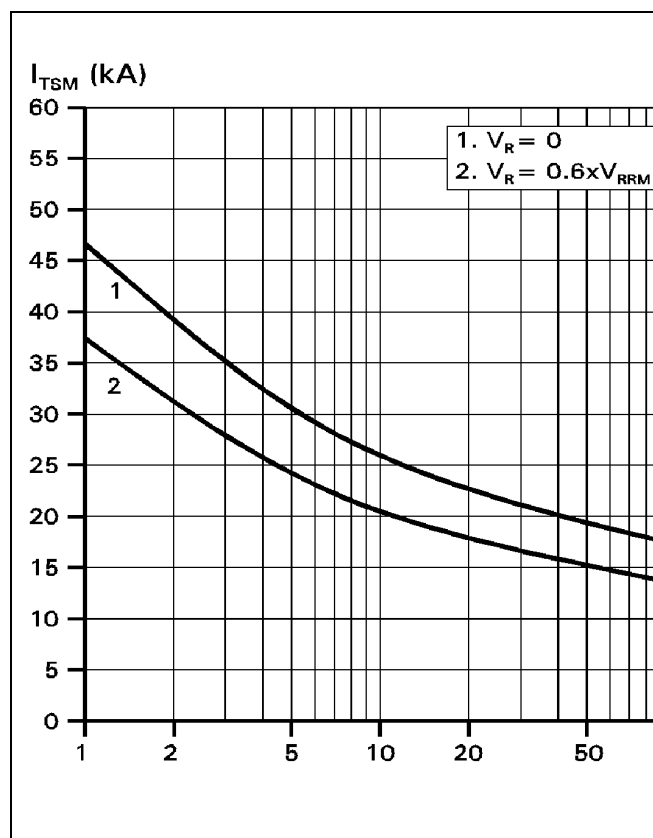


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

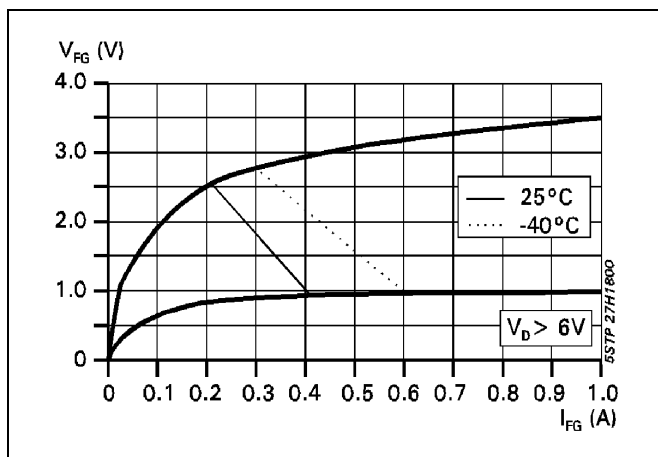


Fig. 8 Gate trigger characteristics.

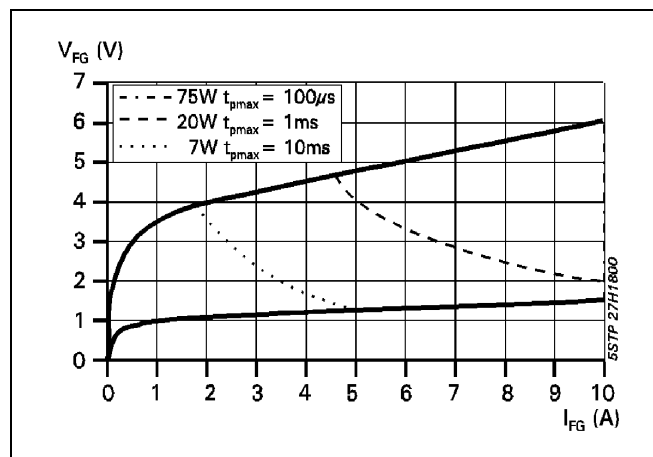


Fig. 9 Max. peak gate power loss.

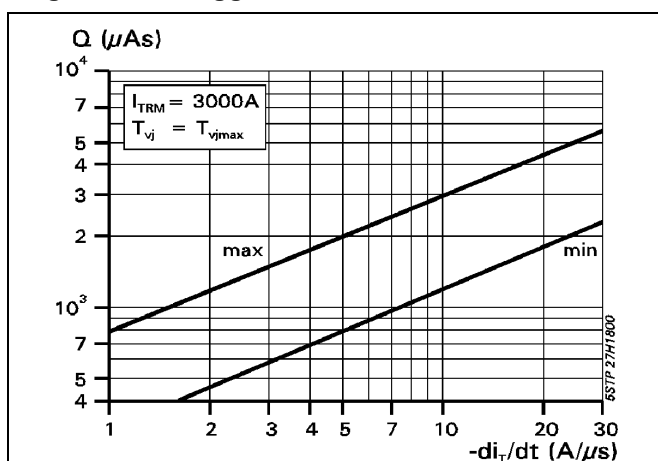


Fig. 10 Recovery charge vs. decay rate of on-state current.

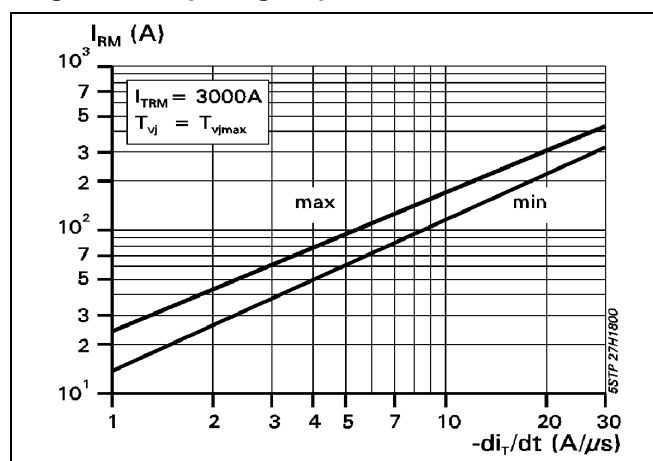


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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