V_{DSM}	=	1800 V
I_{TAVM}	=	325 A
I_{TRMS}	=	510 A
I_{TSM}	=	5000 A
V_{T0}	=	0.89 V
r_T	=	0.850 mΩ

Phase Control Thyristor

5STP 03A1800

Doc. No. 5SYA1032-01 Sep. 01

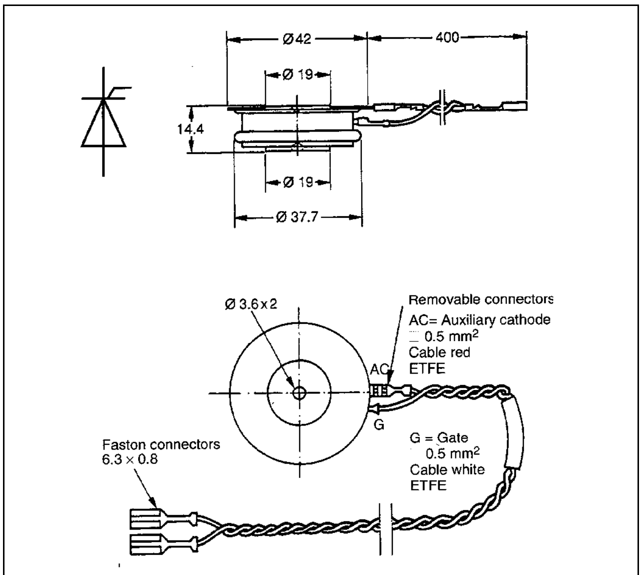
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**

Blocking

Part Number	**5STP 03A1800**	**5STP 03A1600**	**5STP 03A1200**	Conditions	
V_{DRM} V_{RRM}	1800 V	1600 V	1200 V	f = 50 Hz, t_p = 10ms	
V_{RSM1}	2000 V	1800 V	1400 V	t_p = 5ms, single pulse	
I_{DRM}	≤ 50 mA			V_{DRM}	T_j = 125°C
I_{RRM}	≤ 50 mA			V_{RRM}	
dV/dt_{crit}	1000 V/µs			Exp. to 0.67 x V_{DRM}, T_j = 125°C	

Mechanical data

F_M	Mounting force	nom.	4 kN
		min.	3.6 kN
		max.	4.8 kN
a	Acceleration Device unclamped Device clamped		 50 m/s² 100 m/s²
m	Weight		0.06 kg
D_S	Surface creepage distance		7 mm
D_a	Air strike distance		6 mm



On-state

I_{TAVM}	Max. average on-state current	325 A	Half sine wave, T_C = 70°C	
I_{TRMS}	Max. RMS on-state current	510 A		
I_{TSM}	Max. peak non-repetitive	5000 A	tp = 10 ms	T_j = 125°C
	surge current	5400 A	tp = 8.3 ms	After surge:
I^2t	Limiting load integral	125 kA^2s	tp = 10 ms	$V_D = V_R$ = 0V
		121 kA^2s	tp = 8.3 ms	
V_T	On-state voltage	1.40 V	I_T = 600 A	
V_{T0}	Threshold voltage	0.89 V	I_T = 200 - 600 A	T_j = 125°C
r_T	Slope resistance	0.850 mΩ		
I_H	Holding current	20-70 mA	T_j = 25°C	
		15-60 mA	T_j = 125°C	
I_L	Latching current	50-300 mA	T_j = 25°C	
		30-275 mA	T_j = 125°C	

Switching

di/dt_{crit}	Critical rate of rise of on-state	150 A/µs	Cont. f = 50 Hz	$V_D \leq 0.67 \cdot V_{DRM}$, T_j = 125°C
	current	300 A/µs	60 sec. f = 50Hz	I_{TRM} = 600 A I_{FG} = 1.5 A, t_r = 0.5 µs
t_d	Delay time	≤ 3.0 µs	$V_D = 0.4 \cdot V_{DRM}$	I_{FG} = 1.5 A, t_r = 0.5 µs
t_q	Turn-off time	≤ 400 µs	$V_D \leq 0.67 \cdot V_{DRM}$ dv_D/dt = 20V/µs	I_{TRM} = 600 A, T_j = 125°C V_R > 200 V, di_T/dt = -20 A/µs
Q_{rr}	Recovery charge min	400 µAs		
	max	1100 µAs		

Triggering

V_{GT}	Gate trigger voltage	2.4 V	T_j = 25°
I_{GT}	Gate trigger current	250 mA	T_j = 25°
V_{GD}	Gate non-trigger voltage	0.3 V	V_D =0.4 x V_{DRM}
I_{GD}	Gate non-trigger current	10 mA	V_D = 0.4 x V_{DRM}
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Gate power loss	3 W	

Thermal

T_{jmax}	Max. operating junction temperature range	125 °C	
T_{stg}	Storage temperature range	-40…140 °C	
R_{thJC}	Thermal resistance junction to case	130 K/kW	Anode side cooled
		160 K/kW	Cathode side cooled
		90 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	80 K/kW	Single side cooled
		40 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i\left(1 - e^{-t/\tau_i}\right)$$

i	1	2	3	4
R_i(K/kW)	15.6	17.9	18.7	18.2
τ_i(s)	1.4191	0.181	0.1614	0.0941

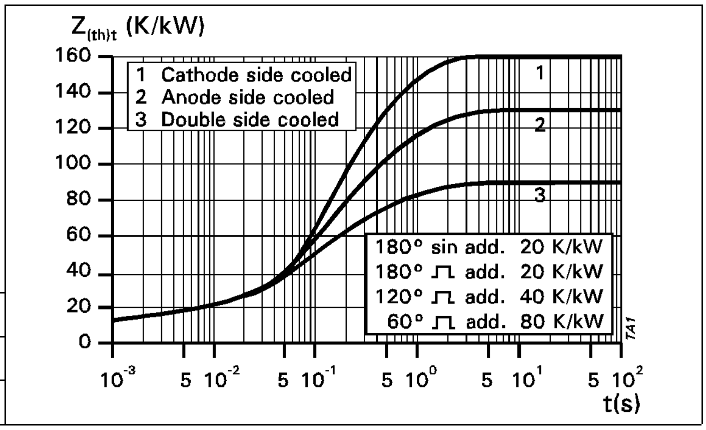


Fig. 1 Transient thermal impedance junction to case.

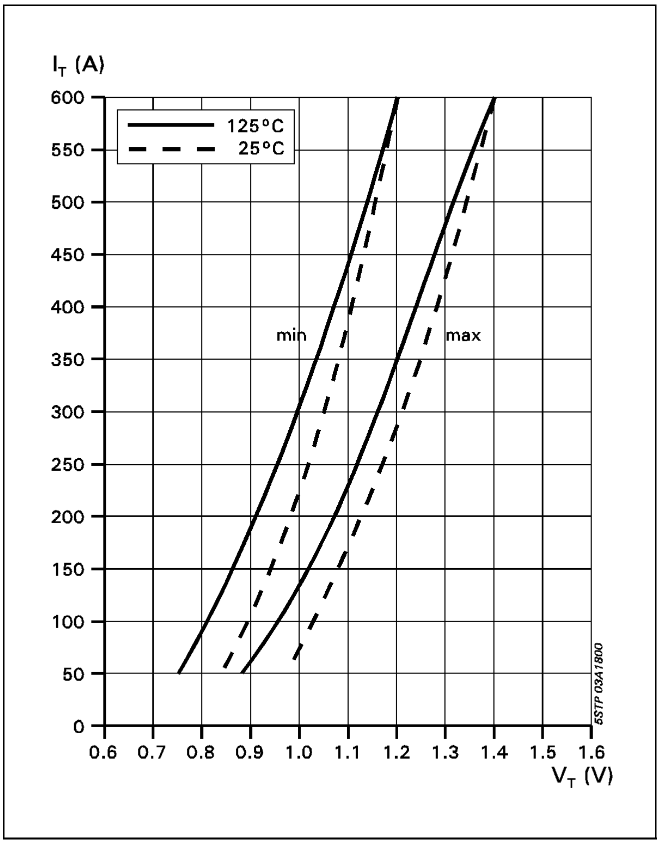


Fig. 2 On-state characteristics.

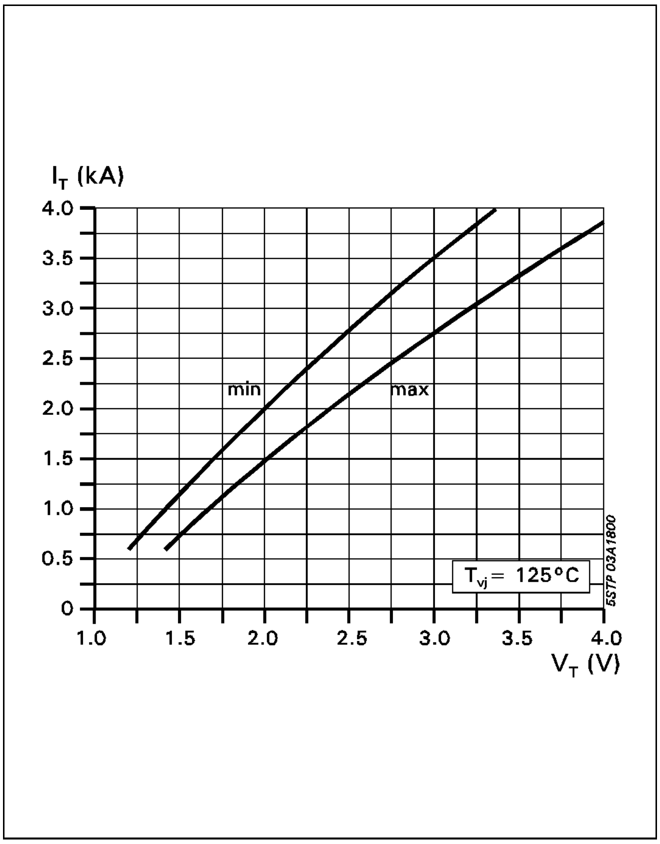


Fig. 3 On-state characteristics.
T_j=125°C, 10ms half sine

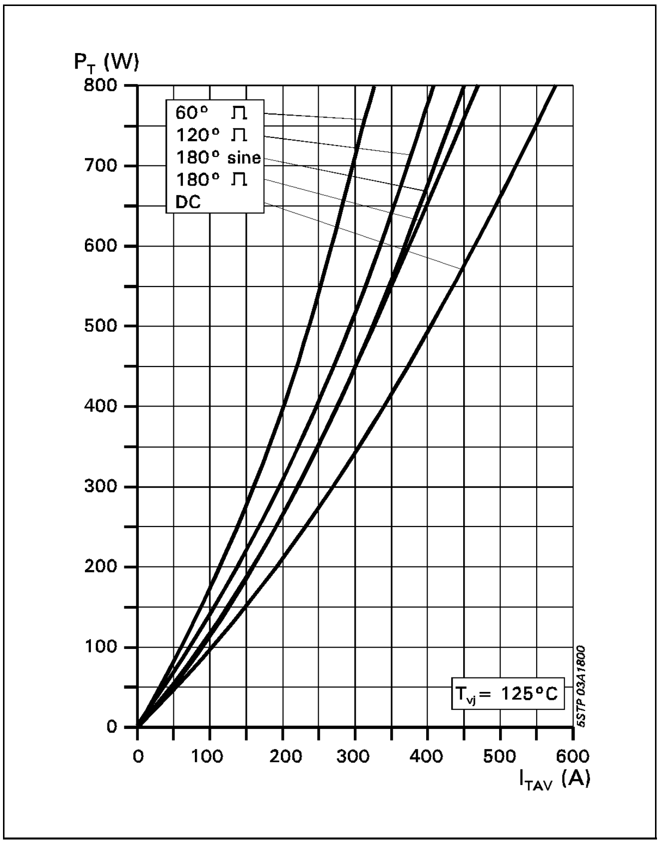


Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.

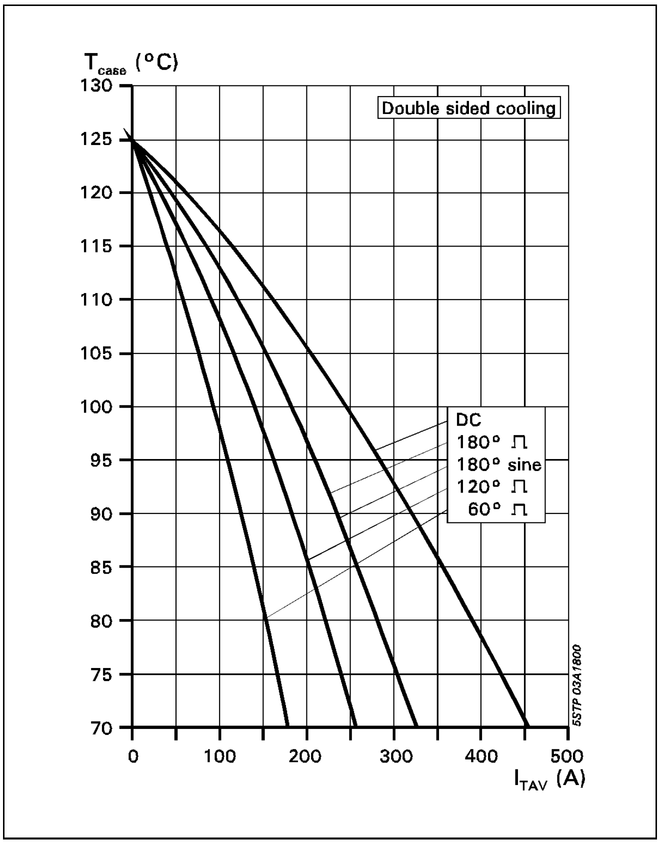


Fig. 5 Max. permissible case temperature vs. mean on-state current.

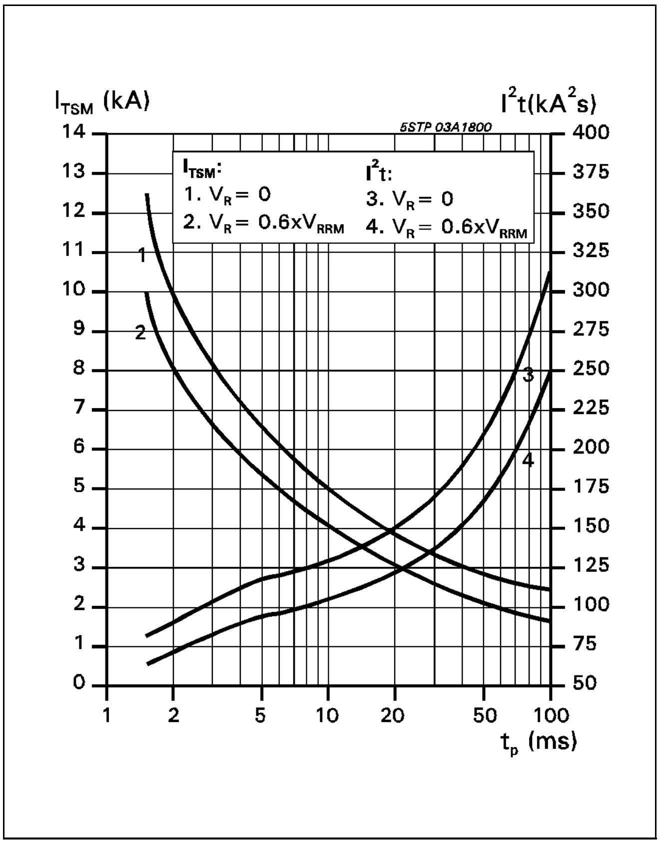


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

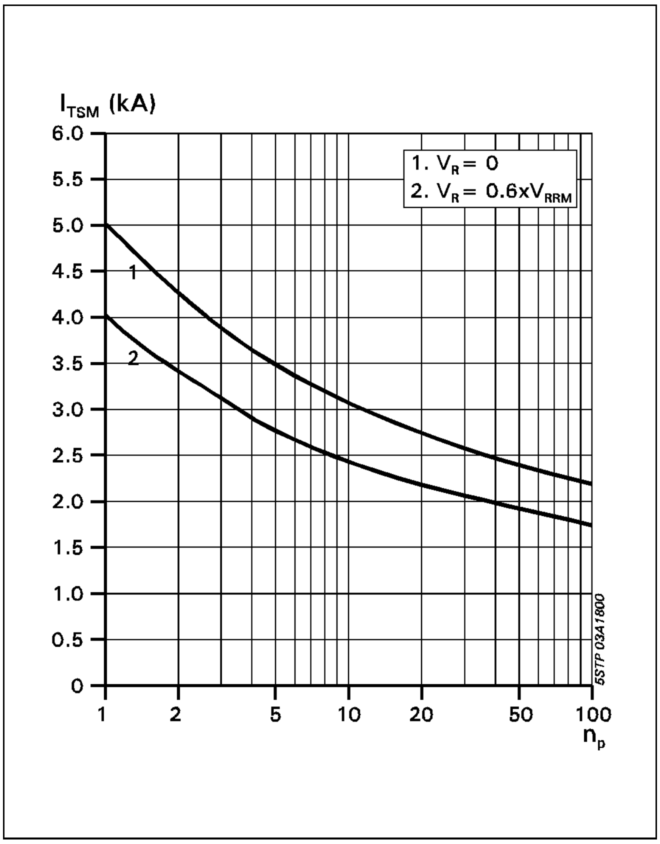


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

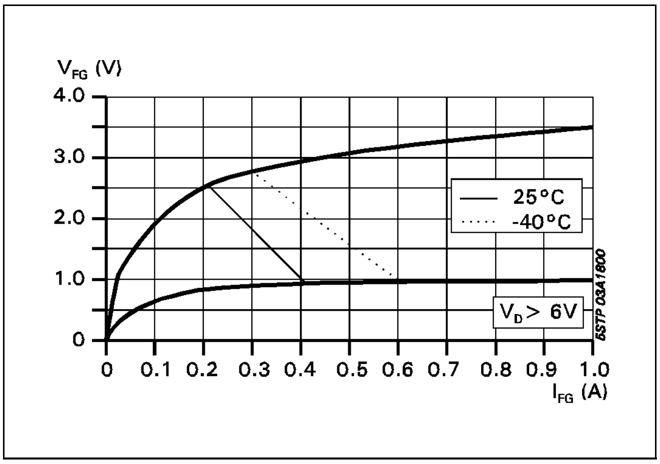


Fig. 8 Gate trigger characteristics.

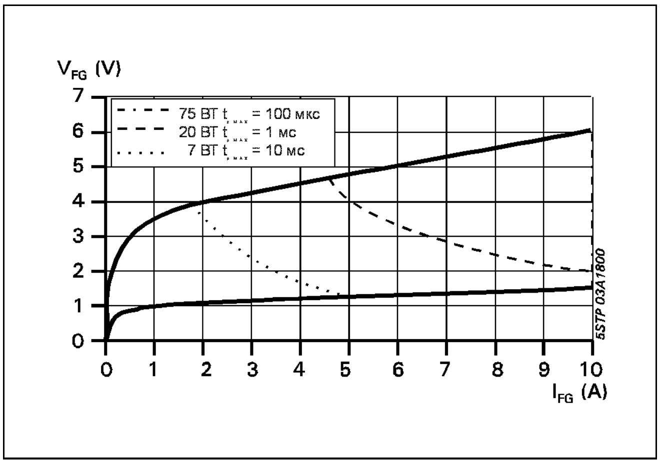


Fig. 9 Max. peak gate power loss.

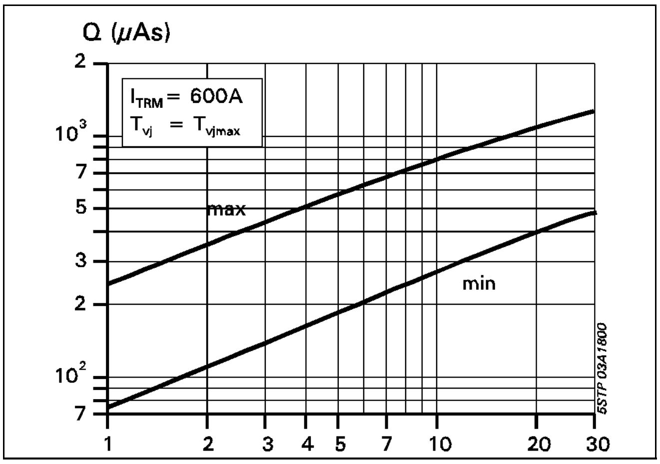


Fig. 10 Recovery charge vs. decay rate of on-state current.

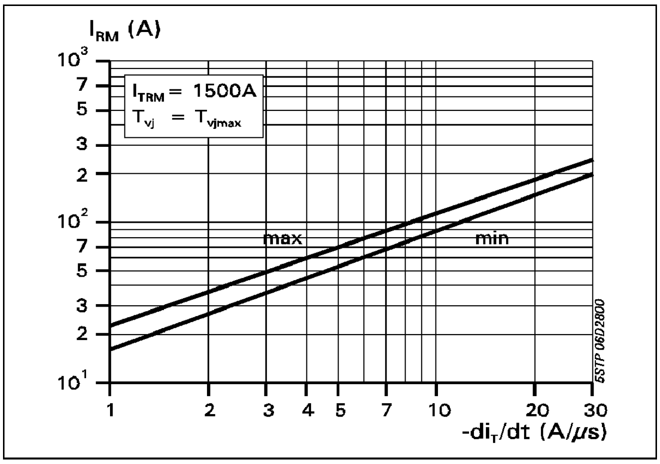


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

ABB Semiconductors AG reserves the right to change specifications without notice.

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