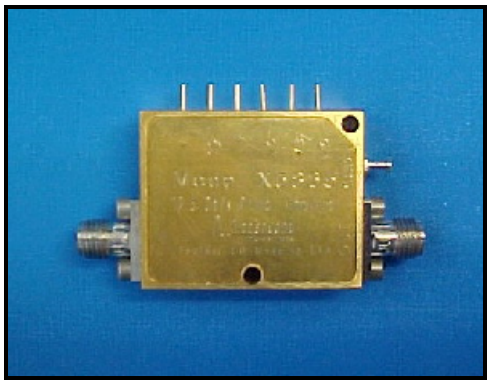
Model 5865

12.5 Gb/s Driver Amplifier

Preliminary Information

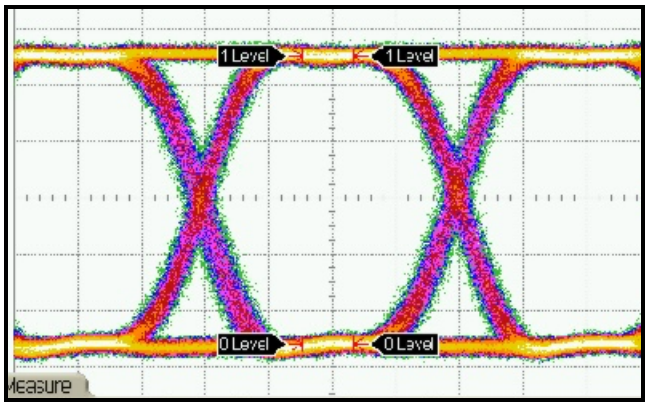
- **$LiNbO_3$ modulator driver amplifier (7.0 Vp-p output)**
- **High gain with low power dissipation (2 watts)**
- **Temperature compensated design for output stability**
- **Includes EOM bias network, crossing point control & adjustable output voltage**



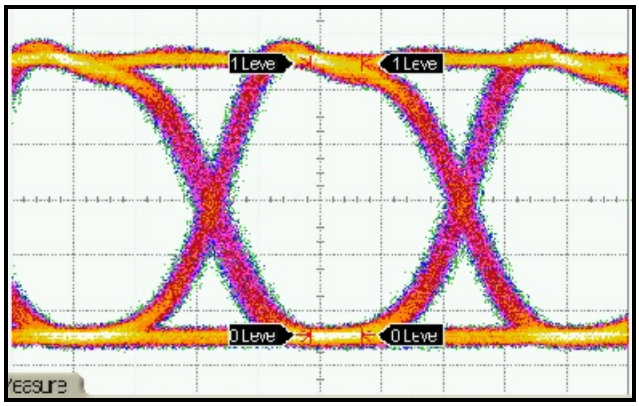
The Picosecond Pulse Labs Model 5865 is a driver amplifier intended for use driving $LiNbO_3$ modulators at data rates up to 12.5 Gb/s. Driven by only 500 mV of input signal, this amplifier produces excellent, wide-open eye patterns with 7 V of amplitude. The 5865 covers a broad band of frequencies from 22 kHz to 13.5 GHz and has very flat frequency and time domain responses.

The 5865 includes internal temperature compensation for excellent gain stability over temperature and exhibits both high gain and low power dissipation. It also incorporates internal sequencing circuitry, making it insensitive to power supply application sequence.

Typical 12.5 Gb/s Eye Measurements



Input Test Signal
513mV eye amplitude (100 mV/div, 20 ps/div)



Output Response
7.4 V eye amplitude (1.5 V/div, 20 ps/div)

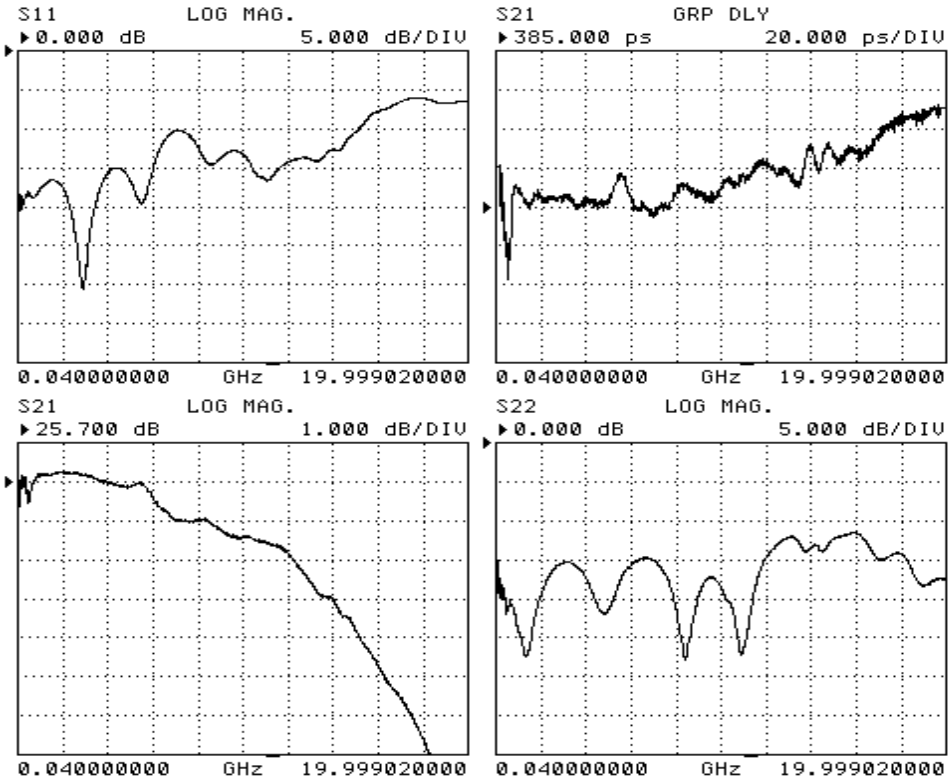
The 5865 is currently in the prototype stage of development. The information stated here is preliminary but typical of measurements made in the PSPL laboratories. This information is subject to change.

5865 Preliminary Specifications

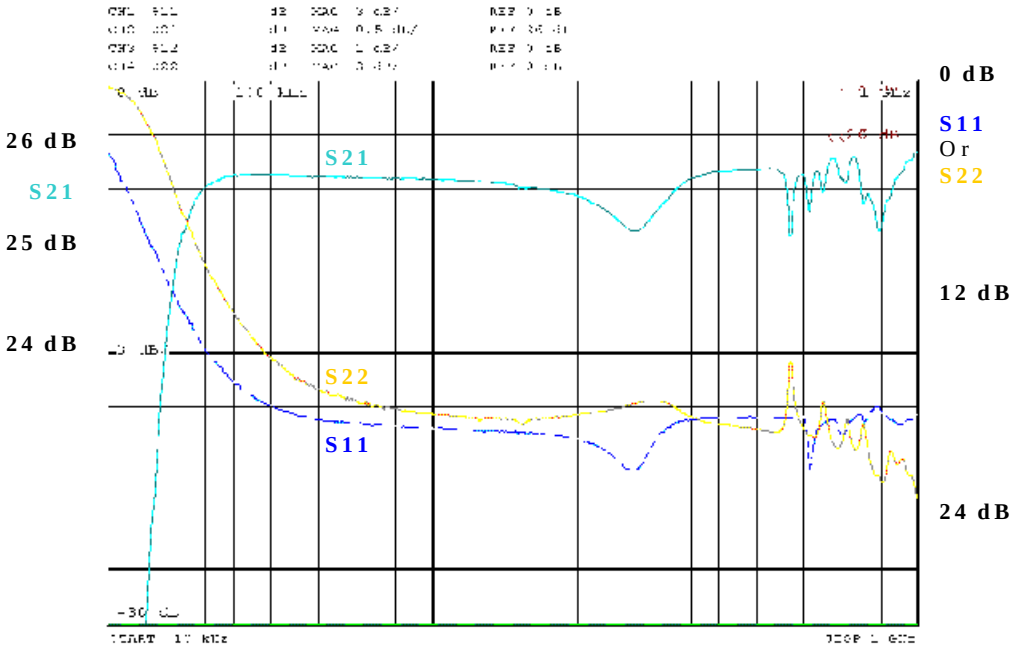
PARAMETER	SYMBOL	UNITS	MIN	TYPICAL	MAX	TEST CONDITIONS
Polarity						Non-inverting
Gain		dB	24	26		V_{gc} = 0 V
Output Saturation Voltage	$V_{SAT,OUT}$	V		7		0.65 V_{p-p} Input
Output Saturation Voltage Adjustment Range		V_{p-p}		7 to < 3		V_{SAT} dc control voltage from 0 V to –10 V, V_{IN} = 500 mV
1dB Output Compression Voltage	$V_{1dB,OUT}$	V_{p-p}		5.75		0.35 V_{p-p} Input, 12.5 Gb/s PRBS
Risetime	t_r	ps		29		10% to 90%, V_{in} = 500 mV, saturated output
RMS Total Jitter (Including Pattern Dependency)		ps		2		0.66 V_{p-p} Input, 12.5 Gb/s PRBS
V_{P-P} Variation from 0 to 70C		%		± 3		V_{gc} = 0 V, V_{p-p} in = 0.5 V 12.5 GHz PRBS
Crossing Point Adjust		%		±5		±5 V input at adjustment pin
Crossing Point Variation		%		±2.5		0.5 V_{p-p} Input, 12.5 Gb/s PRBS, 0 to 70°C, $0 \le V_{gc} \le -10$ V
Overshoot / Undershoot		%		5		12.5 Gb/s PRBS
High Frequency range (-3 dB)	f_{HIGH}	GHz	12.5	13.5		Small Signal
Low Frequency range (-3 dB)	f_{LOW}	kHz		22		Small Signal
Gain Ripple		dB		± 1.0		
Group Delay Variation		ps_{p-p}		± 20		f≤10 GHz
Input Return Loss freq < 5 GHz 5 GHz ≤ freq < 12 GHz	S_{11}	dB	 -12 -8	 -15 -10		
Output return loss freq < 12 GHz	S_{22}	dB	-12	-15		
Noise Figure	NF	dB		6		1 GHz
Effective Input Noise Voltage		µV RMS		110		
Maximum allowed Input		V_{p-p}			1.0	Damage threshold for input
DC Voltage Supply (pos)	$+V_{DC}$	V_{DC}	8	8	8.25	230 mA typical
DC Voltage Supply (neg)	$-V_{DC}$	V_{DC}	-5.25		-4.75	20 mA typical
Output Voltage Bias	V_{bias}	V_{DC}	-12		12	2 kΩ resistor (zero current)
Operating Temperature	T_{CASE}	°C	0		70	Case Temperature
Dimensions	1.25” x 1.0” x 0.375”					
RF Connectors	SMA Jack input / Jack output is Standard. Optional: SMA Plug					

All data taken after the unit achieved thermal equilibrium

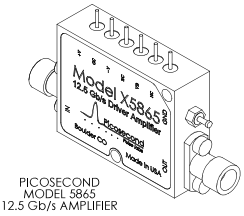
Typical 40 MHz - 20 GHz Frequency Response

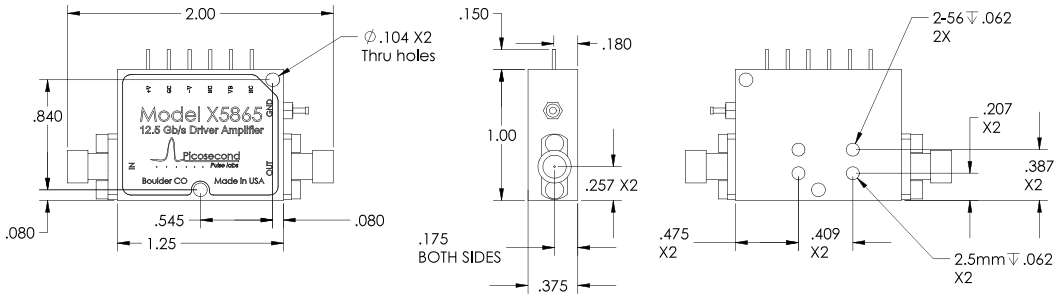


Typical 10 kHz – 1 GHz Frequency Response



5865 Mechanical Dimensions





5865 Pin Out

V_{out} CTRL = V_{out} control pin
CP_{adj} = crossing point adjust pin
VB_{EOM} = EOM bias pin