1066 MHz RDRAM®

Advance Information

512/576 Mb (8Mx16/18x4i)

Overview

The 1066 MHz Rambus DRAM (RDRAM®) is a general purpose high-performance memory device suitable for use in a broad range of applications including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The 512/576 Mb RDRAM devices are extremely high-speed CMOS DRAMs organized as 32M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600 MHz to 1066 MHz transfer rates while using conventional system and board design technologies. 1066 MHz RDRAM devices are capable of sustained data transfers at 0.9375 ns per two bytes (7.5 ns per sixteen bytes).

The architecture of RDRAM devices allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM devices four banks support up to four simultaneous transactions.

System-oriented features for mobile, graphics and large memory systems include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth or for error correction.

Features

- Highest sustained bandwidth per DRAM device
  - 2.1 GB/s sustained data transfer rate
  - Separate control and data buses for maximized efficiency
  - Separate row and column control buses for easy scheduling and highest performance
  - 4 banks: four transactions can take place simultaneously at full bandwidth data rates
- Low latency features
  - Write buffer to reduce read latency
  - 3 precharge mechanisms for controller flexibility
  - Interleaved transactions
- Advanced power management:
  - Multiple low power states allows flexibility in power consumption versus time to transition to active state
  - Power-down self-refresh
- Organization: 2 Kb pages and 4 banks, x 16/18
  - x18 organization allows ECC configurations or increased storage/bandwidth
  - x16 organization for low cost applications
- Uses Rambus Signaling Level (RSL) for up to 1066 MHz operation

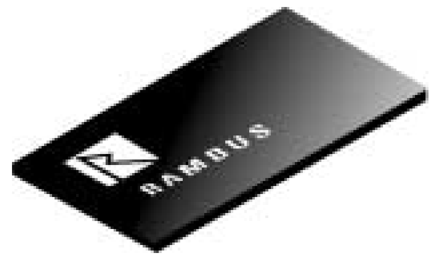


Figure 1: 1066 MHz RDRAM® CSP Package

The 512/576 Mb RDRAM devices are offered in a CSP horizontal package suitable for desktop as well as low-profile add-in card and mobile applications.

Key Timing Parameters/Part Numbers

Organization[a]	I/O Freq. MHz	Core Access Time (ns)	Part Number
8Mx16x4i	600	53	512Mi-53-600
8Mx16x4i	800	45	512Mi-45-800
8Mx16x4i	800	40	512Mi-40-800
8Mx16x4i	1066	35	512Mi-35-1066
8Mx18x4i	600	53	576Mi-53-600
8Mx18x4i	800	45	576Mi-45-800
8Mx18x4i	800	40	576Mi-40-800
8Mx18x4i	1066	35	576Mi-35-1066

a. The bank designations are described in a later section. Refer to Section "Row and Column Cycle Description" on page 17.
4i - 4 banks which use an "independent" bank architecture.
"1.8V" appended to the part number indicates the VDD supply voltage.

Related Documentation

Data sheets for the Rambus memory system components are available on the Rambus website at **www.rambus.com**. Please obtain the "Documentation Change History"for this datasheet. The DCH is an integral part of the data sheet and contains the most recent information about changes made to the published version. Check the Rambus website regularly for the latest DCH and data sheet updates.

Pinouts and Definitions

Center-Bonded Devices - Preliminary

This table shows the pin assignments of the center-bonded RDRAM package. The mechanical dimensions of this package are shown in a later section. Refer to Section "Center-Bonded uBGA Package (9x8 OPTIONAL)" on page 65.

Table 1: Center Bonded Device (top view)

10		VDD	GND		VDD	GND	VDD					VDD	VDD	VDD		GND	VDD	
9																		
8	GND	VDD	CMD	VDD	GND	GNDa	GNDa	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VCMOS	VDD	GND
7	VDD	DQA8	DQA7	DQA5	DQA3	DQA1	$\overline{CTM}$	CTM	ROW2	ROW0	COL3	COL1	DQB1	DQB3	DQB5	DQB7	DQB8	VDD
6																		
5																		
4	GND	GND	DQA6	DQA4	DQA2	DQA0	CFM	$\overline{CFM}$	ROW1	COL4	COL2	COL0	DQB0	DQB2	DQB4	DQB6	GND	GND
3	VDD	GND	SCK	VCMOS	GND	VDD	GND	VDDa	VREF	GND	VDD	GND	GND	VDD	SIO0	SIO1	GND	VDD
2																		
1		VDD	GND		GND	VDD	GND					GND	GND	GND		GND	VDD	
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**	**K**	**L**	**M**	**N**	**P**	**R**	**S**	**T**	**U**

Note the following:

- This is the “Top View” (balls facing down, backside of chip facing up).
- Pin #1 designation is at location A1.
- Columns “A” and “U”, and Rows “1” and “10” can be deleted when die size shrink to the point that those balls will not fall within the die boundaries.
- For 32Mx8 devices either DQA8 & DQB8 must be defined as no connects or columns “B” and “T” must be deleted completely.

Table 2: Pin Description

Signal	I/O	Type	# Pins edge	# Pins center	Description
SIO1,SIO0	I/O	CMOS[a]	2	2	Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
CMD	I	CMOS[a]	1	1	Command input. Pins used in conjunction with SIO0 and SIO1 for reading from and writing to the control registers. Also used for power management.
SCK	I	CMOS[a]	1	1	Serial clock input. Clock source used for reading from and writing to the control registers
V_{DD}			14	6	Supply voltage for the RDRAM core and interface logic.
V_{DDa}			2	1	Supply voltage for the RDRAM analog circuitry.
V_{CMOS}			2	2	Supply voltage for CMOS input/output pins.
GND			19	9	Ground reference for RDRAM core and interface.
GNDa			2	1	Ground reference for RDRAM analog circuitry.
DQA8..DQA0	I/O	RSL[b]	9	9	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM device. DQA8 is not used by RDRAM devices with a x16 organization.
CFM	I	RSL[b]	1	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	I	RSL[b]	1	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity
V_{REF}			1	1	Logic threshold reference voltage for RSL signals
CTMN	I	RSL[b]	1	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	I	RSL[b]	1	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RQ7..RQ5 or ROW2..ROW0	I	RSL[b]	3	3	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL[b]	5	5	Column access control. Five pins containing control and address information for column accesses.
DQB8.. DQB0	I/O	RSL[b]	9	9	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM device. DQB8 is not used by RDRAM devices with a x16 organization.
Total pin count per package			74	54	

a. All CMOS signals are high-true; a high voltage is a logic one and a low voltage is logic zero.
b. All RSL signals are low-true; a low voltage is a logic one and a high voltage is logic zero.

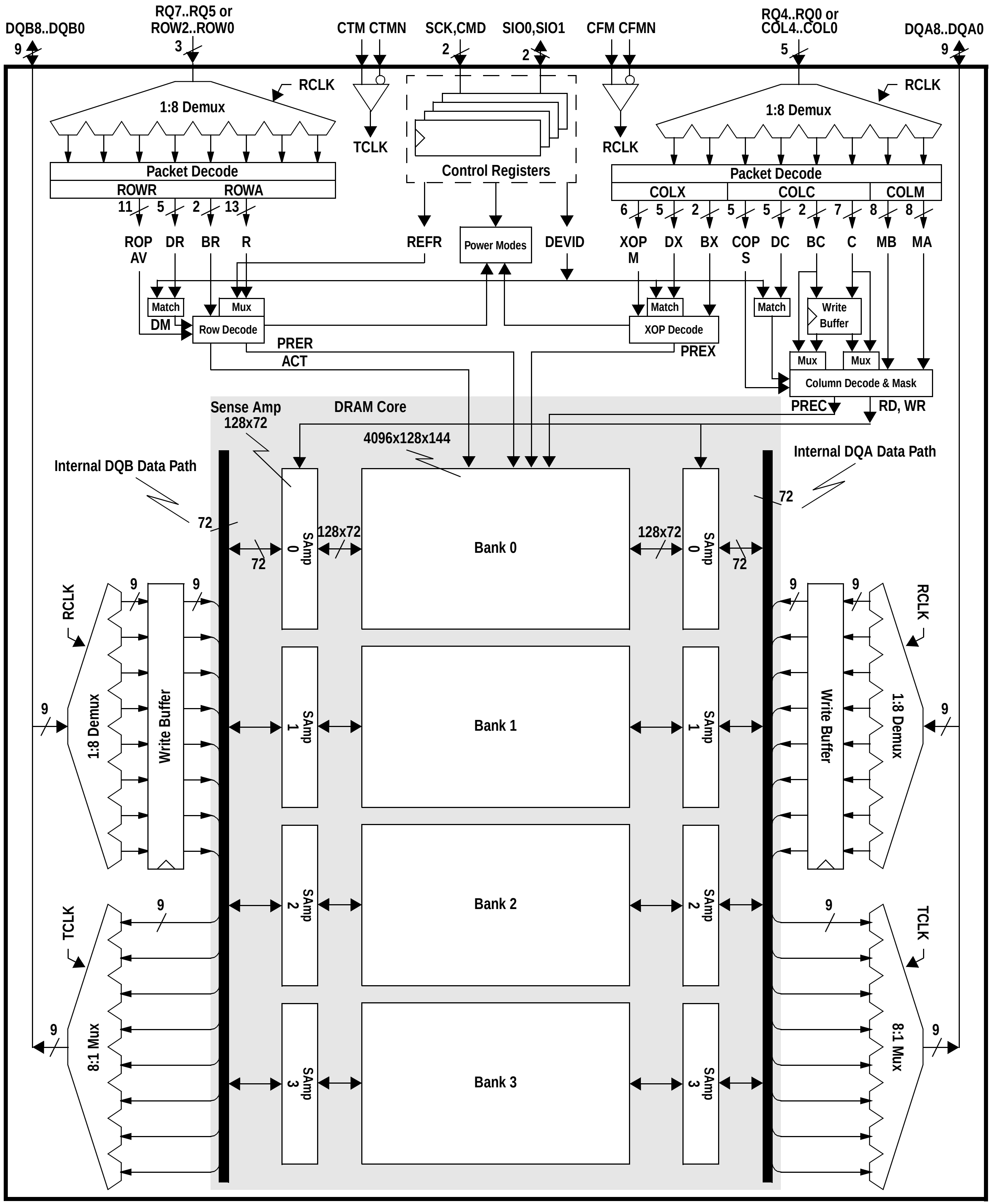


Figure 2: 512/576 Mb ((8Mx16/18x4i)) RDRAM Block Diagram

General Description

Figure 2 is a block diagram of the 512 / 576 Mb Direct RDRAM device. It consists of two major blocks: a “core” block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus interface block which permits an external controller to access this core at up to 1.6 GB / s.

Control Registers: The CMD, SCK, SIO0, and SIO1 pins appear in the upper center of Figure 2. They are used to write and read a block of control registers. These registers supply the RDRAM configuration information to a controller and they select the operating modes of the device. The REFR value is used for tracking the last refreshed row. Most importantly, the five bit DEVID specifies the device address of the RDRAM device on the Channel.

Clocking: The CTM and CTMN pins (Clock-To-Master) generate TCLK (Transmit Clock), the internal clock used to transmit read data. The CFM and CFMN pins (Clock-From-Master) generate RCLK (Receive Clock), the internal clock signal used to receive write data and to receive the ROW and COL pins.

DQA,DQB Pins: These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed / de-multiplexed from / to two 72-bit data paths (running at one-eighth the data frequency) inside the RDRAM device.

Banks: The 64Mbyte core of the RDRAM device is divided into 4 16.0Mbyte banks, each organized as 8192 rows, with each row containing 128 dualocts, and each dualoct containing 16 bytes. A dualoct is the smallest unit of data that can be addressed.

Sense Amps: The RDRAM device contains 4 sense amps. Each sense amp consists of 2kbyte of fast storage (1kbyte for DQA and 1kbyte for DQB) and can hold one row of one bank of the RDRAM device. The sense amp may hold any of the 8192 rows of an associated bank.

RQ Pins: These pins carry control and address information. They are broken into two groups. RQ7..RQ5 are also called ROW2..ROW0, and are used primarily for controlling row accesses. RQ4..RQ0 are also called COL4..COL0, and are used primarily for controlling column accesses.

ROW Pins: The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM device. These pins are de-multiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins: The principle use of these five pins is to manage the transfer of data between the DQA / DQB pins and the sense amps of the RDRAM device. These pins are de-multiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17-bit COLX (extended-operation) packet.

ACT Command: An ACT (activate) command from an ROWA packet causes one of the 8192 rows of the selected bank to be loaded to its associated sense amps (one 1kbyte sense amp for DQA and one for DQB).

PRER Command: A PRER (precharge) command from an ROWR packet causes the selected bank to release its associated sense amp, permitting a different row in that bank to be activated.

RD Command: The RD (read) command causes one of the 128 dualocts of one of the sense amps to be transmitted on the DQA / DQB pins of the Channel.

WR Command: The WR (write) command causes a dualoct received from the DQA / DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional bytemask) to one of the 128 dualocts of one of the sense amps during a subsequent COP command. A retire can take place during a RD, WR, or NOCOP to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD to the same device. The write buffer reduces the delay needed for the internal DQA / DQB data path turn-around.

PREC Precharge: The PREC, RDA and WRA commands are similar to NOCOP, RD and WR, except that a precharge operation is performed at the end of the column operation. These commands provide a second mechanism for performing precharge.

PREX Precharge: After a RD command, or after a WR command with no byte masking (M=0), a COLX packet may be used to specify an extended operation (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

Packet Format

Figure 3 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 3 describes the fields which comprise these packets. DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM device.

The AV (ROWA / ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packet provide a 5-bit device address and a 2-bit bank address. An ROWA packet uses the remaining bits to specify a 13-bit row address, and the ROWR packet uses the remaining bits for an 11-bit opcode field. Note the use of the “RsvX” notation to reserve bits for future address field extension.

Table 3: Field Description for ROWA Packet and ROWR Packet

Field	Description
DR4T,DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR4..DR0	Device address for ROWA or ROWR packet.
BR1..BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits ignored by the RDRAM device.
AV	Selects between ROWA packet (AV=1) and ROWR packet (AV=0).
R12..R0	Row address for ROWA packet. RsvR denotes bits ignored by the RDRAM device.
ROP10..ROP0	Opcode field for ROWR packet. Specifies precharge, refresh, and power management functions.

Figure 3 also shows the formats of the COLC, COLM, and COLX packets on the COL pins. Table 4 describes the fields which comprise these packets.

The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23-bit COLC packet has a 5-bit device address, a 2-bit bank address, a 7-bit column address, and a 4-bit opcode. The COLC packet specifies a read or write command, as well as some power management commands.

The remaining 17 bits are interpreted as a COLM (M=1) or COLX (M=0) packet. A COLM packet is used for a COLC write command which needs bytemask control. The COLM packet is associated with the COLC packet from at least t_{RTR} earlier. A COLX packet may be used to specify an independent precharge command. It contains a 5-bit device address, a 2-bit bank address, and a 5-bit opcode. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is framed within a COLC packet but is not otherwise associated with any other packet.

Table 4: Field Description for COLC Packet, COLM Packet, and COLX Packet

Field	Description
S	Bit for framing (recognizing) a COLC packet, and indirectly for framing COLM and COLX packets.
DC4..DC0	Device address for COLC packet.
BC1..BC0	Bank address for COLC packet. RsvB denotes bits reserved for future extension (controller drives 0’s).
C6..C0	Column address for COLC packet. RsvC denotes bits ignored by the RDRAM device.
COP3..COP0	Opcode field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Selects between COLM packet (M=1) and COLX packet (M=0).
MA7..MA0	Bytemask write control bits. 1=write, 0=no-write. MA0 controls the earliest byte on DQA8..0.
MB7..MB0	Bytemask write control bits. 1=write, 0=no-write. MB0 controls the earliest byte on DQB8..0.
DX4..DX0	Device address for COLX packet.
BX1..BX0	Bank address for COLX packet. RsvB denotes bits reserved for future extension (controller drives 0’s).
XOP4..XOP0	Opcode field for COLX packet. Specifies precharge, I_{OL} control, and power management functions.

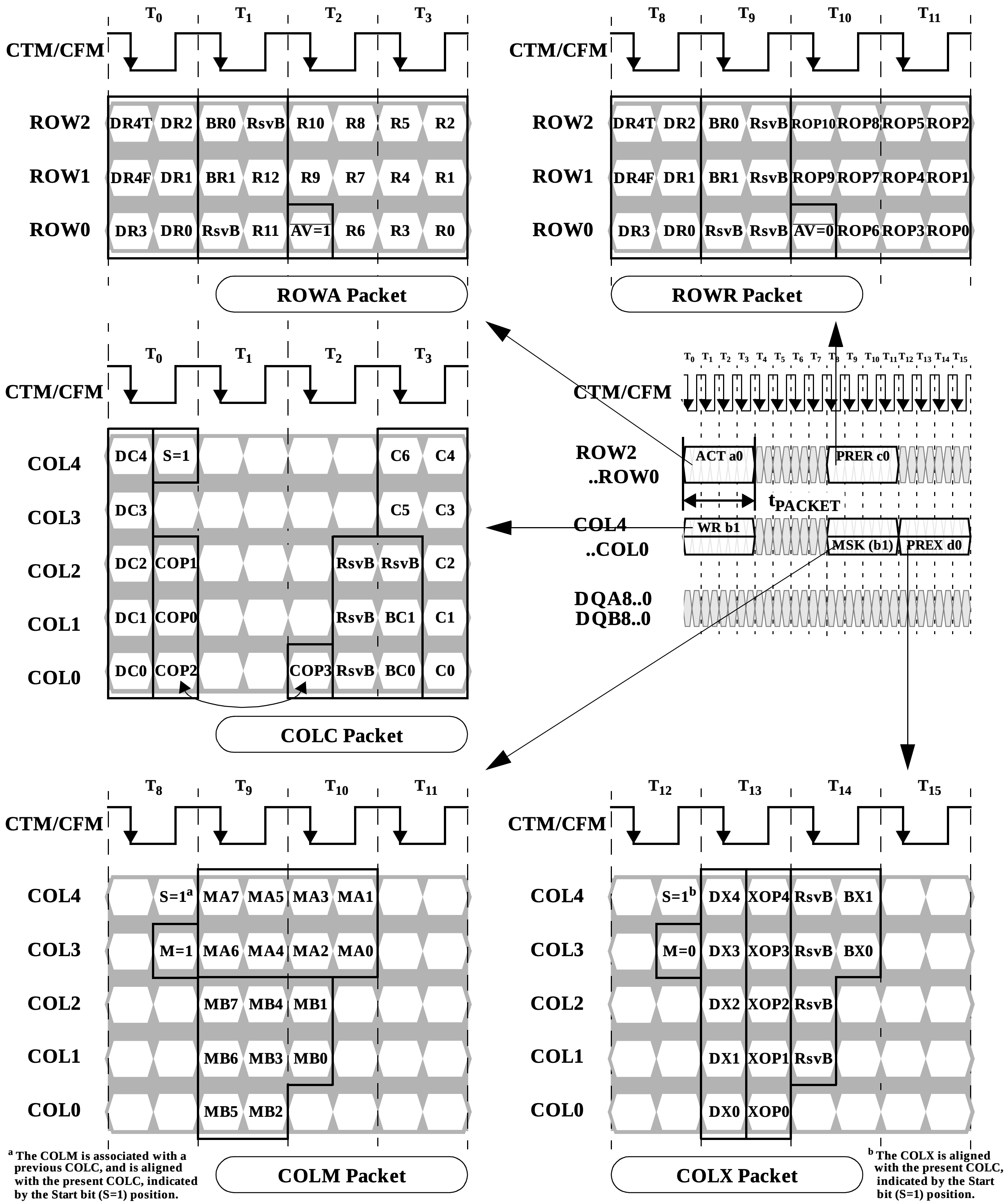


Figure 3: Packet Formats

Field Encoding Summary

Table 5 shows how the six device address bits are decoded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (DeviceMatch) signal is asserted and an ACT or ROP command is performed.

Table 5: Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Device Selection	Device Match signal (DM)
1	1	All devices (broadcast)	DM is set to 1
0	1	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {0,DR3..DR0} else DM is set to 0
1	0	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {1,DR3..DR0} else DM is set to 0
0	0	No packet present	DM is set to 0

Table 6 shows the encodings of the remaining fields of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device to be loaded into the associated sense amps.

An ROWR packet is specified when AV is not asserted. An 11-bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its associated sense amps to precharge, so another row may be activated. The REFA (refresh-activate) command is similar to the ACT command, except the row address comes from an internal register REFR, and REFR is incremented at the largest bank address. The REFP (refresh-precharge) command is identical to a PRER command.

The NAPR, NAPRC, PDNR, ATTN, and RLXR commands are used for managing the power dissipation of the RDRAM device and are described in more detail in “Power State Management” on page 38. The TCEN and TCAL commands are used to adjust the output driver slew rate and they are described in more detail in “Current and Temperature Control” on page 44.

Table 6: ROWA Packet and ROWR Packet Field Encodings

DM[a]	AV	ROP10..ROP0 Field									Name	Command Description
		10	9	8	7	6	5	4	3	2:0		
0	-	-	-	-	-	-	-	-	-	---	-	No operation.
1	1	Row address									ACT	Activate row R12..R0 of bank BR1..BR0 of device and move device to ATTN[b].
1	0	1	1	0	0	0	x[c]	x	x	000	PRER	Precharge bank BR1..BR0 of this device.
1	0	0	0	0	1	1	0	0	x	000	REFA	Refresh (activate) row REFR12..REFR0 of bank BR1..BR0 of device. Increment REFR if BR1..BR0 = 1..1 (see Figure 50).
1	0	1	0	1	0	1	0	0	x	000	REFP	Precharge bank BR1..BR0 of this device after REFA (see Figure 50).
1	0	x	x	0	0	0	0	1	x	000	PDNR	Move this device into the powerdown (PDN) power state (see Figure 47).
1	0	x	x	0	0	0	1	0	x	000	NAPR	Move this device into the nap (NAP) power state (see Figure 47).
1	0	x	x	0	0	0	1	1	x	000	NAPRC	Move this device into the nap (NAP) power state conditionally
1	0	x	x	x	x	x	x	x	0	000	ATTN[b]	Move this device into the attention (ATTN) power state (see Figure 45).
1	0	x	x	x	x	x	x	x	1	000	RLXR	Move this device into the standby (STBY) power state (see Figure 46).
1	0	0	0	0	0	0	0	0	x	001	TCAL	Temperature calibrate this device (see Figure 53).
1	0	0	0	0	0	0	0	0	x	010	TCEN	Temperature calibrate/enable this device (see Figure 53).
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

a. The DM (Device Match signal) value is determined by the DR4T,DR4F, DR3..DR0 field of the ROWA and ROWR packets. See Table 5.

b. The ATTN command does not cause a RLX-to-ATTN transition for a broadcast operation (DR4T / DR4F=1 / 1).
c. An "x" entry indicates which commands may be combined. For instance, the three commands PRER / NAPRC / RLXR may be specified in one ROP value (011000111000).

Table 7 shows the COP field encoding. The device must be in the ATTN power state in order to receive COLC packets. The COLC packet is used primarily to specify RD (read) and WR (write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See Figure 17 for a more detailed description.

The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA / WRA commands are equivalent to combining RD / WR with a PREC. RLXC (relax) performs a power mode transition. See "Power State Management" on page 38.

Table 7: COLC Packet Field Encodings

S	DC4.. DC0 (select device)[a]	COP3..0	Name	Command Description
0	----	-----	-	No operation.
1	/ = (DEVID4 ..0)	-----	-	Retire write buffer of this device.
1	== (DEVID4 ..0)	x000[b]	NOCOP	Retire write buffer of this device.
1	== (DEVID4 ..0)	x001	WR	Retire write buffer of this device, then write column C6..C0 of bank BC1..BC0 to write buffer.
1	== (DEVID4 ..0)	x010	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x011	RD	Read column C6..C0 of bank BC1..BC0 of this device.
1	== (DEVID4 ..0)	x100	PREC	Retire write buffer of this device, then precharge bank BC1..BC0 (see Figure 14).
1	== (DEVID4 ..0)	x101	WRA	Same as WR, but precharge bank BC1..BC0 after write buffer (with new data) is retired.
1	== (DEVID4 ..0)	x110	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x111	RDA	Same as RD, but precharge bank BC1..BC0 afterward.
1	== (DEVID4 ..0)	1xxx	RLXC	Move this device into the standby (STBY) power state (see Figure 46).

a. "/ =" means not equal, "==" means equal.
b. An "x" entry indicates which commands may be combined. For instance, the two commands WR / RLXC may be specified in one COP value (1001).

Table 8 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two 8-bit bytemask fields MA and MB. If the M bit is not asserted, a COLX is specified. It has device and bank address fields, and an opcode field. The primary use of the COLX packet is to permit an independent PREX (precharge) command to be specified without consuming control bandwidth on the ROW pins. It is also used for the CAL(calibrate) and SAM (sample) current control commands (see "Current and Temperature Control" on page 44), and for the RLXX power mode command (see "Power State Management" on page 38).

Table 8: COLM Packet and COLX Packet Field Encodings

M	DX4 .. DX0 (selects device)	XOP4..0	Name	Command Description
1	----	-	MSK	MB / MA bytemasks used by WR / WRA.
0	/ = (DEVID4 ..0)	-	-	No operation.
0	== (DEVID4 ..0)	00000	NOXOP	No operation.
0	== (DEVID4 ..0)	1xxx0[a]	PREX	Precharge bank BX1..BX0 of this device (see Figure 14).
0	== (DEVID4 ..0)	x10x0	CAL	Calibrate (drive) I_{OL} current for this device (see Figure 52).
0	== (DEVID4 ..0)	x11x0	CAL / SAM	Calibrate (drive) and Sample (update) I_{OL} current for this device (see Figure 52).
0	== (DEVID4 ..0)	xxx10	RLXX	Move this device into the standby (STBY) power state (see Figure 46).
0	== (DEVID4 ..0)	xxxx1	RSRV	Reserved, no operation.

a. An "x" entry indicates which commands may be combined. For instance, the two commands PREX / RLXX may be specified in one XOP value (10010).

DQ Packet Timing

Figure 4 shows the timing relationship of COLC packets with D and Q data packets. This document uses a specific convention for measuring time intervals between packets: all packets on the ROW and COL pins (ROWA, ROWR, COLC, COLM, COLX) use the trailing edge of the packet as a reference point, and all packets on the DQA / DQB pins (D and Q) use the leading edge of the packet as a reference point.

An RD or RDA command will transmit a dualoct of read data Q a time t_{CAC} later. This time includes one to five cycles of round-trip propagation delay on the Channel. The t_{CAC} parameter may be programmed to a one of a range of values (7, 8, 9, 10, 11, or 12 t_{CYCLE}). The value chosen depends upon the number of RDRAM devices on the Channel and the RDRAM timing bin. See Figure 39 for more information.

A WR or WRA command will receive a dualoct of write data D a time t_{CWD} later. This time does not need to include the round-trip propagation time of the Channel since the COLC and D packets are traveling in the same direction.

When a Q packet follows a D packet (shown in the left half of the figure), a gap (t_{CAC} -t_{CWD}) will automatically appear between them because the t_{CWD} value is always less than the t_{CAC} value. There will be no gap between the two COLC packets with the WR and RD commands which schedule the D and Q packets.

When a D packet follows a Q packet (shown in the right half of the figure), no gap is needed between them because the t_{CWD} value is less than the t_{CAC} value. However, a gap of t_{CAC} -t_{CWD} or greater must be inserted between the COLC packets with the RD WR commands by the controller so the Q and D packets do not overlap.

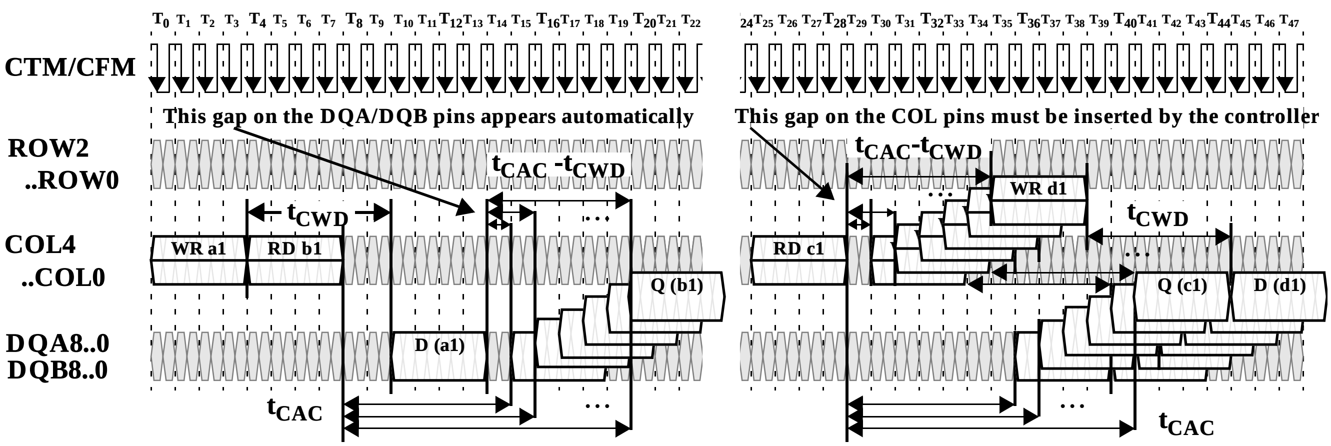


Figure 4: Read (Q) and Write (D) Data Packet - Timing for t_{CAC} = 7, 8, 9, 10, 11, or 12 t_{CYCLE}

COLM Packet to D Packet Mapping

Figure 5 shows a write operation initiated by a WR command in a COLC packet. If a subset of the 16 bytes of write data are to be written, then a COLM packet is transmitted on the COL pins a time t_{RTR} after the COLC packet containing the WR command. The M bit of the COLM packet is set to indicate that it contains the MA and MB mask fields. Note that this COLM packet is aligned with the COLC packet which causes the write buffer to be retired. See Figure 17 for more details.

If all 16 bytes of the D data packet are to be written, then no further control information is required. The packet slot that would have been used by the COLM packet (t_{RTR} after the COLC packet) is available to be used as an COLX packet. This could be used for a PREX precharge command or for a housekeeping command (this case is not shown). The M bit is not asserted in an COLX packet and causes all 16 bytes of the previous WR to be written unconditionally. Note that a RD command will never need a COLM packet, and will always be able to use the COLX packet option (a read operation has no need for the byte-write-enable control bits).

Figure 5 also shows the mapping between the MA and MB fields of the COLM packet and bytes of the D packet on the DQA and DQB pins. Each mask bit controls whether a byte of data is written (=1) or not written (=0).

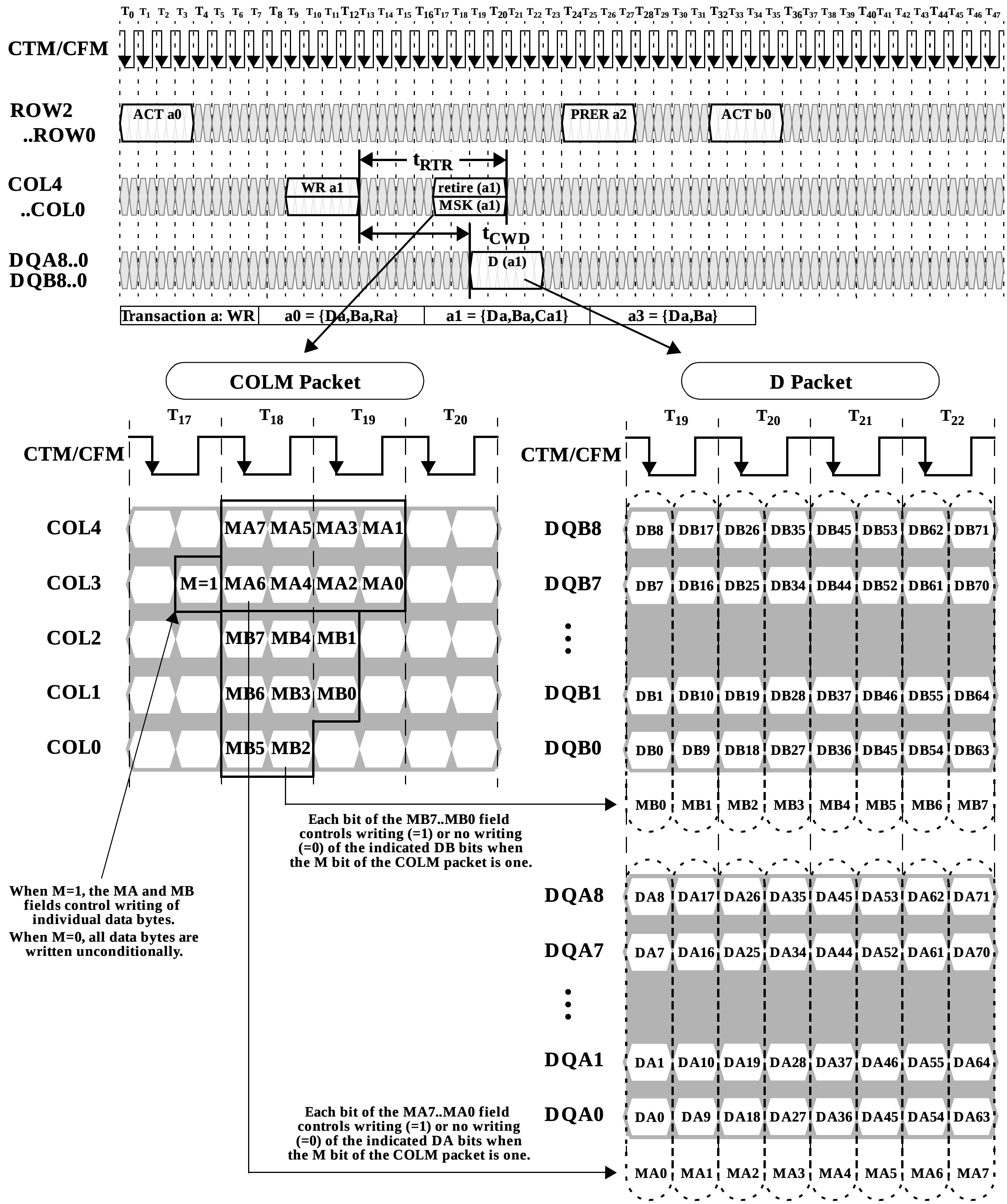


Figure 5: Mapping Between COLM Packet and D Packet for WR Command

ROW-to-ROW Packet Interaction

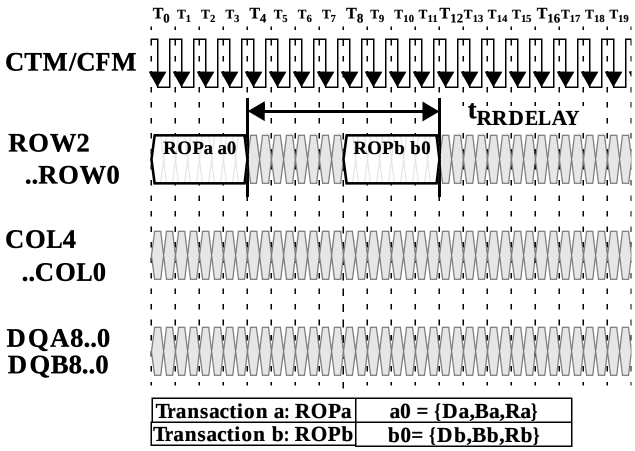


Figure 6: ROW-to-ROW Packet Interaction- Timing

Figure 6 shows two packets on the ROW pins separated by an interval $t_{RRDELAY}$ which depends upon the packet contents. No other ROW packets are sent to bank {Ba} between packet "a" and packet "b" unless noted otherwise. Table 9 summarizes the $t_{RRDELAY}$ values for all possible cases.

Cases RR1 through RR4 show two successive ACT commands. In case RR1, there is no restriction since the ACT commands are to different devices. In case RR2, the t_{RR} restriction applies to the same device with different banks. Case RR4 is illegal (as shown) since bank Ba needs to be precharged. If a PRER to Ba is inserted, $t_{RRDELAY}$ is t_{RC} (t_{RAS} to the PRER command, and t_{RP} to the next ACT).

Cases RR5 through RR8 show an ACT command followed by a PRER command. In cases RR5 and RR6, there are no restrictions since the commands are to different devices or to different banks of the same device. In case RR8, the t_{RAS} restriction means the activated bank must wait before it can be precharged.

Cases RR9 through RR12 show a PRER command followed by an ACT command. In cases RR9 and RR10, there are essentially no restrictions since the commands are to different devices or to different banks of the same device. In case RR12, the same bank must wait t_{RP} for the sense amp and bank to precharge before being activated.

Table 9: ROW-to-ROW Packet Interaction - Rules

Case #	ROPa	Da	Ba	Ra	ROPb	Db	Bb	Rb	$t_{RRDELAY}$	Example
RR1	ACT	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 11
RR2	ACT	Da	Ba	Ra	ACT	== Da	/= {Ba}	x..x	t_{RR}	Figure 11
RR4	ACT	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RC} - illegal unless PRER to {Ba} is given	Figure 10
RR5	ACT	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 11
RR6	ACT	Da	Ba	Ra	PRER	== Da	/= {Ba}	x..x	t_{PACKET}	Figure 11
RR8	ACT	Da	Ba	Ra	PRER	== Da	== {Ba}	x..x	t_{RAS}	Figure 15
RR9	PRER	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 12
RR10	PRER	Da	Ba	Ra	ACT	== Da	/= {Ba}	x..x	t_{PACKET}	Figure 12
RR12	PRER	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RP}	Figure 10
RR13	PRER	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 12
RR14	PRER	Da	Ba	Ra	PRER	== Da	/= {Ba}	x..x	t_{PP}	Figure 12
RR16	PRER	Da	Ba	Ra	PRER	== Da	== Ba	x..x	t_{PP}	Figure 12

ROW-to-ROW Packet Interaction - (con't)

Cases RR13 through RR16 summarize the combinations of two successive PRER commands. In case RR13 there is no restriction since two devices are addressed. In RR14, t_{PP} applies, since the same device is addressed. In RR16, the same bank may be given repeated PRER commands with only the t_{PP} restriction.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, NAPRC, PDNR, RLXR, ATTN, TCAL, and TCEN commands are discussed in later sections (see Table 6 for cross-ref).

ROW-to-COL Packet Interaction

Figure 7 shows two packets on the ROW and COL pins. They must be separated by an interval $t_{RCDELAY}$ which depends upon the packet contents. Table 10 summarizes the $t_{RCDELAY}$ values for all possible cases. Note that if the COL packet is earlier than the ROW packet, it is considered a COL-to-ROW interaction.

Cases RC1 through RC5 summarize the rules when the ROW packet has an ACT command. Figure 15 and Figure 16 show examples of RC5 - an activation followed by a read or write. In cases RC1, RC2, and RC3, there is no interaction of the ROW and COL packets.

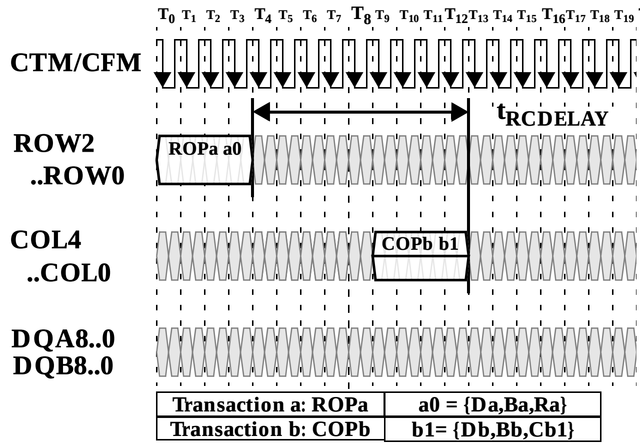


Figure 7: ROW-to-COL Packet Interaction- Timing

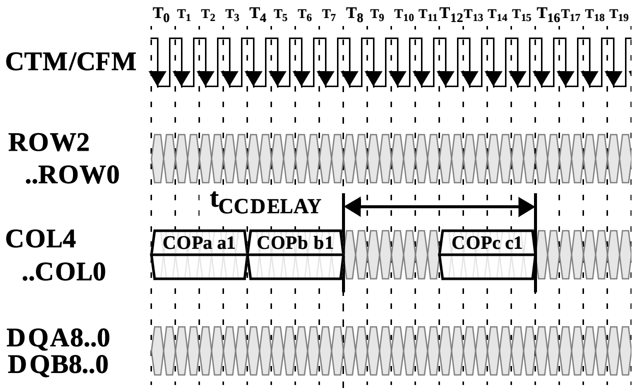
Cases RC6 through RC9 summarize the rules when the ROW packet has a PRER command. There is either no interaction (RC6 through RC8) or an illegal situation with a read or write of a precharged bank (RC9).

The COL pins can also schedule a precharge operation with a RDA, WRA, or PREC command in a COLC packet or a PREX command in a COLX packet. The constraints of these precharge operations may be converted to equivalent PRER command constraints using the rules summarized in Figure 14.

Table 10: ROW-to-COL Packet Interaction - Rules

Case #	ROPa	Da	Ba	Ra	COPb	Db	Bb	Cb1	$t_{RCDELAY}$	Example
RC1	ACT	Da	Ba	Ra	NOCOP,RD,retire	/= Da	xxxx	x..x	0	
RC2	ACT	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC3	ACT	Da	Ba	Ra	RD,retire	== Da	/= {Ba}	x..x	0	
RC5	ACT	Da	Ba	Ra	RD,retire	== Da	== Ba	x..x	t_{RCD}	Figure 15
RC6	PRER	Da	Ba	Ra	NOCOP,RD,retire	/= Da	xxxx	x..x	0	
RC7	PRER	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC8	PRER	Da	Ba	Ra	RD,retire	== Da	/= {Ba}	x..x	0	
RC9	PRER	Da	Ba	Ra	RD,retire	== Da	== {Ba}	x..x	illegal	

COL-to-COL Packet Interaction



Transaction a: COPa	a1 = {Da,Ba,Ca1}
Transaction b: COPb	b1 = {Db,Bb,Cb1}
Transaction c: COPc	c1 = {Dc,Bc,Cc1}

Figure 8: COL-to-COL Packet Interaction- Timing

Figure 8 shows three arbitrary packets on the COL pins. Packets “b” and “c” must be separated by an interval $t_{CCDELAY}$ which depends upon the command and address values in all three packets. Table 11 summarizes the $t_{CCDELAY}$ values for all possible cases.

Cases CC1 through CC5 summarize the rules for every situation other than the case when COPb is a WR command and COPc is a RD command. In CC3, when a RD command is followed by a WR command, a gap of t_{CAC} -t_{CWD} must be inserted between the two COL packets. See Figure 4 for more explanation of why this gap is needed. For cases CC1, CC2, CC4, and CC5, there is no restriction ($t_{CCDELAY}$ is t_{CC}).

In cases CC6 through CC10, COPb is a WR command and COPc is a RD command. The $t_{CCDELAY}$ value needed between these two packets depends upon the command and address in the packet with COPa. In particular, in case CC6 when there is WR-WR-RD command sequence directed to the same device, a gap will be needed between the packets with COPb and COPc. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place. Figure 18 (right) provides a more detailed explanation of this case.

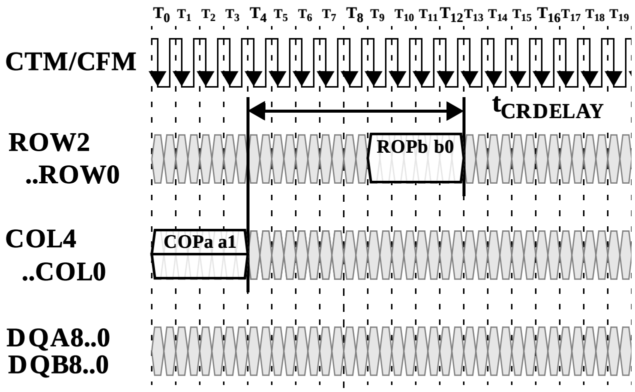
Cases CC7, CC8, CC9 and CC10 have no restriction ($t_{CCDELAY}$ is t_{CC}).

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation PREC to take place. This precharge may be converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 14.

Table 11: COL-to-COL Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	COPb	Db	Bb	Cb1	COPc	Dc	Bc	Cc1	$t_{CCDELAY}$	Example
CC1	xxxx	xxxxx	x..x	x..x	NOCOP	Db	Bb	Cb1	xxxx	xxxxx	x..x	x..x	t_{CC}	
CC2	xxxx	xxxxx	x..x	x..x	RD,WR	Db	Bb	Cb1	NOCOP	xxxxx	x..x	x..x	t_{CC}	
CC3	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	t_{CC}+t_{CAC} -t_{CWD}	Figure 4
CC4	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	RD	xxxxx	x..x	x..x	t_{CC}	Figure 15
CC5	xxxx	xxxxx	x..x	x..x	WR	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	t_{CC}	Figure 16
CC6	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{RTR}	Figure 18
CC7	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	/ = Db	x..x	x..x	t_{CC}	
CC8	WR	/ = Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC9	NOCOP	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC10	RD	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	

COL-to-ROW Packet Interaction



Transaction a: COPa	a1= {Da,Ba,Ca1}
Transaction b: ROPb	b0= {Db,Bb,Rb}

Figure 9: COL-to-ROW Packet Interaction- Timing

Figure 9 shows arbitrary packets on the COL and ROW pins. They must be separated by an interval $t_{CRDELAY}$ which depends upon the command and address values in the packets. Table 12 summarizes the $t_{CRDELAY}$ value for all possible cases.

Cases CR1, CR2, CR3, and CR9 show no interaction between the COL and ROW packets, either because one of the commands is a NOP or because the packets are directed to different devices or to different banks.

Case CR4 is illegal because an already-activated bank is to be re-activated without being precharged

In case CR6, the COLC packet contains a RD command, and the ROW packet contains a PRER command for the same bank. The t_{RDP} parameter specifies the required spacing.

Likewise, in case CR7, the COLC packet causes an automatic retire to take place, and the ROW packet contains a PRER command for the same bank. The t_{RTP} parameter specifies the required spacing.

Case CR8 is labeled “Hazardous” because a WR command should always be followed by an automatic retire before a precharge is scheduled. Figure 19 shows an example of what can happen when the retire is not able to happen before the precharge.

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation to take place. This precharge may converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 14.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, PDNR, and RLXR commands are discussed in a later section.

Table 12: COL-to-ROW Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	ROPb	Db	Bb	Rb	$t_{CRDELAY}$	Example
CR1	NOCOP	Da	Ba	Ca1	x..x	xxxxx	xxxx	x..x	0	
CR2	RD/WR	Da	Ba	Ca1	x..x	/= Da	xxxx	x..x	0	
CR3	RD/WR	Da	Ba	Ca1	x..x	== Da	/= {Ba}	x..x	0	
CR4	RD/WR	Da	Ba	Ca1	ACT	== Da	== {Ba}	x..x	Illegal	
CR6	RD	Da	Ba	Ca1	PRER	== Da	== {Ba}	x..x	t_{RDP}	Figure 15
CR7	retire[a]	Da	Ba	Ca1	PRER	== Da	== {Ba}	x..x	t_{RTP}	Figure 16
CR8	WR[b]	Da	Ba	Ca1	PRER	== Da	== {Ba}	x..x	0	Figure 19
CR9	xxxx	Da	Ba	Ca1	NOROP	xxxxx	xxxx	x..x	0	

a. This is any command which permits the write buffer of device Da to retire (see Table 7). “Ba” is the bank address in the write buffer.
b. This situation is hazardous because the write buffer will be left unretired while the targeted bank is precharged. See Figure 19.

ROW-to-ROW Examples

Figure 10 shows examples of some of the the ROW-to-ROW packet spacings from Table 9. A complete sequence of activate and precharge commands is directed to a bank. The RR8 and RR12 rules apply to this sequence. In addition to satisfying the t_{RAS} and t_{RP} timing parameters, the separation between ACT commands to the same bank must also satisfy the t_{RC} timing parameter (RR4).

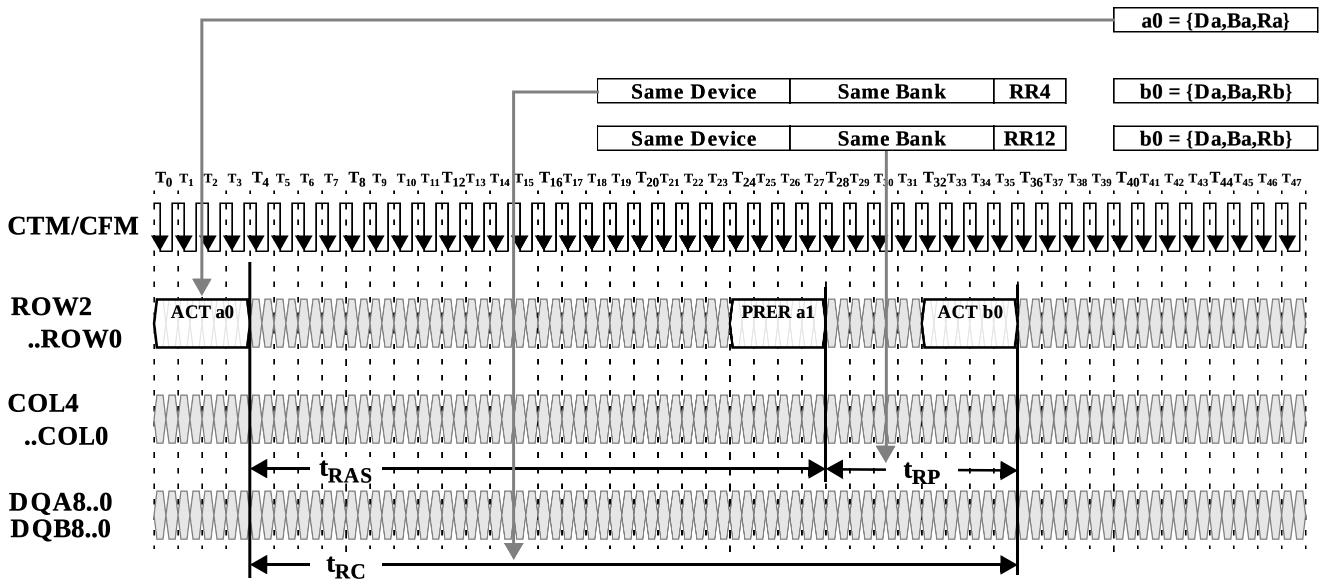


Figure 10: Row Packet Example

Figure 11 shows examples of the ACT-to-ACT (RR1, RR2) and ACT-to-PRER (RR5, RR6) command spacings from Table 9. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same bank or unless they are a similar command type (both PRER or both ACT) directed to the same device.

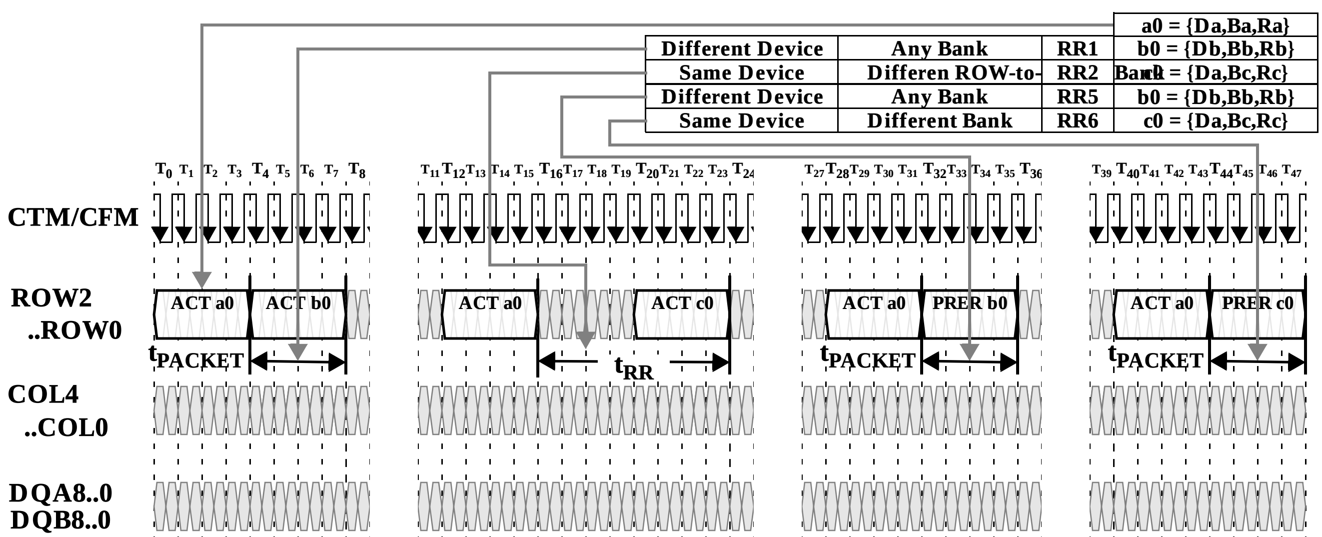


Figure 11: Row Packet Example

Figure 12 shows examples of the PRER-to-PRER (RR13, RR14) and PRER-to-ACT (RR9, RR10) command spacings from Table 9. The RR16 case (PRER-to-PRER to same bank) is not shown, but is similar to RR14. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same bank or unless they are a similar command type (both PRER or both ACT) directed to the same device.

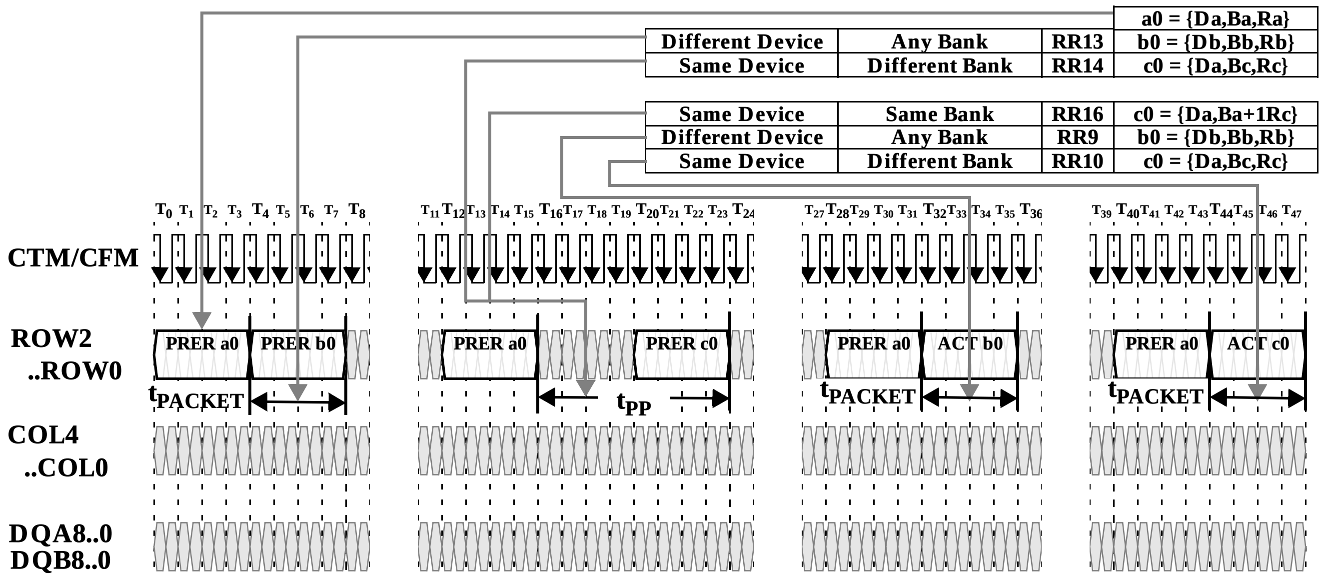


Figure 12: Row Packet Examples

Row and Column Cycle Description

Activate: A row cycle begins with the activate (ACT) operation. The activation process is destructive; the act of sensing the value of a bit in a bank's storage cell transfers the bit to the sense amp, but leaves the original bit in the storage cell with an incorrect value.

Restore: Because the activation process is destructive, a hidden operation called restore is automatically performed. The restore operation rewrites the bits in the sense amp back into the storage cells of the activated row of the bank.

Read/Write: While the restore operation takes place, the sense amp may be read (RD) and written (WR) using column operations. If new data is written into the sense amp, it is automatically forwarded to the storage cells of the bank so the data in the activated row and the data in the sense amp remain identical.

Precharge: When both the restore operation and the column operations are completed, the sense amp and bank are precharged (PRE). This leaves them in the proper state to begin another activate operation.

Intervals: The activate operation requires the interval $t_{RCD,MIN}$ to complete. The hidden restore operation requires the interval $t_{RAS,MIN}$ - $t_{RCD,MIN}$ to complete. Column read / write operations can also be performed during the $t_{RAS,MIN}$ - $t_{RCD,MIN}$ interval . The precharge operation requires the interval $t_{RP,MIN}$ to complete.

Adjacent Banks: An RDRAM device with a "d" or "s" designation indicates it contains a doubled or split core. Sense amps are shared between two adjacent banks in "d" and "s" cores (sense amps are not shared in "i" independent cores).

Precharge Mechanisms

Figure 13 shows an example of precharge with the ROWR packet mechanism. The PRER command must occur a time t_{RAS} after the ACT command, and a time t_{RP} before the next ACT command. This timing will serve as a baseline aginst which the other precharge mechanisms can be compared.

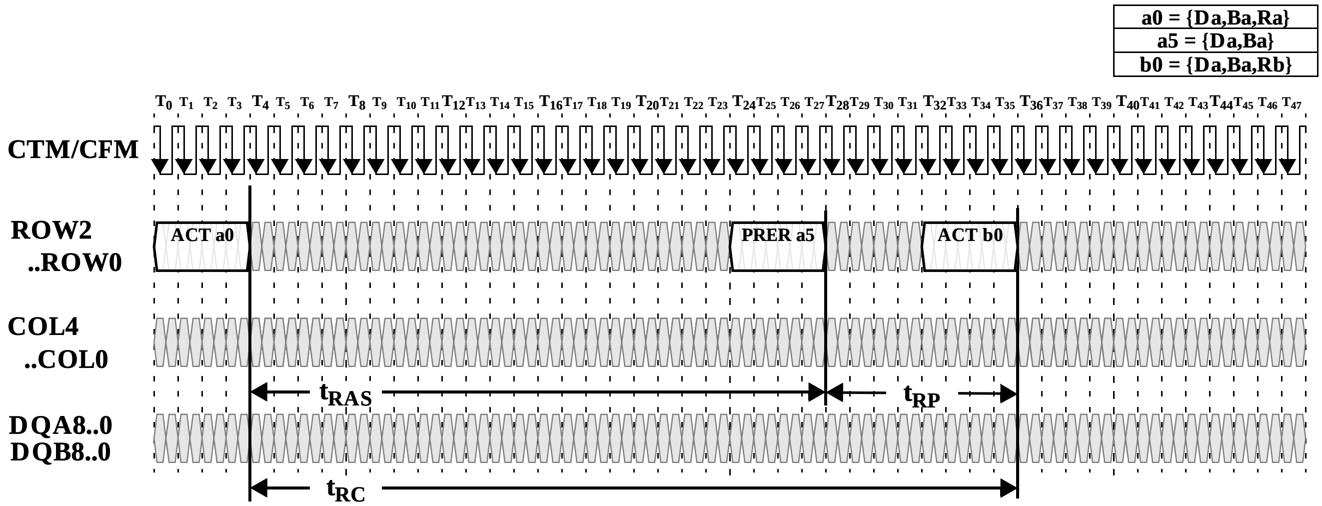


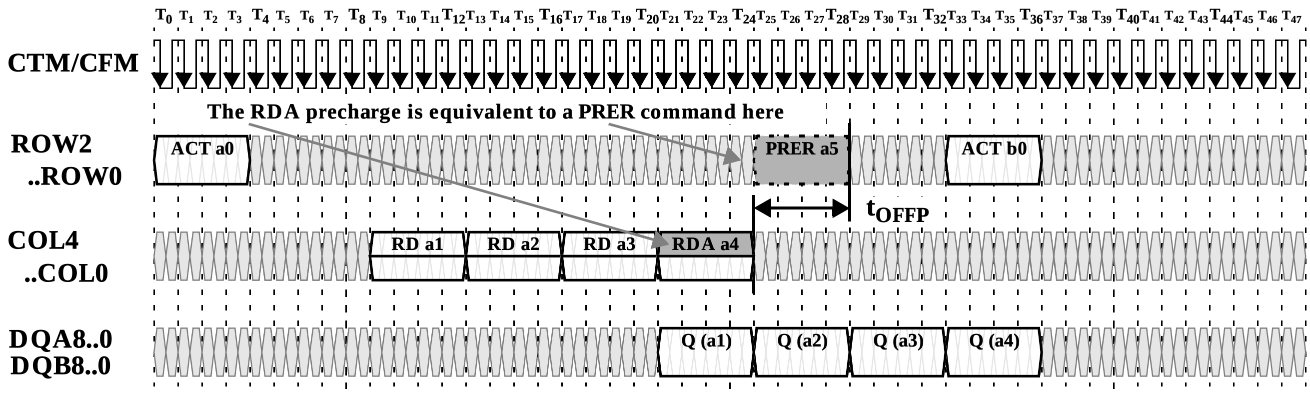
Figure 13: Precharge via PRER Command in ROWR Packet

Figure 14 (top) shows an example of precharge with a RDA command. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these commands is a RDA, which causes the bank to automatically precharge when the final read has finished. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet with the RDA command. The RDA command should be treated as a RD command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets.

Figure 14 (middle) shows an example of precharge with a WRA command. As in the RDA example, a bank is activated with an ROWA packet on the ROW pins. Then, two dualocts are written with WR commands in COLC packets on the COL pins. The second of these commands is a WRA, which causes the bank to automatically precharge when the final write has been retired. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet that causes the automatic retire. The WRA command should be treated as a WR command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets. Note that the automatic retire is triggered by a COLC packet a time t_{RTR} after the COLC packet with the WR command unless the second COLC contains a RD command to the same device. This is described in more detail in Figure 17.

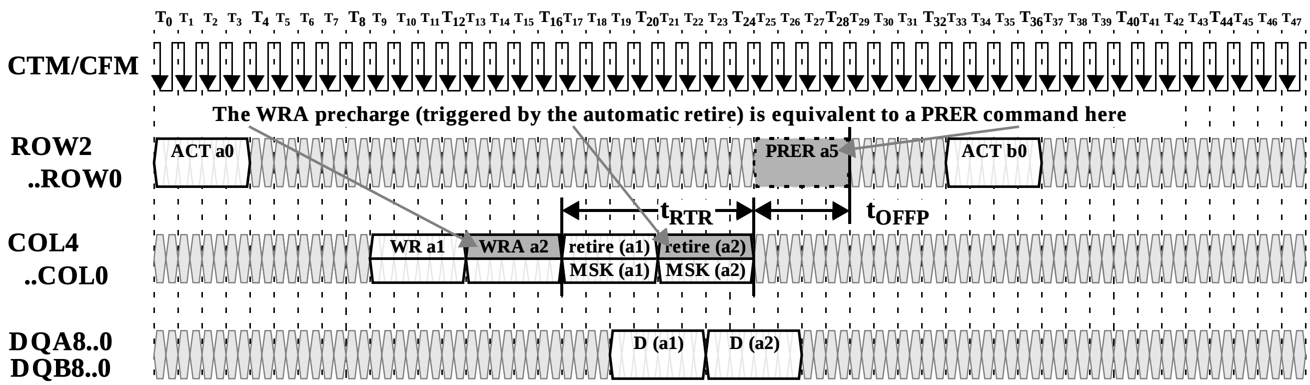
Figure 14 (bottom) shows an example of precharge with a PREX command in an COLX packet. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these COLC packets includes an COLX packet with a PREX command. This causes the bank to precharge with timing equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLX packet with the PREX command.

COLC Packet: RDA Precharge Offset



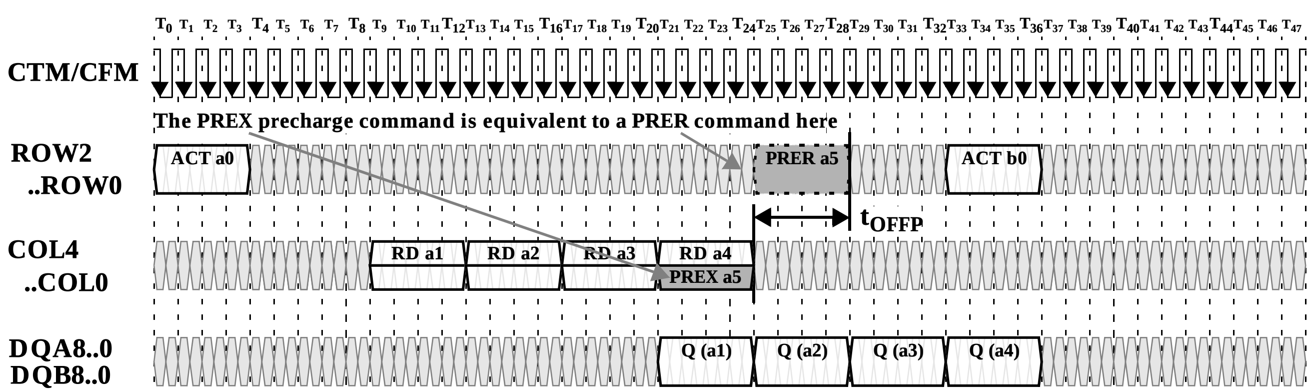
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

COLC Packet: WDA Precharge Offset



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a5 = {Da,Ba}

COLX Packet: PREX Precharge Offset



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

Figure 14: Offsets for Alternate Precharge Mechanisms

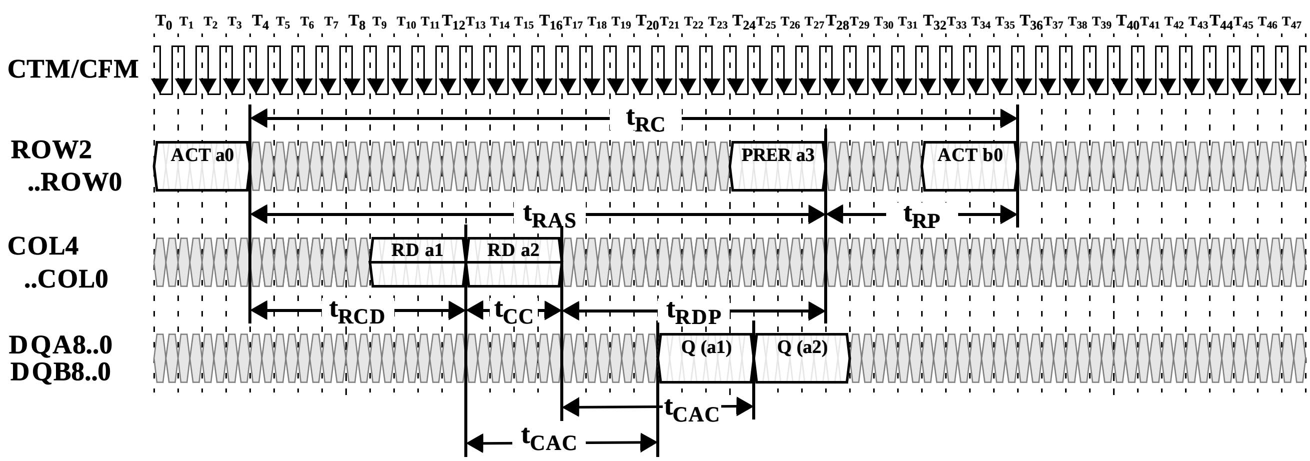
Read Transaction - Example

Figure 15 shows an example of a read transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD} later a RD a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the RD command includes device, bank, and column address (abbreviated as a1). A time t_{CAC} after the RD command the read data dualoct Q(a1) is returned by the device. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA / DQB pins use the beginning of the packet as a timing reference point.

A time t_{CC} after the first COLC packet on the COL pins a second is issued. It contains a RD a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CAC} after the second RD command a second read data dualoct Q(a2) is returned by the device.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval). The PRER command must also occur a time t_{RDP} or more after the last RD command. Note that the t_{RDP} value shown is greater than the $t_{RDP,MIN}$ specification in Table 21. This transaction example reads two dualocts, but there is actually enough time to read three dualocts before t_{RDP} becomes the limiting parameter rather than t_{RAS}. If four dualocts were read, the packet with PRER would need to shift right (be delayed) by one t_{CYCLE} (note - this case is not shown).

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

Figure 15: Read Transaction Example

Write Transaction - Example

Figure 16 shows an example of a write transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD}-t_{RTR} later a WR a1 command is issued in a COLC packet (note that the t_{RCD} interval is measured to the end of the COLC packet with the first retire command). Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the WR command includes device, bank, and column address (abbreviated as a1). A time t_{CWD} after the WR command the write data dualoct D(a1) is issued. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA / DQB pins use the beginning of the packet as a timing reference point.

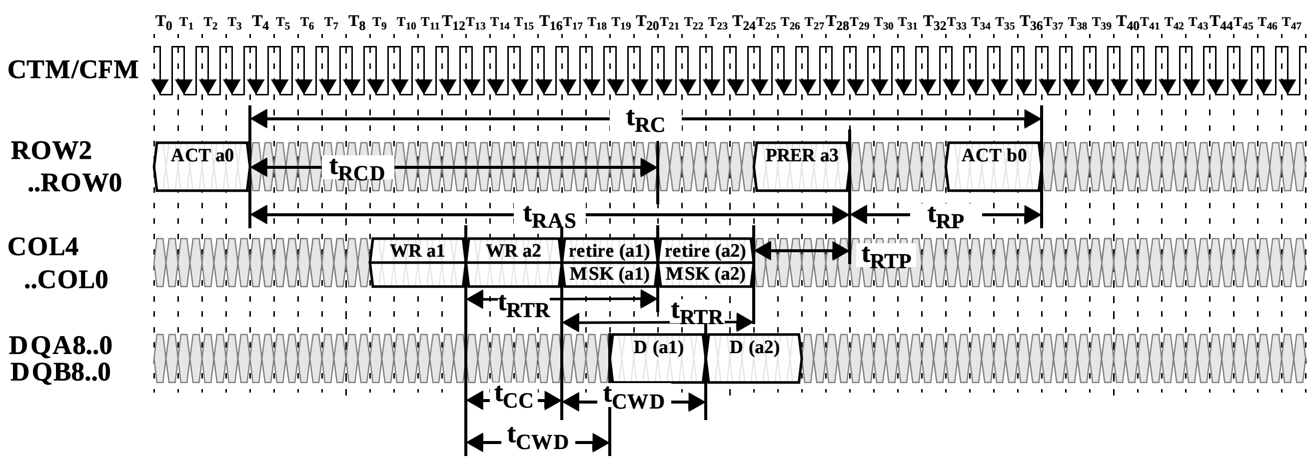
A time t_{CC} after the first COLC packet on the COL pins a second COLC packet is issued. It contains a WR a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CWD} after the second WR command a second write data dualoct D(a2) is issued.

A time t_{RTR} after each WR command an optional COLM packet MSK (a1) is issued, and at the same time a COLC packet is issued causing the write buffer to automatically retire. See Figure 17 for more detail on the write / retire mechanism. If a COLM packet is not used, all data bytes are unconditionally written. If the COLC packet which causes the write buffer to retire is delayed, then the COLM packet (if used) must also be delayed.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval).

A PRER a3 command is issued in an ROWR packet on the ROW pins. The PRER command must occur a time t_{RTP} or more after the last COLC which causes an automatic retire.

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

Figure 16: Write Transaction Example

Write/Retire - Examples

The process of writing a dualoct into a sense amp of an RDRAM bank occurs in two steps. The first step consists of transporting the write command, write address, and write data into the write buffer. The second step happens when the RDRAM device automatically retires the write buffer (with an optional bytemask) into the sense amp. This two-step write process reduces the natural turn-around delay due to the internal bidirectional data pins.

Figure 17 (left) shows an example of this two step process. The first COLC packet contains the WR command and an address specifying device, bank and column. The write data dualoct follows a time t_{CWD} later. This information is loaded into the write buffer of the specified device. The COLC packet which follows a time t_{RTR} later will retire the write buffer. The retire will happen automatically unless (1) a COLC packet is not framed (no COLC packet is present and the S bit is zero), or (2) the COLC packet contains a RD command to the same device. If the retire does not take place at time t_{RTR} after the original WR command, then the device continues to frame COLC packets, looking for the first that is not a RD directed to itself. A bytemask MSK(a1) may be supplied in a COLM packet aligned with the COLC that retires the write buffer at time t_{RTR} after the WR command.

The memory controller must be aware of this two-step write / retire process. Controller performance can be improved, but only if the controller design accounts for several side effects.

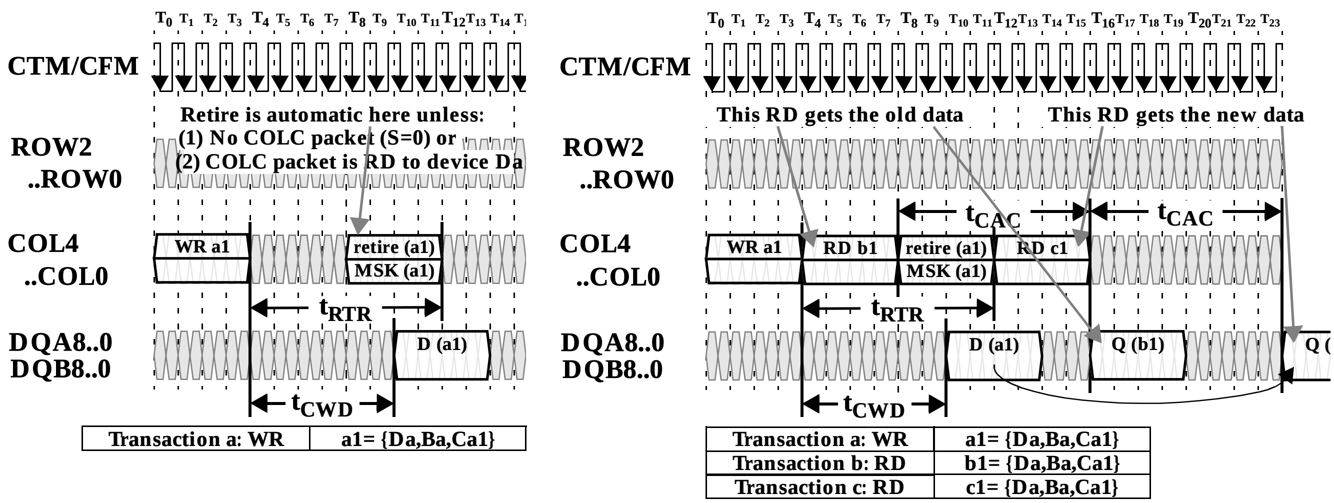


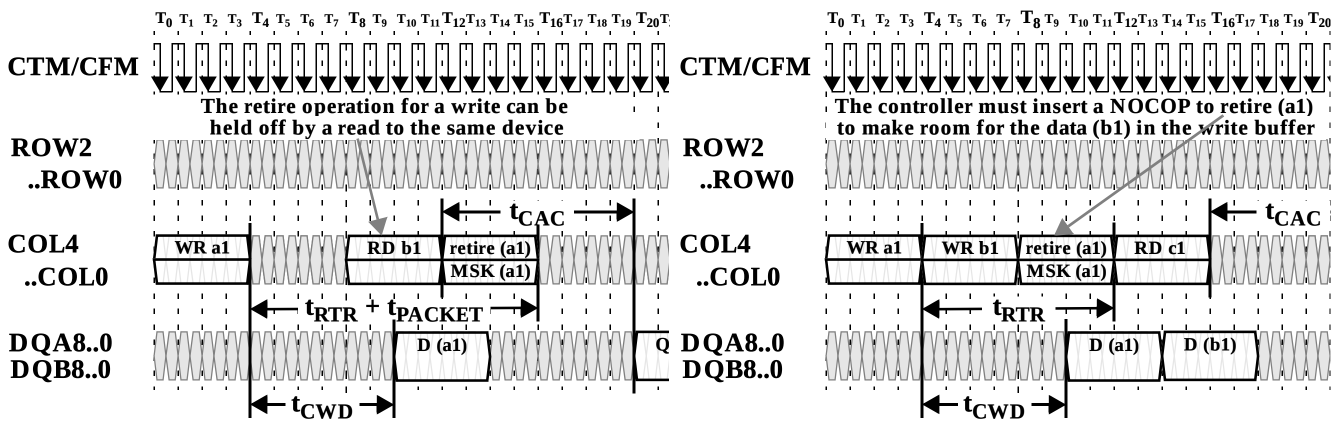
Figure 17: Normal Retire (left) and Retire/Read Ordering (right)

Figure 17 (right) shows the first of these side effects. The first COLC packet has a WR command which loads the address and data into the write buffer. The third COLC causes an automatic retire of the write buffer to the sense amp. The second and fourth COLC packets (which bracket the retire packet) contain RD commands with the same device, bank and column address as the original WR command. In other words, the same dualoct address that is written is read both before and after it is actually retired. The first RD returns the old dualoct value from the sense amp before it is overwritten. The second RD returns the new dualoct value that was just written.

Figure 18 (left) shows the result of performing a RD command to the same device in the same COLC packet slot that would normally be used for the retire operation. The read may be to any bank and column address; all that matters is that it is to the same device as the WR command. The retire operation and MSK(a1) will be delayed by a time t_{PACKET} as a result. If the RD command used the same bank and column address as the WR command, the old data from the sense amp would be returned. If many RD commands to the same device were issued instead of the single one that is shown, then the retire operation would be held off an arbitrarily long time. However, once a RD to another device or a WR or NOCOP to any device is issued, the retire will take place. Figure 18 (right) illustrates a situation in which the controller wants to issue a WR-WR-RD COLC packet sequence, with all commands addressed to the same device, but addressed to any combination of banks and columns.

Write/Retire Examples - continued

The RD will prevent a retire of the first WR from automatically happening. But the first dualoct D(a1) in the write buffer will be overwritten by the second WR dualoct D(b1) if the RD command is issued in the third COLC packet. Therefore, it is required in this situation that the controller issue a NOCOP command in the third COLC packet, delaying the RD command by a time of t_{PACKET}. This situation is explicitly shown in Table 11 for the cases in which $t_{CCDELAY}$ is equal to t_{RTR}.

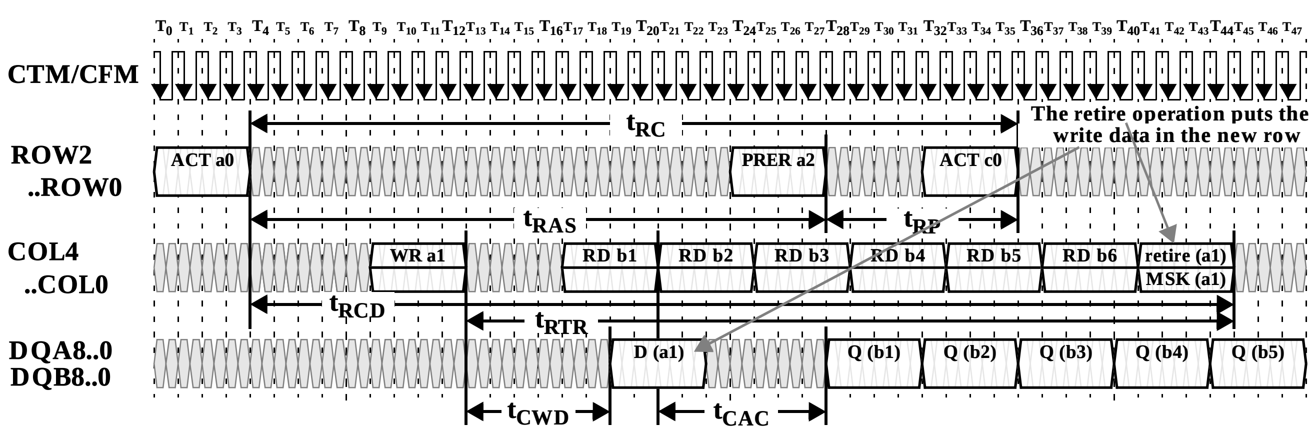


Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: RD	b1= {Da,Bb,Cb1}

Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: WR	b1= {Da,Bb,Cb1}
Transaction c: RD	c1= {Da,Bc,Cc1}

Figure 18: Retire Held Off by Read (left) and Controller Forces WWR Gap (right)

Figure 19 shows a possible result when a retire is held off for a long time (an extended version of Figure 18-left). After a WR command, a series of six RD commands are issued to the same device (but to any combination of bank and column addresses). In the meantime, the bank Ba to which the WR command was originally directed is precharged, and a different row Rc is activated. When the retire is automatically performed, it is made to this new row, since the write buffer only contains the bank and column address, not the row address. The controller can insure that this doesn't happen by never precharging a bank with an unretired write buffer. Note that in a system with more than one RDRAM device, there will never be more than two RDRAM devices with unretired write buffers. This is because a WR command issued to one device automatically retires the write buffers of all other devices written a time t_{RTR} before or earlier.



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba}
Transaction b: RD	b1 = {Da,Bb,Cb1}	b2 = {Da,Bb,Cb2}	b3= {Da,Bb,Cb3}
	b4 = {Da,Bb,Cb4}	b5 = {Da,Bb,Cb5}	b6 = {Da,Bb,Cb6}
Transaction c: WR	c0 = {Da,Ba,Rc}		

WARNING
This sequence is hazardous and must be used with caution

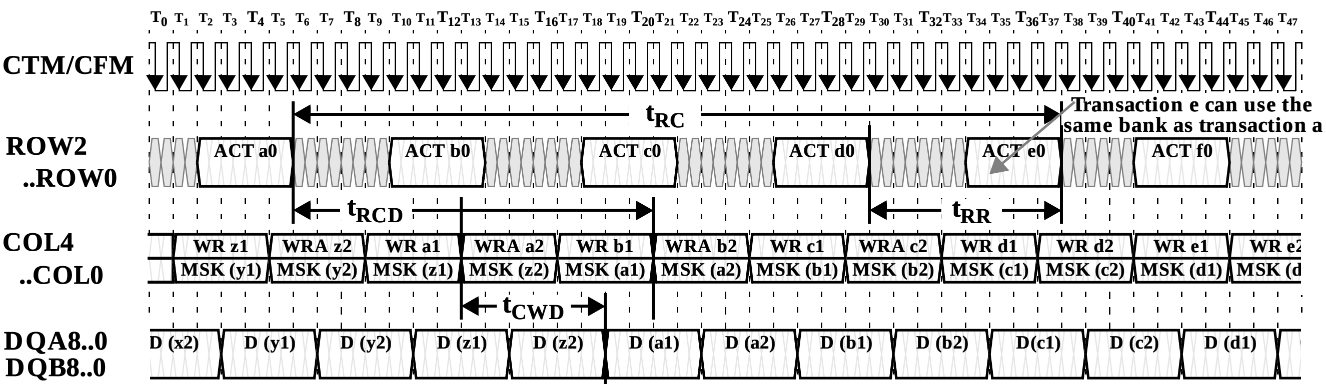
Figure 19: Retire Held Off by Reads to Same Device, Write Buffer Retired to New Row

Interleaved Write - Example

Figure 20 shows an example of an interleaved write transaction. Transactions similar to the one presented in Figure 16 are directed to different banks of a single RDRAM device. This allows a new transaction to be issued once every t_{RR} interval rather than once every t_{RC} interval (four times more often). The DQ data pin efficiency is 100% with this sequence.

With two dualocts of data written per transaction, the COL, DQA, and DQB pins are fully utilized. Banks are precharged using the WRA autoprecharge option rather than the PRER command in an ROWR packet on the ROW pins.

In this example, the first transaction is directed to device Da and bank Ba. The next three transactions are directed to the same device Da, but need to use different banks Bb, Bc, Bd so there is no bank conflict. The fifth transaction could be redirected back to bank Ba without interference, since the first transaction would have completed by then (t_{RC} has elapsed). Each transaction may use any value of row address (Ra, Rb, ..) and column address (Ca1, Ca2, Cb1, Cb2, ...).



Transaction y: WR	y0 = {Da,Ba+1,Ry}	y1 = {Da,Ba+1,Cy1}	y2= {Da,Ba+1,Cy2}	y3 = {Da,Ba+1}
Transaction z: WR	z0 = {Da,Ba+3,Rz}	z1 = {Da,Ba+3,Cz1}	z2= {Da,Ba+3,Cz2}	z3 = {Da,Ba+3}
Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+1,Rc}	c1 = {Da,Ba+1,Cc1}	c2= {Da,Ba+1,Cc2}	c3 = {Da,Ba+1}
Transaction d: WR	d0 = {Da,Ba+3,Rd}	d1 = {Da,Ba+3,Cd1}	d2= {Da,Ba+3,Cd2}	d3 = {Da,Ba+3}
Transaction e: WR	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 20: Interleaved Write Transaction with Two Dualoct Data Length

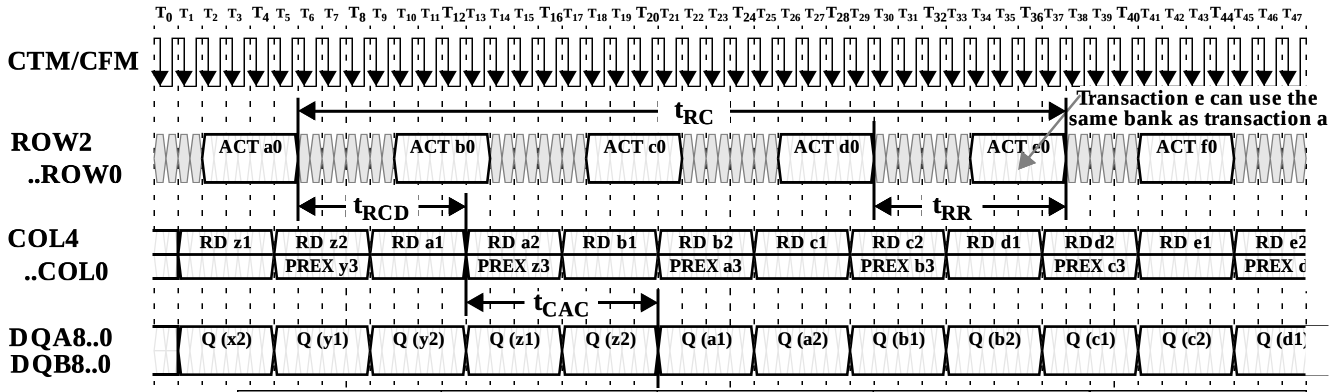
Interleaved Read - Example

Figure 21 shows an example of interleaved read transactions. Transactions similar to the one presented in Figure 15 are directed to different banks of a single RDRAM device. The address sequence is identical to the one used in the previous write example. The DQ data pins efficiency is also 100%. The only difference with the write example (aside from the use of the RD command rather than the WR command) is the use of the PREX command in a COLX packet to precharge the banks rather than the RDA command. This is done because the PREX is available for a readtransaction but is not available for a masked write transaction.

Interleaved RRWW - Example

Figure 22 shows a steady-state sequence of 2-dualoct RD / RD / WR / WR.. transactions directed to different banks of a single RDRAM device. This is similar to the interleaved write and read examples in Figure 20 and Figure 21 except that bubble cycles need to be inserted by the controller at read / write boundaries. The DQ data pin efficiency for the example in Figure 22 is 32 / 42 or 76%. If there were more RDRAMdevices on the Channel, the DQ pin efficiency would approach 32 / 34 or 94% for the two-dualoct RRWW sequence (this case is not shown).

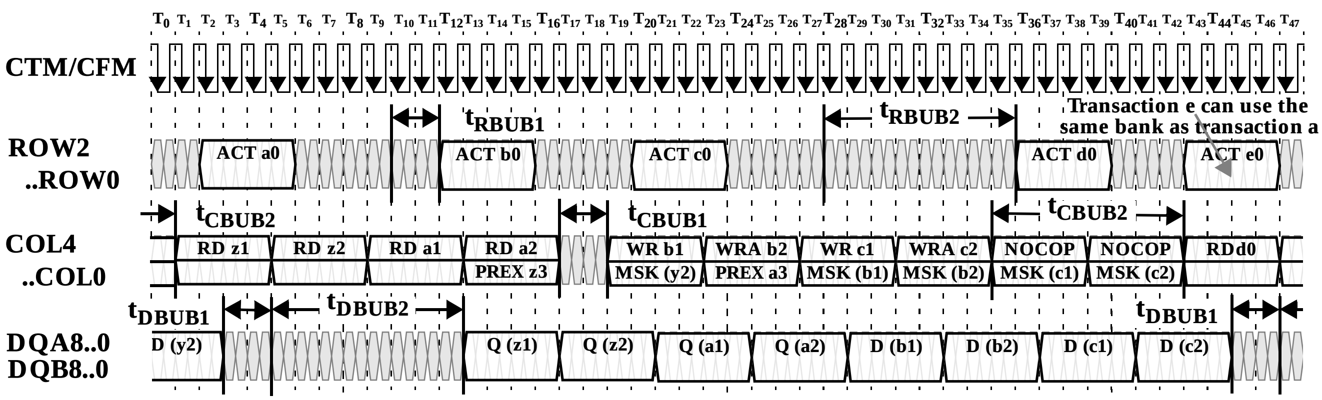
In Figure 22, the first bubble type t_{CBUB1} is inserted by the controller between a RD and WR command on the COL pins. This bubble accounts for the round-trip propagation delay that is seen by read data, and is explained in detail in Figure 4. This bubble appears on the DQA and DQB pins as t_{DBUB1} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB1}.



Transaction y: RD	y0 = {Da,Ba+1,Ry}	y1 = {Da,Ba+1,Cy1}	y2= {Da,Ba+1,Cy2}	y3 = {Da,Ba+1}
Transaction z: RD	z0 = {Da,Ba+3,Rz}	z1 = {Da,Ba+3,Cz1}	z2= {Da,Ba+3,Cz2}	z3 = {Da,Ba+3}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: RD	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: RD	c0 = {Da,Ba+1,Rc}	c1 = {Da,Ba+1,Cc1}	c2= {Da,Ba+1,Cc2}	c3 = {Da,Ba+1}
Transaction d: RD	d0 = {Da,Ba+3,Rd}	d1 = {Da,Ba+3,Cd1}	d2= {Da,Ba+3,Cd2}	d3 = {Da,Ba+3}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: RD	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 21: Interleaved Read Transaction with Two Dualoct Data Length

The second bubble type t_{CBUB2} is inserted (as a NOCOP command) by the controller between a WR and RD command on the COL pins when there is a WR-WR-RD sequence to the same device. This bubble enables write data to be retired from the write buffer without being lost, and is explained in detail in Figure 18. There would be no bubble if address c0 and address d0 were directed to different devices. This bubble appears on the DQA and DQB pins as t_{DBUB2} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB2}.



Transaction y: RD	y0 = {Da,Ba+1,Ry}	y1 = {Da,Ba+1,Cy1}	y2= {Da,Ba+1,Cy2}	y3 = {Da,Ba+1}
Transaction z: RD	z0 = {Da,Ba+3,Rz}	z1 = {Da,Ba+3,Cz1}	z2= {Da,Ba+3,Cz2}	z3 = {Da,Ba+3}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: RD	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: RD	c0 = {Da,Ba+1,Rc}	c1 = {Da,Ba+1,Cc1}	c2= {Da,Ba+1,Cc2}	c3 = {Da,Ba+1}
Transaction d: RD	d0 = {Da,Ba+3,Rd}	d1 = {Da,Ba+3,Cd1}	d2= {Da,Ba+3,Cd2}	d3 = {Da,Ba+3}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: RD	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 22: Interleaved RRWW Sequence with Two Dualoct Data Length

Control Register Transactions

The RDRAM device has two CMOS input pins SCK and CMD and two CMOS input/output pins SIO0 and SIO1. These provide serial access to a set of control registers in the RDRAM device. These control registers provide configuration information to the controller during the initialization process. They also allow an application to select the appropriate operating mode of the RDRAM device.

SCK (serial clock) and CMD (command) are driven by the controller to all RDRAM devices in parallel. SIO0 and SIO1 are connected (in a daisy chain fashion) from one RDRAM device to the next. In normal operation, the data on SIO0 is repeated on SIO1, which connects to SIO0 of the next RDRAM device (the data is repeated from SIO1 to SIO0 for a read data packet). The controller connects to SIO0 of the first RDRAM device.

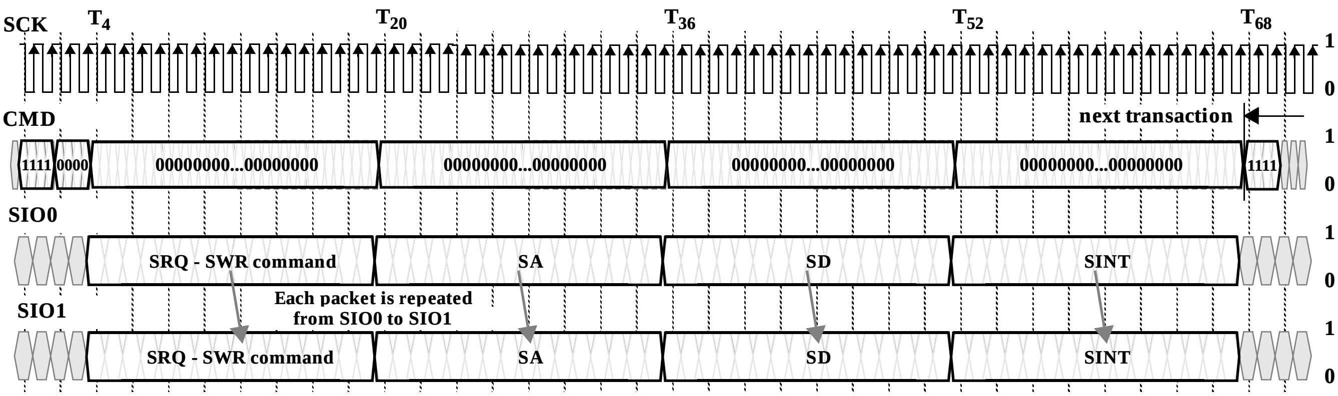


Figure 23: Serial Write (SWR) Transaction to Control Register

Write and read transactions are each composed of four packets, as shown in Figure 23 and Figure 24. Each packet consists of 16 bits, as summarized in Table 13 and Table 14. The packet bits are sampled on the falling edge of SCK. A transaction begins with a SRQ (Serial Request) packet. This packet is framed with a 11110000 pattern on the CMD input (note that the CMD bits are sampled on both the falling edge and the rising edge of SCK). The SRQ packet contains the SOP3..SOP0 (Serial Opcode) field, which selects the transaction type. The SDEV5..SDEV0 (Serial Device address) selects one of the 32 RDRAM devices. If SBC (Serial Broadcast) is set, then all RDRAM devices are selected. The SA (Serial Address) packet contains a 12 bit address for selecting a register.

A write transaction has a SD (Serial Data) packet next. This contains 16 bits of data that is written into the selected control register. A SINT (Serial Interval) packet is last, providing some delay for any side-effects to take place. A read transaction has a SINT packet, then a SD packet. This provides delay for the selected RDRAM device to access the control register. The SD read data packet travels in the opposite direction (towards the controller) from the other packet types. Because the RDRAM device drives data on the falling SCK edge, the read data transmit window is offset $t_{SCYCLE}/2$ relative to the other packet types. The SCK cycle time will accomodate the total propagation delay.

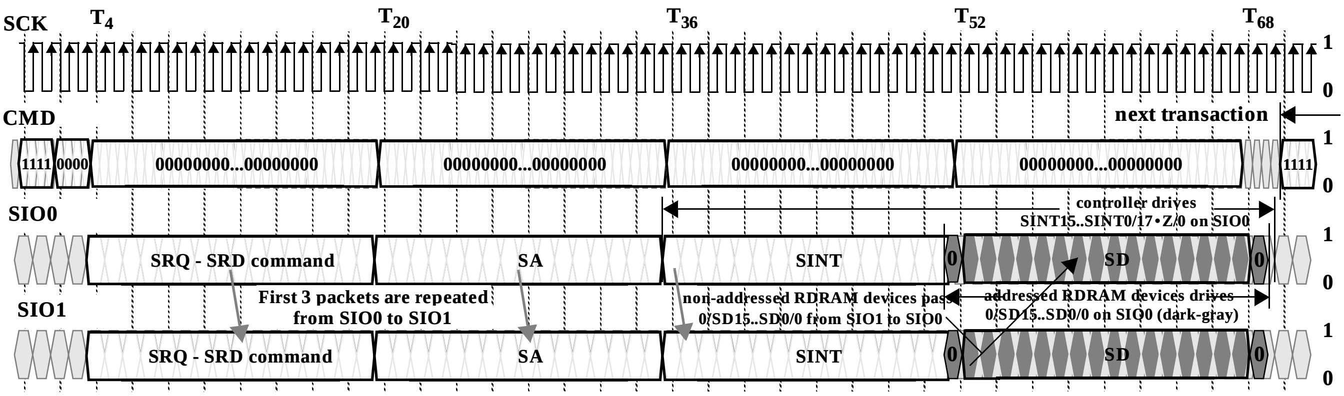


Figure 24: Serial Read (SRD) Transaction Control Register

Control Register Packets

Table 13 summarizes the formats of the four packet types for control register transactions. Table 14 summarizes the fields that are used within the packets.

Figure 25 shows the transaction format for the SETR, CLRR, and SETF commands. These transactions consist of a single SRQ packet, rather than four packets like the SWR and SRD commands. The same framing sequence on the CMD input is used, however.

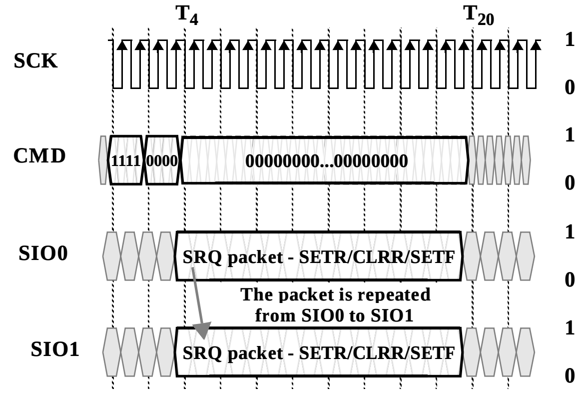


Figure 25: SETR, CLRR,SETF Transaction

Table 13: Control Register Packet Formats

SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD	SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD
0	rsrv	rsrv	0	SD15	8	SOP1	SA7	0	SD7
1	rsrv	rsrv	0	SD14	9	SOP0	SA6	0	SD6
2	rsrv	rsrv	0	SD13	10	SBC	SA5	0	SD5
3	rsrv	rsrv	0	SD12	11	SDEV4	SA4	0	SD4
4	rsrv	SA11	0	SD11	12	SDEV3	SA3	0	SD3
5	SDEV5	SA10	0	SD10	13	SDEV2	SA2	0	SD2
6	SOP3	SA9	0	SD9	14	SDEV1	SA1	0	SD1
7	SOP2	SA8	0	SD8	15	SDEV0	SA0	0	SD0

Table 14: Field Description for Control Register Packets

Field	Description
rsrv	Reserved. Should be driven as “0” by controller.
SOP3..SOP0	0000 - SRD. Serial read of control register {SA11..SA0} of RDRAM device {SDEV5..SDEV0}.
	0001 - SWR. Serial write of control register {SA11..SA0} of RDRAM device {SDEV5..SDEV0}.
	0010 - SETR. Set Reset bit, all control registers assume their reset values.[a] Must be followed by a delay and a CLRR[b].
	0100 - SETF. Set fast (normal) clock mode. 4 t_{SCYCLE} delay until next command.
	1011 - CLRR. Clear Reset bit, all control registers retain their reset values.[a] 4 t_{SCYCLE} delay until next command.
	1111 - NOP. No serial operation.
	0011, 0101-1010, 1100-1110 - RSRV. Reserved encodings.
SDEV5..SDEV0	Serial device. Compared to SDEVID5..SDEVID0 field of INIT control register field to select the RDRAM device to which the transaction is directed.
SBC	Serial broadcast. When set, RDRAM devices ignore {SDEV5..SDEV0} for RDRAM device selection.
SA11..SA0	Serial address. Selects which control register of the selected RDRAM device is read or written.
SD15..SD0	Serial data. The 16 bits of data written to or read from the selected control register of the selected RDRAM device.

a. The SETR and CLRR commands must always be applied in two successive transactions to RDRAM devices; i.e. they may not be used in isolation. This is called “SETR / CLRR Reset”.
b. A minimum gap equal to the larger of {$16 \cdot t_{SCYCLE}$, $2816 \cdot t_{CYCLE}$} must be inserted between a SETR / CLRR command pair.

Initialization

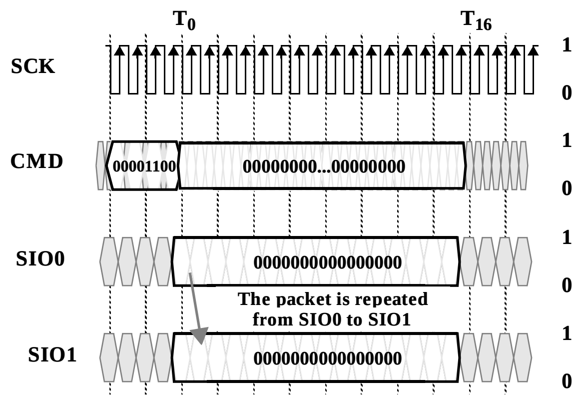


Figure 26: SIO Reset Sequence

Initialization refers to the process that a controller must go through after power is applied to the system or the system is reset. The controller prepares the RDRAM sub-system for normal Channel operation by (primarily) using a sequence of control register transactions on the serial CMOS pins. The following steps outline the sequence seen by the various memory subsystem components (including the RDRAM components) during initialization. This sequence is available in the form of reference code. Contact Rambus Inc. for more information.

1.0 Start Clocks - This step calculates the proper clock frequencies for PClk (controller logic), SynClk (RAC block), RefClk (DRCG component), CTM (RDRAM component), and SCK (SIO block).

2.0 RAC Initialization - This step causes the INIT block to generate a sequence of pulses which resets the RAC, performs RAC maintainance operations, and measures timing intervals in order to ensure clock stability.

3.0 RDRAM device Initialization - This stage performs most of the steps needed to initialize the RDRAM devices. The rest are performed in stages 5.0, 6.0, and 7.0. All of the steps in 3.0 are carried out through the SIO block interface.

- **3.1/3.2 SIO Reset -** This reset operation is performed before any SIO control register read or write transactions. It clears ten registers (TEST34, CCA, CCB, SKIP, NAPX, PDNXA, PDNX, TCPS, TCYCLE, TEST77, TEST78, and TEST79) and places the INIT register into a special state (all bits cleared except SKP and SDEVID fields are set to ones). SCK must be held low until SIOReset.
- **3.3 Write SDEVID Register -** The SDEVID (serial device identification) register of each RDRAM device is written with a unique address value so that directed SIO read and write transactions can be performed. This address value increases from 0 to 31 according to the distance an RDRAM device is from the ASIC component on the SIO bus (the closest RDRAM device is address 0).
- **3.4 Write DEVID Register -** The DEVID (device identification) register of each RDRAM device is written with a unique address value so that directed memory read and write transactions can be performed. This address value increases from 0 to 31. The DEVID value is not necessarily the same as the SDEVID value. RDRAM devices are sorted into regions of the same core configuration (number of bank, row, and column address bits and core type).
- **3.5 Write PDNX,PDNXA Registers -** The PDNX and PDNXA registers are written with values that are used to measure the timing intervals connected with an exit from the PDN (powerdown) power state.
- **3.6 Write NAPX Register -** The NAPX register is written with values that are used to measure the timing intervals connected with an exit from the NAP power state.
- **3.7 Write TPARM Register -** The TPARM register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set each RDRAM device to the minimum value permitted for the system. This will be adjusted later in stage 6.0.
- **3.8 Write TCDLY1 Register -** The TCDLY1 register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set each RDRAM device to the minimum value permitted for the system. This will be adjusted later in stage 6.0.
- **3.9 Write TFRM Register -** The TFRM register is written with a value that is related to the t_{RCD} parameter for the system. The t_{RCD} parameter is

the time interval between a ROW packet with an activate command and the COL packet with a read or write command.

- ❐ **3.10 SETR/CLRR -** Each RDRAM device is given a SETR command and a CLRR command through the SIO block. This sequence performs a second reset operation on the RDRAM devices.
- ❐ **3.11 Write CCA and CCB Registers -** These registers are written with a value halfway between their minimum and maximum values. This shortens the time needed for the RDRAM devices to reach their steady-state current control values in stage 5.0.
- ❐ **3.12 Powerdown Exit -** The RDRAM devices are in the PDN power state at this point. A broadcast PDNExit command is performed by the SIO block to place the RDRAM devices in the RLX (relax) power state in which they are ready to receive ROW packets.
- ❐ **3.13 SETF -** Each RDRAM device is given a SETF command through the SIO block. One of the operations performed by this step is to generate a value for the AS (autoskip) bit in the SKIP register and fix the RDRAM device to a particular read domain.

4.0 Controller Configuration- This stage initializes the controller block. Each step of this stage will set a field of the ConfigRMC[63:0] bus to the appropriate value. Other controller implementations will have similar initialization requirements, and this stage may be used as a guide.

- ❐ **4.1 Initial Read Data Offset-** The ConfigRMC bus is written with a value which determines the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The value written sets RMC.d1 to the minimum value permitted for the system. This will be adjusted later in stage 6.0.
- ❐ **4.2 Configure Row/Column Timing -** This step determines the values of the $t_{RAS,MIN}$, $t_{RP,MIN}$, $t_{RC,MIN}$, $t_{RCD,MIN}$, $t_{RR,MIN}$, and $t_{PP,MIN}$ RDRAM timing parameters that are present in the system. The ConfigRMC bus is written with values that will be compatible with all RDRAM devices that are present.
- ❐ **4.3 Set Refresh Interval -** This step determines the values of the $t_{REF,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.
- ❐ **4.4 Set Current Control Interval -** This step determines the values of the $t_{CCTRL,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.
- ❐ **4.5 Set Slew Rate Control Interval -** This step determines the values of the $t_{TEMP,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.
- ❐ **4.6 Set Bank/Row/Col Address Bits -** This step determines the number of RDRAM bank, row, and column address bits that are present in the system. It also determines the RDRAM core types (independent, doubled, or split) that are present. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

5.0 RDRAM Current Control - This step causes the INIT block to generate a sequence of pulses which performs RDRAM maintainance operations.

6.0 RDRAM Core, Read Domain Initialization- This stage completes the RDRAM device initialization

- ❐ **6.1 RDRAM Core Initialization -** A sequence of 192 memory refresh transactions is performed in order to place the cores of all RDRAM devices into the proper operating state.
- ❐ **6.2 RDRAM Read Domain Initialization -** A memory write and memory read transaction is performed to each RDRAM device to determine which read domain each RDRAM device occupies. The programmed delay of each RDRAM device is then adjusted so the total RDRAM read delay (propagation delay plus programmed delay) is constant. The TPARM and TCDLY1 registers of each RDRAM device are rewritten with the appropriate read delay values. The ConfigRMC bus is also rewritten with an updated value.

7.0 Other RDRAM Register Fields - This stage rewrites the INIT register with the final values of the LSR, NSR, and PSR fields.

In essence, the controller must read all the read-only configuration registers of all RDRAM devices (or it must read the SPD device present on each RIMM), it must process this information, and then it must write all the read-write registers to place the RDRAM devices into the proper operating mode.

Initialization Note [1]: During the initialization process, it is necessary for the controller to perform 128 current control operations (3xCAL, 1xCAL / SAM) and one temperature calibrate operation (TCEN / TCAL) after reset or after powerdown (PDN) exit.

Initialization Note [2]: There are two classes of 64 / 72Mbit RDRAM device. They are distinguished by the “S28IECO” bit in the SPD. The behavior of the RDRAM device at initialization is slightly different for the two types:
S28IECO=0: Upon powerup the device enters ATTN state. The serial operations SETR, CLRR, and SETF are performed without requiring a SDEVID match of the SBC bit (broadcast) to be set.
S28IECO=1: Upon powerup the device enters PDN state. The serial operations SETR, CLRR, and SETF require a SDEVID match.
See the document detailing the reference initialization procedure for more information on how to handle this in a system.

Initialization Note [3]: After the step of equalizing the total read delay of each RDRAM device has been completed (i.e. after the TCDLY0 and TCDLY1 fields have been written for the final time), a single final memory read transaction should be made to each RDRAM device in order to ensure that the output pipeline stages have been cleared.

Initialization Note [4]: The SETF command (in the serial SRQ packet) should only be issued once during the Initialization process, as should the SETR and CLRR commands.

Initialization Note [5]: The CLRR command (in the serial SRQ packet) leaves some of the contents of the memory core in an indeterminate state.

Control Register Summary

Table 15 summarizes the RDRAM control registers. Detail is provided for each control register in Figure 27 through Figure 43. Read-only bits which are shaded gray are unused and return zero. Read-write bits which are shaded gray are reserved and should always be written with zero. The RIMM SPD Application Note (DL-0054) describes additional read-only configuration registers which are present on Direct RIMMs.

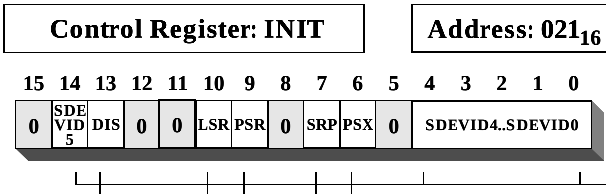
The state of the register fields are potentially affected by the IO Reset operation or the SETR / CLRR operation. This is indicated in the text accompanying each register diagram.

Table 15: Control Register Summary

SA11..SA0	Register	Field	read-write/ read-only	Description
021_{16}	INIT	SDEVID	read-write, 6 bits	Serial device ID. Device address for control register read / write.
		PSX	read-write, 1 bit	Power select exit. PDN / NAP exit with device addr on DQA5..0.
		SRP	read-write, 1 bit	SIO repeater. Used to initialize RDRAM device.
		PSR	read-write, 1 bit	PDN self-refresh. Enables self-refresh in PDN mode.
		LSR	read-write, 1 bit	Low power self-refresh. Enables low power self-refresh.
		DIS	read-write, 1 bit	RDRAM disable.
022_{16}	TEST34	TEST34	write-only, 16 bits	Test register.
023_{16}	CNFGA	REFBIT	read-only, 3 bit	Refresh bank bits. Used for multi-bank refresh.
		DBL	read-only, 1 bit	Double. Specifies doubled-bank architecture
		MVER	read-only, 6 bit	Manufacturer version. Manufacturer identification number.
		PVER	read-only, 6 bit	Protocol version. Specifies version of Direct protocol supported.
024_{16}	CNFGB	BYT	read-only, 1 bit	Byte. Specifies an 8-bit or 9-bit byte size.
		DEVTYP	read-only, 3 bit	Device type. Device can be RDRAM device or some other device category.
		SPT	read-only, 1 bit	Split-core. Each core half is an individual dependent core.
		CORG	read-only, 6 bit	Core organization. Bank, row, column address field sizes.
		SVER	read-only, 6 bit	Stepping version. Mask version number.

Table 15: Control Register Summary (Continued)

SA11..SA0	Register	Field	read-write/ read-only	Description
040_{16}	DEVID	DEVID	read-write, 5 bits	Device ID. Device address for memory read / write.
041_{16}	REFB	REFB	read-write, two bits	Refresh bank. Next bank to be refreshed by self-refresh.
042_{16}	REFR	REFR	read-write, thirteen bits	Refresh row. Next row to be refreshed by REFA, self-refresh.
043_{16}	CCA	CCA	read-write, 7 bits	Current control A. Controls I_{OL} output current for DQA.
		ASYMA	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL} / V_{OH} swing for DQA.
044_{16}	CCB	CCB	read-write, 7 bits	Current control B. Controls I_{OL} output current for DQB.
		ASYMB	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL} / V_{OH} swing for DQB.
045_{16}	NAPX	NAPXA	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A.
		NAPX	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A + phase B.
		DQS	read-write, 1 bits	DQ select. Selects CMD framing for NAP / PDN exit.
046_{16}	PDNXA	PDNXA	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A.
047_{16}	PDNX	PDNX	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A + phase B.
048_{16}	TPARM	TCAS	read-write, 2 bits	t_{CAS-C} core parameter. Determines t_{OFFP} datasheet parameter.
		TCLS	read-write, 2 bits	t_{CLS-C} core parameter. Determines t_{CAC} and t_{OFFP} parameters.
		TCDLY0	read-write, 3 bits	$t_{CDLY0-C}$ core parameter. Programmable delay for read data.
049_{16}	TFRM	TFRM	read-write, 4 bits	t_{FRM-C} core parameter. Determines ROW-COL packet framing interval.
$04a_{16}$	TCDLY1	TCDLY1	read-write, 3 bits	$t_{CDLY1-C}$ core parameter. Programmable delay for read data.
$04c_{16}$	TCYCLE	TCYCLE	write-only, 14 bits	t_{CYCLE} datasheet parameter. Specifies cycle time in 64ps units.
$04b_{16}$	SKIP	AS	read-only, 1 bit	Autoskip value established by the SETF command.
		MSE	read-write, 1 bit	Manual skip enable. Allows the MS value to override the AS value.
		MS	read-write, 1 bit	Manual skip value.
$04d_{16}$	TEST77	TEST77	write-only, 16 bits	Test register.
$04e_{16}$	TEST78	TEST78	write-only, 16 bits	Test register.
$04f_{16}$	TEST79	TEST79	write-only, 16 bits	Test register.
055_{16}	TCPS	TCPS	read-write, 2 bits	t_{CPS-C} core parameter. Determines t_{OFFP}.
080_{16} - $0ff_{16}$	reserved	reserved	vendor-specific	Vendor-specific test registers. Do not read or write after SIO reset.



Read / write register.
Reset values are undefined except as affected by SIO Reset as noted below. SETR / CLRR Reset does not affect this register.

SDEVID5..0 - Serial Device Identification. Compared to SDEV5..0 serial address field of serial request packet for register read / write transactions. This determines which RDRAM devices is selected for the register read or write operation. **SDEVID resets to 3f$_{16}$.**

PSX - Power Exit Select. PDN and NAP are exited with (=0) or without (=1) a device address on the DQA5..0 pins. PDEV5 (on DQA5) selectes broadcast (1) or directed (0) exit. For a directed exit, PDEV4..0 (on DQA4..0) is compared to DEVID4..0 to select a device.

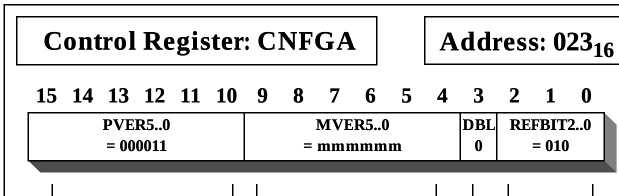
SRP - SIO Repeater. Controls value on SIO1; SIO1=SIO0 if SRP=1, SIO1=1 if SRP=0. **SRP resets to 1.**

PDN Self-Refresh. PSR=1 enables self-refresh in PDN mode. PSR can't be set while in PDN mode. **PSR resets to 0.**

Low Power Self-Refresh. LSR=1 enables longer self-refresh interval. The self-refresh supply current is reduced. **LSR resets to 0.**

RDRAM Disable. DIS=1 causes RDRAM device to ignore NAP / PDN exit sequence, DIS=0 permits normal operation. This mechanism disables an RDRAM device. **DIS resets to 0.**

Figure 27: INIT Register



Read-only register.

REFBIT2..0 - Refresh Bank Bits. Specifies the number of bank address bits used by REFA and REFP commands. Permits multi-bank refresh in future RDRAM devices.

DBL - Doubled-Bank. DBL=1 means the device uses a doubled-bank architecture with adjacent-bank dependency. DBL=0 means no dependency.

MVER5..0 - Manufacturer Version. Specifies the manufacturer identification number.

PVER5..0 - Protocol Version. Specifies the Direct Protocol version used by this device:
0 - Compliant with version 0.62
1 - Version 1
2 - Version 2 (IDM+ Version1)
3 - Version 3 (See change history for protocol change summary

Note: In RDRAM devices with protocol version 1 PVER[5:0] = 000001, the range of the PDNX field (PDNX[2:0] in the PDNX register) may not be large enough to specify the location of the restricted interval in Figure 48. In this case, the effective t_{S4} parameter must increase and no row or column packets may overlap the restricted interval. See Figure 48 and Table 17.

Figure 28: CNFGA Register

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Control Register: CNFGB **Address: 024_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVER5..0 = ssssss						CORG4..0 = 01110					SPT 0	DEVTYP2..0 = 000			BYT B

Read-only register.

BYT - Byte width. B=1 means the device reads and writes 9-bit memory bytes. B=0 means 8 bits.

DEVTYP2..0 - Device type. DEVTYP = 000 means that this device is an RDRAM device.

SPT - Split-core. SPT=1 means the core is split, SPT=0 means it is not.

CORG4..0 - Core organization. This field specifies the number of bank (two), row (thirteen), and column (seven) address bits.

SVER5..0 - Stepping version. Specifies the mask version number of this device.

Figure 29: CNFGB Register

Control Register: TEST34 **Address: 022_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write-only register.
Reset value of TEST34 is zero (from SIO Reset)
This register are used for testing purposes. It must not be read or written after SIO Reset.

Figure 30: TEST Register

Control Register: DEVID **Address: 040_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	DEVID4..DEVID0				

Read / write register.
Reset value is undefined.
Device Identification register.
DEVID4..DEVID0 is compared to DR4..DR0, DC4..DC0, and DX4..DX0 fields for all memory read or write transactions. This determines which RDRAM device is selected for the memory read or write transaction.

Figure 31: DEVID Register

Control Register: REFB — **Address: 041_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	REFB1..REFB0	

Read / write register.
Reset value is zero (from SETR / CLRR).
Refresh Bank register.
REFB1..REFB0 is the bank that will be refreshed next during self-refresh. REFB1..0 is incremented after each self-refresh activate and precharge operation pair.

Figure 32: REFB Register

Control Register: CCA — **Address: 043_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYMA0	CCA6..CCA0						

Read / write register.
Reset value is zero (SETR / CLRR or SIO Reset).
CCA6..CCA0 - Current Control A. Controls the I_{OL} output current for the DQA8..DQA0 pins.

ASYMA0 control the asymmetry of the V_{OL} / V_{OH} voltage swing about the V_{REF} reference voltage for the DQA8..0 pins:

ASYMA0	ODF	R_{DA}
0	0.00	1.00
1	0.12	0.81

where ODF is the OverDrive Factor (the extra I_{OL} current sunk by an RSL output when ASYMA0 is set) and Table 18 shows the R_{DA} parameter range, where $R_{DA} = 1 / (1+2 \bullet ODF)$

Figure 33: CCA Register

Control Register: REFR — **Address: 042_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	REFR12..REFR0												

Read / write register.
Reset value is zero (from SETR / CLRR).
Refresh Row register.
REFR12..REFR0 is the row that will be refreshed next by the REFA command or by self-refresh. REFR12..0 is incremented when BR1..0=1..1 for the REFA command. REFR12..0 is incremented when REFB1..0=1..1 for self-refresh.

Figure 34: REFR Register

Control Register: CCB — **Address: 044_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYMB0	CCB6..CCB0						

Read / write register.
Reset value is zero (SETR / CLRR or SIO Reset).
CCB6..CCB0 - Current Control B. Controls the I_{OL} output current for the DQB8..DQB0 pins.

ASYMB0 control the asymmetry of the V_{OL} / V_{OH} voltage swing about the V_{REF} reference voltage for the DQB8..0 pins:

ASYMB0	ODF	R_{DA}
0	0.00	1.00
1	0.12	0.81

where ODF is the OverDrive Factor (the extra I_{OL} current sunk by an RSL output when ASYMB0 is set) and Table 18 shows the R_{DA} parameter range, where $R_{DA} = 1 / (1+2 \bullet ODF)$

Figure 35: CCB Register

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Control Register: NAPX **Address: 045_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	DQS	NAPX4..0					NAPXA4..0				

Read / write register.
Reset value is 0525_{16} (SIO Reset)
Note - t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

NAPXA4..0 - Nap Exit Phase A. This field specifies the number of SCK cycles during the first phase for exiting NAP mode. It must satisfy:
$NAPXA \bullet t_{SCYCLE} \geq t_{NAPXA,MAX}$
Do not set this field to zero.

NAPX4..0 - Nap Exit Phase A plus B. This field specifies the number of SCK cycles during the first plus second phases for exiting NAP mode. It must satisfy:
$NAPX \bullet t_{SCYCLE} \geq NAPXA \bullet t_{SCYCLE} + t_{NAPXB,MAX}$
Do not set this field to zero.

DQS - DQ Select. This field specifies the number of SCK cycles (0 => 0.5 cycles, 1 => 1.5 cycles) between the CMD pin framing sequence and the device selection on DQ5..0. See Figure 49 - This field must be written with a “1” for this RDRAM device.

Figure 36: NAPX Register

Control Register: PDNXA **Address: 046_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PDNXA12..0												

Read / write register.
Reset value is 0008_{16} (SIO Reset)
PDNXA4..0 - PDN Exit Phase A. This field specifies the number of (64•SCK cycle) units during the first phase for exiting PDN mode. It must satisfy:
$PDNXA \bullet 64 \bullet t_{SCYCLE} \geq t_{PDNXA,MAX}$
Do not set this field to zero.
Note - only PDNXA5..0 are implemented.
Note - t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

Figure 37: PDNXA Register

Control Register: PDNX **Address: 047_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PDNX12..0												

Read / write register.
Reset value is 0004_{16} (SIO Reset)
PDNX4..0 - PDN Exit Phase A plus B. This field specifies the number of (256•SCK cycle) units during the first plus second phases for exiting PDN mode. It should satisfy:
$PDNX \bullet 256 \bullet t_{SCYCLE} \geq PDNXA \bullet 64 \bullet t_{SCYCLE} + t_{PDNXB,MAX}$
If this cannot be satisfied, then the maximum PDNX value should be written, and the t_{S4} / t_{H4} timing window will be modified (see Figure 50).
Do not set this field to zero.
Note - only PDNX2..0 are implemented.
Note - t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

Figure 38: PDNX Register

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Control Register: TPARM **Address: 048_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	TCDLY0			TCLS		TCAS	

Read / write register.
Reset value is undefined.
TCAS1..0 - Specifies the t_{CAS-C} core parameter in t_{CYCLE} units. This should be "10" ($2 \bullet t_{CYCLE}$).

TCLS1..0 - Specifies the t_{CLS-C} core parameter in t_{CYCLE} units. Should be "10" ($2 \bullet t_{CYCLE}$).

TCDLY0 - Specifies the $t_{CDLY0-C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values "010" ($2 \bullet t_{CYCLE}$) through "101" ($5 \bullet t_{CYCLE}$).

The equations relating the core parameters to the datasheet parameters follow:

$t_{CAS-C} = 2 \bullet t_{CYCLE}$
$t_{CLS-C} = 2 \bullet t_{CYCLE}$
$t_{CPS-C} = 1 \bullet t_{CYCLE}$ or $2 \bullet t_{CYCLE}$

$t_{OFFP} = t_{CPS-C} + t_{CAS-C} + t_{CLS-C} - 1 \bullet t_{CYCLE}$
$= 4 \bullet t_{CYCLE}$ or $5 \bullet t_{CYCLE}$

$t_{RCD} = t_{RCD-C} + 1 \bullet t_{CYCLE} - t_{CLS-C}$
$= t_{RCD-C} - 1 \bullet t_{CYCLE}$

$t_{CAC} = 3 \bullet t_{CYCLE} + t_{CLS-C} + t_{CDLY0-C} + t_{CDLY1-C}$
(see table below for programming ranges)

TCDLY0	$t_{CDLY0-C}$	TCDLY1	$t_{CDLY1-C}$	t_{CAC} @ t_{CYCLE} = 3.3ns	t_{CAC} @ t_{CYCLE} = 2.5ns	t_{CAC}@t_{CYCLE}=1.875ns
010	$2 \bullet t_{CYCLE}$	000	$0 \bullet t_{CYCLE}$	$7 \bullet t_{CYCLE}$	not allowed	not allowed
011	$3 \bullet t_{CYCLE}$	000	$0 \bullet t_{CYCLE}$	$8 \bullet t_{CYCLE}$	$8 \bullet t_{CYCLE}$	not allowed
011	$3 \bullet t_{CYCLE}$	001	$1 \bullet t_{CYCLE}$	$9 \bullet t_{CYCLE}$	$9 \bullet t_{CYCLE}$	not allowed
100	$4 \bullet t_{CYCLE}$	000	$0 \bullet t_{CYCLE}$	$9 \bullet t_{CYCLE}$	$9 \bullet t_{CYCLE}$	$9 \bullet t_{CYCLE}$
011	$3 \bullet t_{CYCLE}$	010	$2 \bullet t_{CYCLE}$	$10 \bullet t_{CYCLE}$	$10 \bullet t_{CYCLE}$	not allowed
100	$4 \bullet t_{CYCLE}$	001	$1 \bullet t_{CYCLE}$	$10 \bullet t_{CYCLE}$	$10 \bullet t_{CYCLE}$	$10 \bullet t_{CYCLE}$
100	$4 \bullet t_{CYCLE}$	010	$2 \bullet t_{CYCLE}$	$11 \bullet t_{CYCLE}$	$11 \bullet t_{CYCLE}$	$11 \bullet t_{CYCLE}$
101	$5 \bullet t_{CYCLE}$	010	$2 \bullet t_{CYCLE}$	$12 \bullet t_{CYCLE}$	$12 \bullet t_{CYCLE}$	$12 \bullet t_{CYCLE}$

Figure 39: TPARM Register

Control Register: TFRM **Address: 049_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TFRM3..0			

Read / write register.
Reset value is undefined.
TFRM3..0 - Specifies the position of the framing point in t_{CYCLE} units. This value must be greater than or equal to the $t_{FRM,MIN}$ parameter. This is the minimum offset between a ROW packet (which places a device at ATTN) and the first COL packet (directed to that device) which must be framed. This field may be written with the values "0111" ($7 \bullet t_{CYCLE}$) through "1010" ($10 \bullet t_{CYCLE}$). TFRM is usually set to the value which matches the largest $t_{RCD,MIN}$ parameter (modulo $4 \bullet t_{CYCLE}$) that is present in an RDRAM device in the memory system. Thus, if an RDRAM device with $t_{RCD,MIN} = 11 \bullet t_{CYCLE}$ were present, then TFRM would be programmed to $7 \bullet t_{CYCLE}$.

Figure 40: TFRM Register

Control Register: TCDLY1 **Address: $04a_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	TCDLY1		

Read / write register.
Reset value is undefined.
TCDLY1 - Specifies the value of the $t_{CDLY1-C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values "000" ($0 \bullet t_{CYCLE}$) through "010" ($2 \bullet t_{CYCLE}$). Refer to Figure 39 for more details.

Figure 41: TCDLY1 Register

Control Register: SKIP — **Address: $04b_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	AS	MSE	MS	0	0	0	0	0	0	0	0	0	0

Read / write register (except AS field).
Reset value is zero (SIO Reset).
AS - Autoskip. Read-only value determined by autoskip circuit and stored when SETF serial command is received by RDRAM device during initialization. In figure 58, AS=1 corresponds to the early Q(a1) packet and AS=0 to the Q(a1) packet one t_{CYCLE} later for the four uncertain cases.
MSE - Manual skip enable (0=auto, 1=manual).

Figure 42: SKIP Register

Control Register: TEST77 — **Address: $04d_{16}$**
Control Register: TEST78 — **Address: $04e_{16}$**
Control Register: TEST79 — **Address: $04f_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write-only registers.
Reset value of TEST77, 78, 79 is zero (SIO Reset).
Do not read or write TEST77, 78, 79 after SIO reset.
These registers must only be used for testing purposes. They must not be read or written after SIO reset.

Figure 43: TEST Registers

Control Register: TCYCLE — **Address: $04c_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	TCYCLE13..TCYCLE0													

Write-only register.
Reset value is undefined
TCYCLE13..0 - Specifies the value of the t_{CYCLE} datasheet parameter in 64ps units. For the $t_{CYCLE,MIN}$ of 2.5ns (2500ps), this field should be written with the value “00027_{16}” (39•64ps).

Figure 44: TCYCLE Register

Control Register: TCPS — **Address: 055_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCPS	

Read / write register.
Reset value is 0001^{16} (SIO Reset).
TCPS - Specifies the value of the $t_{CPS\text{-}C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to t_{OFFP}. This field may be written with the values “01” (1•t_{CYCLE}) through “11” (3•t_{CYCLE}). Refer to Figure 39 for more details.

Figure 45: Control Register

Power State Management

Table 16 summarizes the power states available to a RDRAM device. In general, the lowest power states have the longest operational latencies. For example, the relative power levels of PDN state and STBY state have a ratio of about 1:110, and the relative access latencies to get read data have a ratio of about 250:1.

PDN state is the lowest power state available. The information in the RDRAM core is usually maintained with self-refresh; an internal timer automatically refreshes all rows of all banks. PDN has a relatively long exit latency because the TCLK/RCLK block must resynchronize itself to the external clock signal.

NAP state is another low-power state in which either self-refresh or REFA-refresh are used to maintain the core. See "Refresh" on page 42 for a description of the two refresh mechanisms. NAP has a shorter exit latency than PDN because the TCLK/RCLK block maintains its synchronization state relative to the external clock signal at the time of NAP entry. This imposes a limit (t_{NLIMIT}) on how long an RDRAM device may remain in NAP state before briefly returning to STBY or ATTN to update this synchronization state.

Table 16: Power State Summary

Power State	Description	Blocks consuming power	Power State	Description	Blocks consuming power
PDN	Powerdown state.	Self-refresh	NAP	Nap state. Similar to PDN except lower wake-up latency.	Self-refresh or REFA-refresh TCLK/RCLK-Nap
STBY	Standby state. Ready for ROW packets.	REFA-refresh TCLK/RCLK ROW demux receiver	ATTN	Attention state. Ready for ROW and COL packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver
ATTNR	Attention read state. Ready for ROW and COL packets. Sending Q (read data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ mux transmitter Core power	ATTNW	Attention write state. Ready for ROW and COL packets. Ready for D (write data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ demux receiver Core power

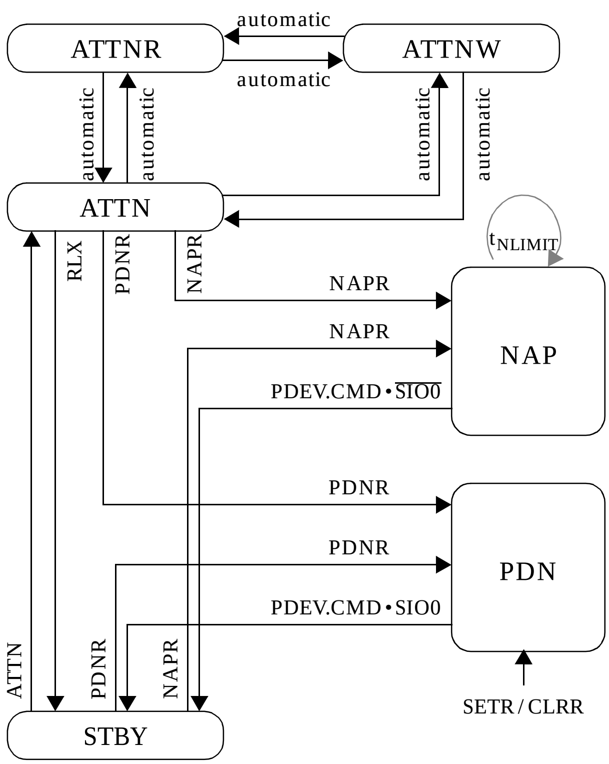
Figure 46 summarizes the transition conditions needed for moving between the various power states. At initialization, the SETR/CLRR Reset sequence will put the RDRAM device into PDN state. The PDN exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins.

Once the RDRAM device is in STBY, it will move to the ATTN/ATTNR/ATTNW states when it receives a non-broadcast ROWA packet or non-broadcast ROWR packet with the ATTN command. The RDRAM device returns to STBY from these three states when it receives a RLX command. Alternatively, it may enter NAP or PDN state from ATTN or STBY states with a NAPR or PDNR command in an ROWR packet. The PDN or NAP exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins. The RDRAM device returns to the STBY state when exiting NAP or PDN.

An RDRAM device may only remain in NAP state for a time t_{NLIMIT}. It must periodically return to ATTN or STBY.

The NAPRC command causes a napdown operation if the RDRAM device's NCBIT is set. The NCBIT is not directly visible. It is undefined on reset. It is set by a NAPR command to the RDRAM device, and it is cleared by an ACT command to the RDRAM device. It permits a controller to manage a set of RDRAM devices in a mixture of power states.

STBY state is the normal idle state of the RDRAM device. In this state all banks and sense amps have usually been left precharged and ROWA and ROWR packets on the ROW pins are being monitored. When a non-broadcast ROWA packet or non-broadcast ROWR packet (with the ATTN command) packet addressed to the RDRAM device is seen, the RDRAM device enters ATTN state (see the right side of Figure 47). This requires a time t_{SA} during which the RDRAM device activates the specified row of the specified bank. A time TFRM • t_{CYCLE} after the ROW packet, the RDRAM device will be able to frame COL packets (TFRM is a control register field - see Figure 40). Once in ATTN state, the RDRAM device will automatically transition to the ATTNW and ATTNR states as it receives WR and RD commands.



Notation:
SETR / CLRR - SETR / CLRR Reset sequence in SRQ packets
PDNR - PDNR command in ROWR packet
NAPR - NAPR command in ROWR packet
RLXR - RLX command in ROWR packet
RLX - RLX command in ROWR,COLC,COLX packets
SIO0 - SIO0 input value
PDEV.CMD - (PDEV=DEVID) • (CMD=01)
ATTN - ROWA packet (non-broadcast) or ROWR packet (non-broadcast) with ATTN command

Figure 46: Power State Transition Diagram

Once the RDRAM device is in ATTN, ATTNW, or ATTNR states, it will remain there until it is explicitly returned to the STBY state with a RLX command. A RLX command may be given in an ROWR, COLC , or COLX packet (see the left side of Figure 47). It is usually given after all banks of the RDRAM device have been precharged; if other banks are still activated, then the RLX command would probably not be given.

If a broadcast ROWA packet or ROWR packet (with the ATTN command) is received, the RDRAM device's power state doesn't change. If a broadcast ROWR packet with RLXR command is received, the RDRAM device goes to STBY.

Figure 48 shows the NAP entry sequence (left). NAP state is entered by sending a NAPR command in a ROW packet. A time t_{ASN} is required to enter NAP state (this specification is provided for power calculation purposes). The clock on CTM / CFM must remain stable for a time t_{CD} after the NAPR command.

The RDRAM device may be in ATTN or STBY state when the NAPR command is issued. When NAP state is exited, the RDRAM device will return to STBY. After a NAP exit, the RDRAM device may consume power as if it is in ATTN state until a RLX command is received.

Figure 48 also shows the PDN entry sequence (right). PDN state is entered by sending a PDNR command in a ROW packet. A time t_{ASP} is required to enter PDN state (this specification is provided for power calculation purposes). The clock on CTM / CFM must remain stable for a time t_{CD} after the PDNR command.

The RDRAM device may be in ATTN or STBY state when the PDNR command is issued. When PDN state is exited, the RDRAM device will return to STBY. After a PDN exit, the RDRAM device may consume power as if it is in ATTN state until a RLX command is received. Also, the current- and slew-rate-control levels must be re-established.

The RDRAM device's write buffer must be retired with the appropriate COP command before NAP or PDN are entered. Also, all the RDRAM device's banks must be precharged before NAP or PDN are entered. The exception to this is if NAP is entered with the NSR bit of the INIT register cleared (disabling self-refresh in NAP). The commands for relaxing, retiring, and precharging may be given to the RDRAM device as late as the ROPa0, COPa0, and XOPa0 packets in Figure 48. No broadcast packets nor packets directed to the RDRAM device entering Nap or PDN may overlay the quiet window. This window extends for a time t_{NPQ} after the packet with the NAPR or PDNR command.

Figure 49 shows the NAP and PDN exit sequences. These sequences are virtually identical; the minor differences will be highlighted in the following description.

Before NAP or PDN exit, the CTM / CFM clock must be stable for a time t_{CE}. Then, on a falling and rising edge of SCK, if there is a "01" on the CMD input, NAP or

PDN state will be exited. Also, on the falling SCK edge the SIO0 input must be at a 0 for NAP exit and 1 for PDN exit.

If the PSX bit of the INIT register is 0, then a device PDEV5..0 is specified for NAP or PDN exit on the DQA5..0 pins. This value is driven on the rising SCK edge 0.5 or 1.5 SCK cycles after the original falling edge, depending upon the value of the DQS bit of the NAPX register. If the PSX bit of the INIT register is 1, then the RDRAM device ignores the PDEV5..0 address packet and exits NAP or PDN when the wake-up sequence is presented on the CMD wire. The ROW and COL pins must be quiet at a time t_{S4}/t_{H4} around the indicated falling SCK edge (timed with the PDNX or NAPX register fields). After that, ROW packets may be directed to the RDRAM device which is now in STBY state.

Figure 50 shows the constraints for entering and exiting NAP and PDN states. On the left side, an RDRAM device exits NAP state at the end of cycle T_3. This RDRAM device may not re-enter NAP or PDN state for an interval of t_{NU0}. The RDRAM device enters NAP state at the end of cycle T_{12}. This RDRAM device may not re-exit NAP state for an interval of t_{NU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. NAPX is the value in the NAPX field in the NAPX register.

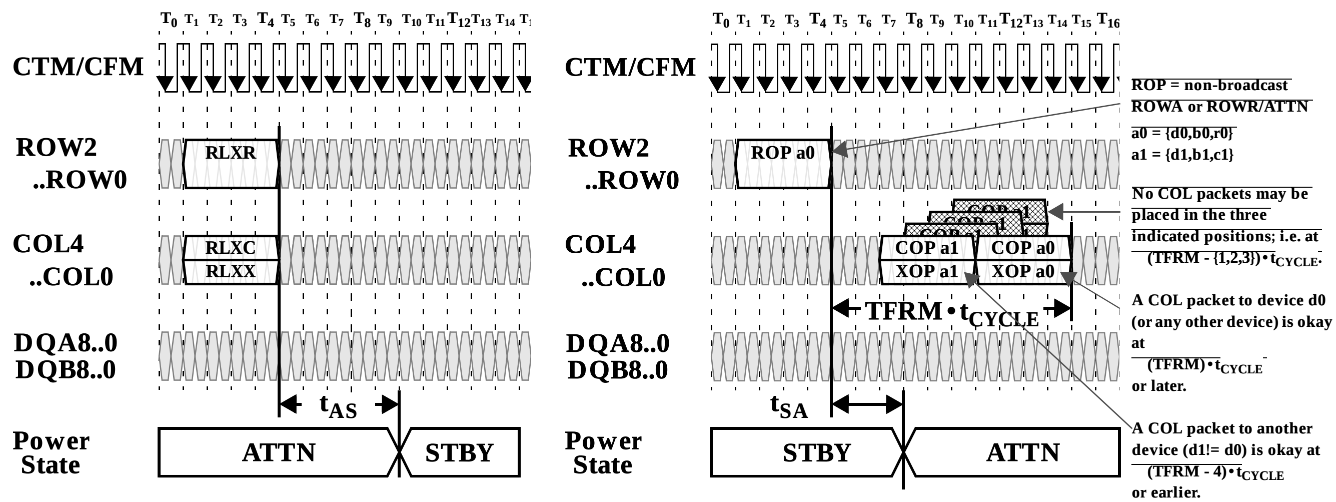
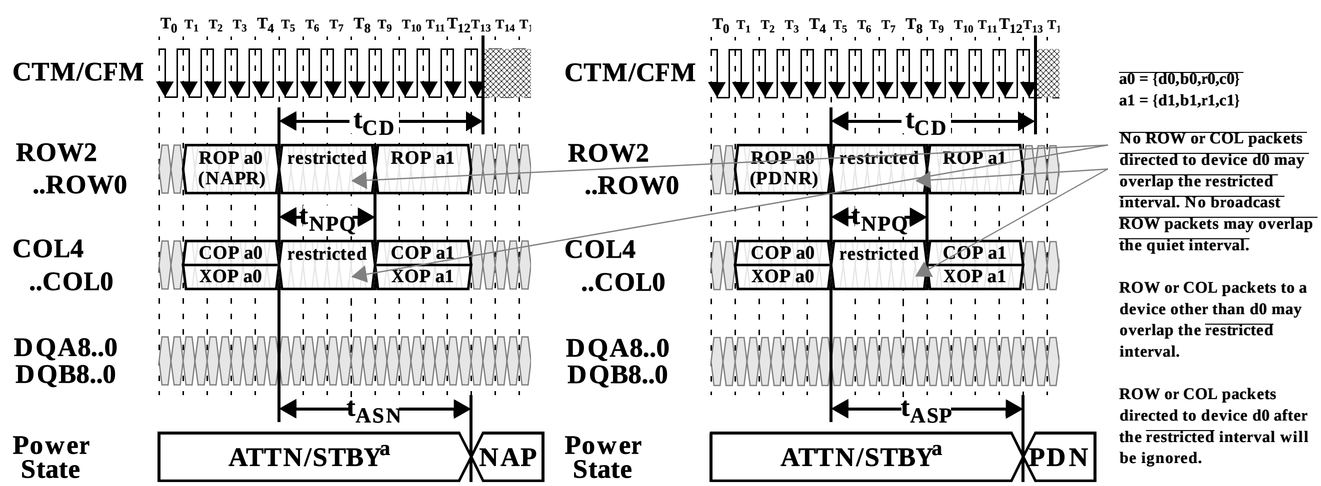


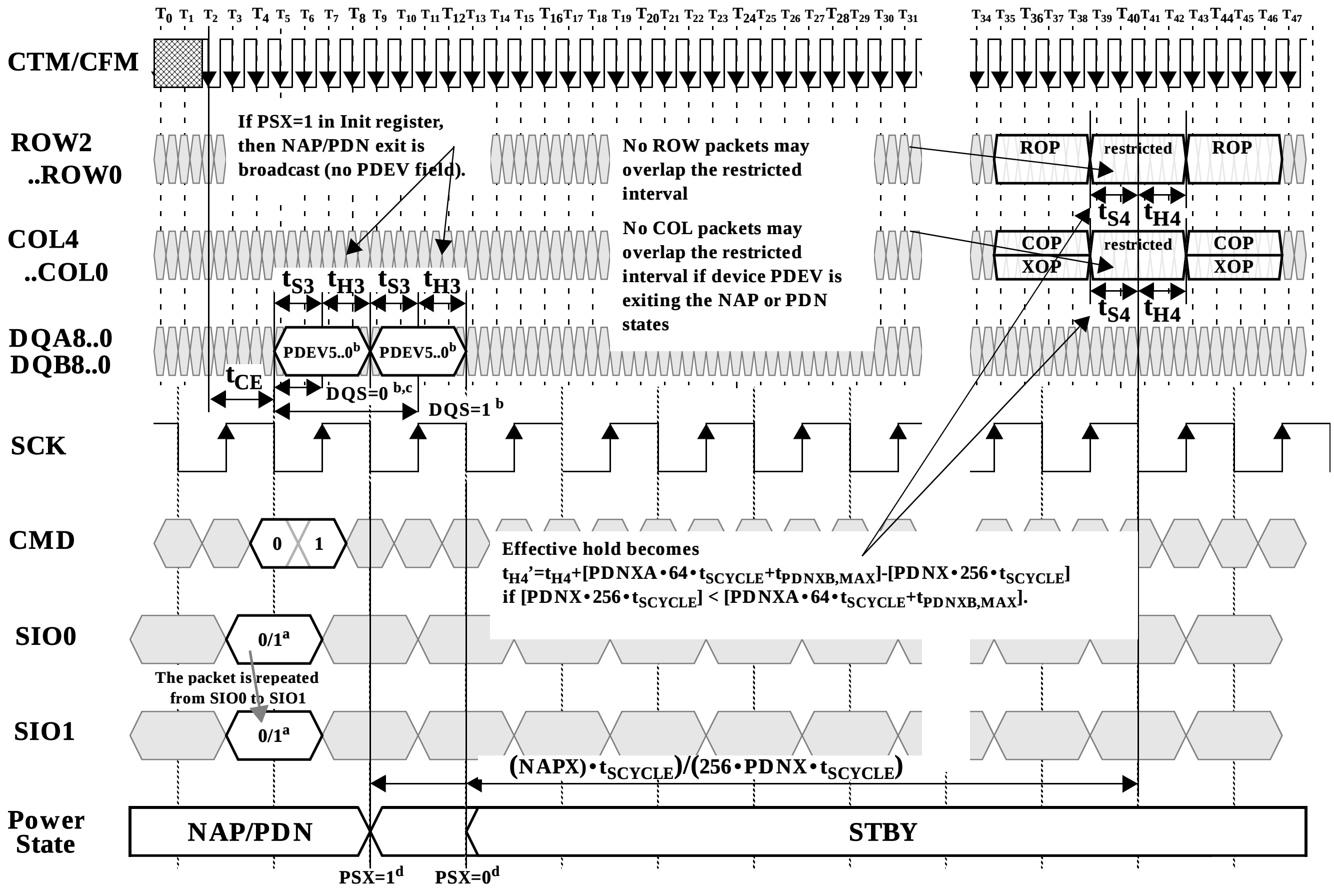
Figure 47: STBY Entry (left) and STBY Exit (right)



[a] The (eventual) NAP/PDN exit will be to the same ATTN/STBY state the RDRAM device was in prior to NAP/PDN entry

Figure 48: NAP Entry (left) and PDN Entry (right)

On the right side of Figure 49, an RDRAM device exits PDN state at the end of cycle T_3. This RDRAM device may not re-enter PDN or NAP state for an interval of t_{PU0}. The RDRAM device enters PDN state at the end of cycle T_{13}. This RDRAM device may not re-exit PDN state for an interval of t_{PU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. PDNX is the value in the PDNX field in the PDNX register.



[a] Use 0 for NAP exit, 1 for PDN exit

[b] Device selection timing slot is selected by DQS field of NAPX register

[c] The DQS field must be written with “1” for this RDRAM device.

[d] The PSX field determines the start of NAP/PDN exit .

Figure 49: NAP and PDN Exit

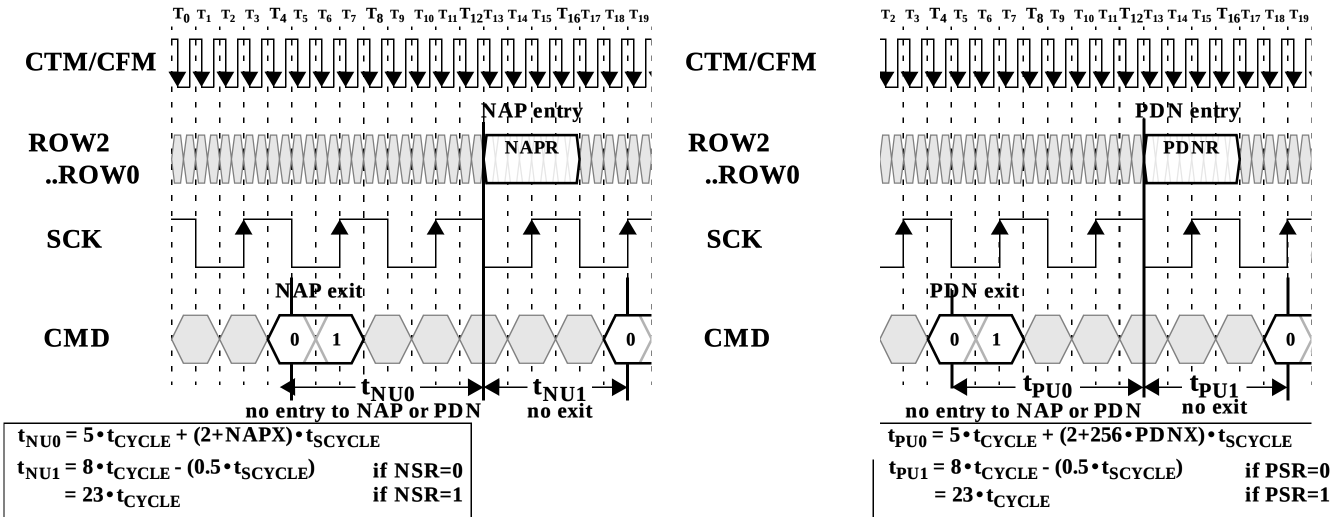


Figure 50: NAP Entry/Exit Windows (left) and PDN Entry/Exit Windows (right)

Refresh

RDRAM devices, like any other DRAM technology, use volatile storage cells which must be periodically refreshed. This is accomplished with the REFA command. Figure 50 shows an example of this.

The REFA command in the transaction is typically a broadcast command (DR4T and DR4F are both set in the ROWR packet), so that in all devices bank number Ba is activated with row number REFR, where REFR is a control register in the RDRAM device. When the command is broadcast and ATTN is set, the power state of the RDRAM devices (ATTN or STBY) will remain unchanged. The controller increments the bank address Ba for the next REFA command. When Ba is equal to its maximum value, the RDRAM device automatically increments REFR for the next REFA command.

On average, these REFA commands are sent once every $t_{REF} / 2^{BBIT+RBIT}$ (where BBIT are the number of bank address bits and RBIT are the number of row address bits) so that each row of each bank is refreshed once every t_{REF} interval.

The REFA command is equivalent to an ACT command, in terms of the way that it interacts with other packets (see Table 9). In the example, an ACT command is sent after t_{RR} to address b0, a different (non-adjacent) bank than the REFA command.

A second ACT command can be sent after a time t_{RC} to address c0, the same bank (or an adjacent bank) as the REFA command.

Note that a broadcast REFP command is issued a time t_{RAS} after the initial REFA command in order to precharge the refreshed bank in all RDRAM devices. After a bank is given a REFA command, no other core operations (activate or precharge) should be issued to it until it receives a REFP.

It is also possible to interleave refresh transactions (not shown). In the figure, the ACT b0 command would be replaced by a REFA b0 command. The b0 address would be broadcast to all devices, and would be {Broadcast,Ba+2,REFR}. Note that the bank address should skip by two to avoid adjacent bank interference. A possible bank incrementing pattern would be: {0,2,1,3}. Every time bank 3 is reached, the REFA command would automatically increment the REFR register.

A second refresh mechanism is available for use in PDN and NAP power states. This mechanism is called self-refresh mode. When the PDN power state is entered, or when NAP power state is entered with the NSR control register bit set, then self-refresh is automatically started for the RDRAM device.

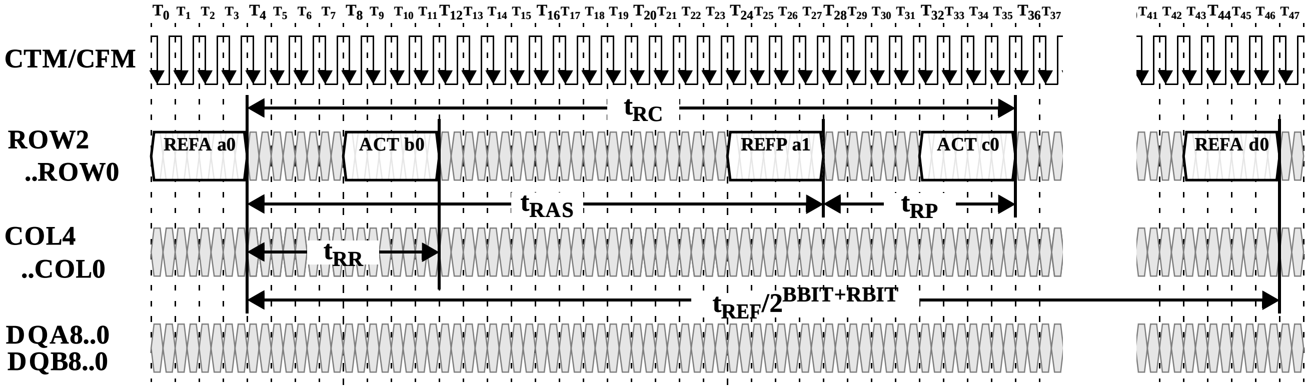
Self-refresh uses an internal time base reference in the RDRAM device. This causes an activate and precharge to be carried out once in every $t_{REF} / 2^{BBIT+RBIT}$ interval. The REFB and REFR control registers are used to keep track of the bank and row being refreshed.

Before a controller places an RDRAM device into self-refresh mode, it should perform REFA / REFP refreshes until the bank address is equal to the last value (this will be 3). This ensures that no rows are skipped. Likewise, when a controller returns an RDRAM device to REFA / REFP refresh, it should start with the first bank address value (0 for the example sequence).

Note that for this RDRAM device, the upper bank address bits are not used. These bits should be set to “0..0” in all bank address fields, but with one exception. When REFA and REFP commands are specified in ROWR packets, it will be necessary to set the upper bank bits to values other than “0..0” when other RDRAM devices with more banks are present on the Channel.

Figure 51 illustrates the requirement imposed by the t_{BURST} parameter. After PDN or NAP (when self-refresh is enabled) power states are exited, the controller must refresh all banks of the RDRAM device once during the interval t_{BURST} after the restricted interval on the ROW and COL buses. This will ensure that regardless of the state of self-refresh during PDN or NAP, the $t_{REF,MAX}$ parameter is met for all banks. During the t_{BURST} interval, the banks may be refreshed in a single burst, or they may be scattered throughout the interval. Note that the first and last banks to be refreshed in the t_{BURST} interval are numbers 0 and 3, in order to match the example refresh sequence.

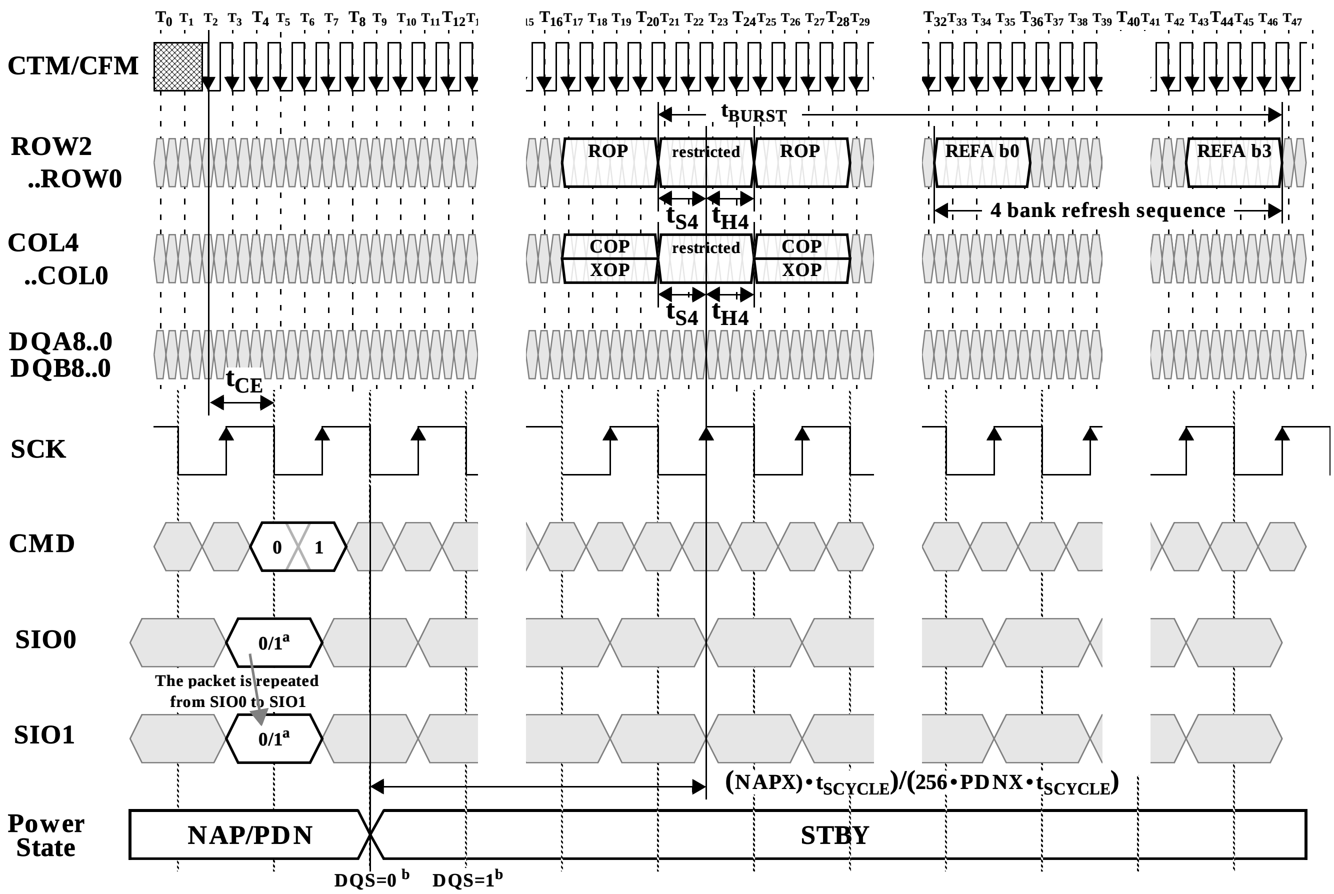
Refresh (continued)



Transaction a: REFA	a0 = {Broadcast,Ba,REFR}	a1 = {Broadcast,Ba}
Transaction b: xx	b0 = {Db, /={Ba}, Rb}	
Transaction c: xx	c0 = {Dc, ==Ba, Rc}	
Transaction d: REFA	d0 = {Broadcast,Ba+1,REFR}	

BBIT = # bank address bits
RBIT = # row address bits
REFB = REFB1..REFB0
REFR = REFR11..REFR0

Figure 51: REFA/REFP Refresh Transaction Example



[a] Use 0 for NAP exit, 1 for PDN exit

Figure 52: NAP/PDN Exit - t_{BURST} Requirement

Current and Temperature Control

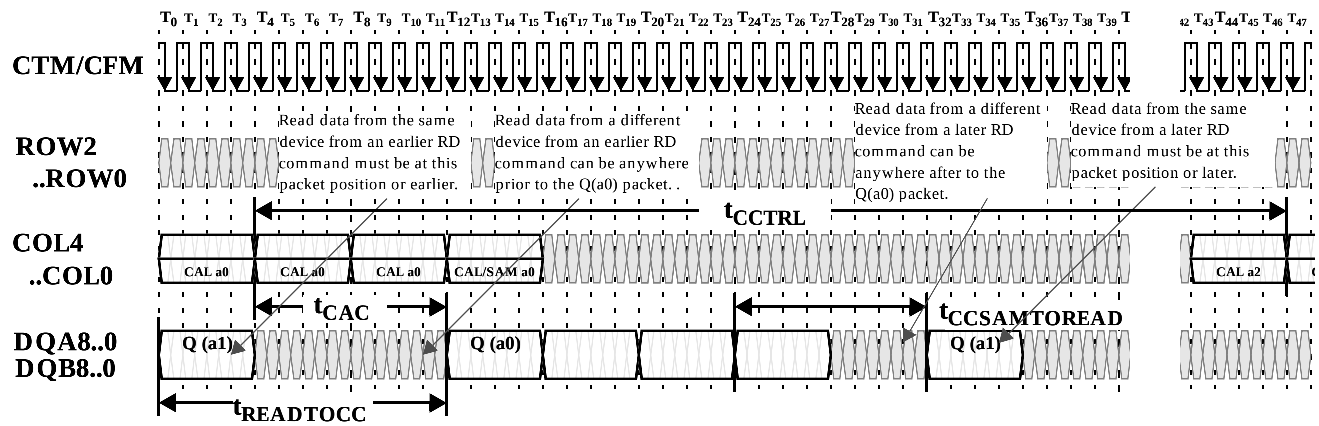
Figure 53 shows an example of a transaction which performs current control calibration. It is necessary to perform this operation once to every RDRAM in every t_{CCTRL} interval in order to keep the I_{OL} output current in its proper range.

This example uses four COLX packets with a CAL command. These cause the RDRAM to drive four calibration packets Q(a0) a time t_{CAC} later. An offset of t_{RDTOCC} must be placed between the Q(a0) packet and read data Q(a1)from the same device. These calibration packets are driven on the DQA4..3 and DQB4..3 wires. The TSQ bit of the INIT register is driven on the DQA5 wire during same interval as the calibration packets. The remaining DQA and DQB wires are not used during these calibration packets. The last COLX packet also contains a SAM command (concatenated with the CAL command). The RDRAM samples the last calibration packet and adjusts its I_{OL} current value.

Unlike REF commands, CAL and SAM commands cannot be broadcast. This is because the calibration packets from different devices would interfere. Therefore, a current control transaction must be sent every t_{CCTRL} / N, where N is the number of RDRAMs on the Channel. The device field Da of the address a0 in the CAL / SAM command should be incremented after each transaction.

Figure 54 shows an example of a temperature calibration sequence to the RDRAM. This sequence is broadcast once every t_{TEMP} interval to all the RDRAMs on the Channel. The TCEN and TCAL are ROP commands, and cause the slew rate of the output drivers to adjust for temperature drift. During the quiet interval $t_{TCQUIET}$ the devices being calibrated can’t be read, but they can be written

Current and Temperature (con't)



Transaction a0: CAL/SAM	a0 = {Da, Bx}
Transaction a1: RD	a1 = {Da, Bx}
Transaction a2: CAL/SAM	a2 = {Da, Bx}

Figure 53: Current Control CAL/SAM Transaction Example

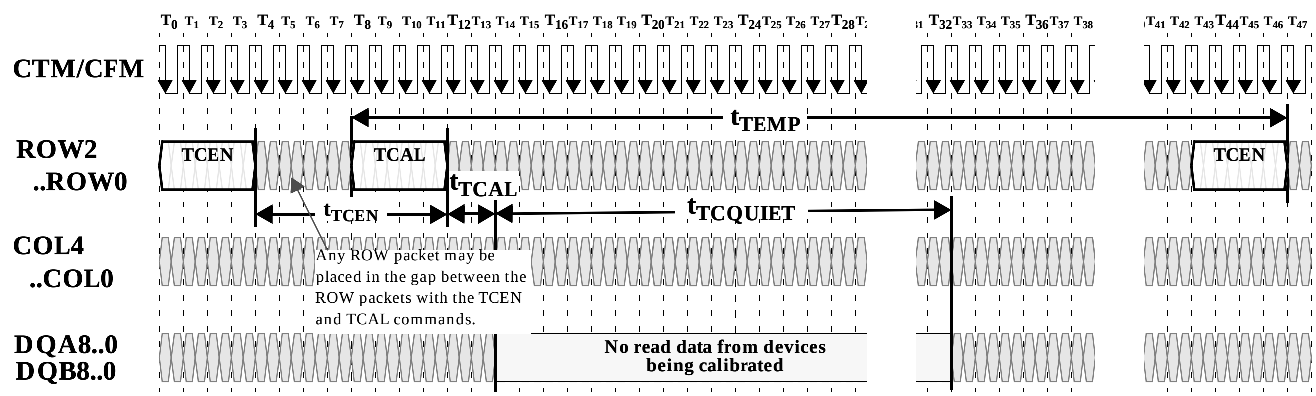


Figure 54: Temperature Calibration (TCEN-TCAL) Transactions to RDRAM

Timing Conditions

Table 17: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{CYCLE}	CTM and CFM cycle times (-600) CTM and CFM cycle times (-800) CTM and CFM cycle times (-1066)	3.33 2.50 1.875	3.33 3.33 3.33	ns ns ns	Figure 55 Figure 55 Figure 55
t_{CR}, t_{CF}	CTM and CFM input rise and fall times. Use the minimum value of these parameters during testing.	0.2	0.5	ns	Figure 55
t_{CH}, t_{CL}	CTM and CFM high and low times	40%	60%	t_{CYCLE}	Figure 55
t_{TR}	CTM-CFM differential (MSE / MS=0 / 0) CTM-CFM differential (MSE / MS=1 / 1)[a]	0.0 0.9	1.0 1.0	t_{CYCLE}	Figure 42 Figure 55
t_{DCW}	Domain crossing window	-0.1	0.1	t_{CYCLE}	Figure 61
t_{DR}, t_{DF}	DQA / DQB / ROW / COL input rise / fall times (20% to 80%). Use the minimum value of these parameters during testing. @ t_{CYCLE}=3.33ns @ t_{CYCLE}=2.50ns @ t_{CYCLE}=1.875ns	 0.2 0.2 0.2	 0.65 0.65 0.45	 ns ns ns	 Figure 56 Figure 56 Figure 56
t_S, t_H	DQA / DQB / ROW / COL-to-CFM set / hold @ t_{CYCLE}=3.33ns DQA / DQB / ROW / COL-to-CFM set / hold @ t_{CYCLE}=2.50ns DQA / DQB / ROW / COL-to-CFM set / hold @t_{CYCLE}=1.875ns	0.275[b,d] 0.200[c,d] 0.160[d]	- - -	ns ns ns	Figure 56 Figure 56 Figure 56
t_{DR1}, t_{DF1}	SIO0, SIO1 input rise and fall times	-	5.0	ns	Figure 58
t_{DR2}, t_{DF2}	CMD, SCK input rise and fall times	-	2.0	ns	Figure 58
t_{CYCLE1}	SCK cycle time - Serial control register transactions	1000	-	ns	Figure 58
	SCK cycle time - Power transitions @ t_{CYCLE}=3.33ns SCK cycle time - Power transitions @ t_{CYCLE}=2.50ns SCK cycle time - Power transitions @ t_{CYCLE}=1.875ns	10 10 7.5	- - -	ns ns ns	Figure 58 Figure 58 Figure 58
t_{CH1}, t_{CL1}	SCK high and low times @ t_{CYCLE}=3.33ns SCK high and low times @ t_{CYCLE}=2.50ns SCK high and low times @ t_{CYCLE}=1.875ns	4.25 4.25 3.5	- - -	ns ns ns	Figure 58 Figure 58 Figure 58
t_{S1}	CMD setup time to SCK rising or falling edge[e] @ t_{CYCLE}=3.33ns @ t_{CYCLE}=2.50ns @ t_{CYCLE}=1.875ns	 1.25 1.25 1.0	 - - -	 ns ns ns	 Figure 58 Figure 58 Figure 58
t_{H1}	CMD hold time to SCK rising or falling edge[f] @ t_{CYCLE}=3.33ns @ t_{CYCLE}=2.50ns @ t_{CYCLE}=1.875ns	 1.0 1.0 1.0	 - - -	 ns ns ns	 Figure 58 Figure 58 Figure 58
t_{S2}	SIO0 setup time to SCK falling edge	40	-	ns	Figure 58
t_{H2}	SIO0 hold time to SCK falling edge	40	-	ns	Figure 58
t_{S3}	PDEV setup time on DQA5..0 to SCK rising edge.	0	-	ns	Figure 48, Figure 59
t_{H3}	PDEV hold time on DQA5..0 to SCK rising edge.	5.5	-	ns	
t_{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	t_{CYCLE}	Figure 48
t_{H4}	ROW2..0, COL4..0 hold time for quiet window[g]	5	-	t_{CYCLE}	Figure 48

Table 17: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{NPQ}	Quiet on ROW / COL bits during NAP / PDN entry	4	-	t_{CYCLE}	Figure 47
$t_{READTOCC}$	Offset between read data and CC packets (same device)	12	-	t_{CYCLE}	Figure 53
$t_{CCSAMTOREAD}$	Offset between CC packet and read data (same device)	8	-	t_{CYCLE}	Figure 53
t_{CE}	CTM / CFM stable before NAP / PDN exit	2	-	t_{CYCLE}	Figure 48
t_{CD}	CTM / CFM stable after NAP / PDN entry	100	-	t_{CYCLE}	Figure 47
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	-	t_{CYCLE}	Figure 46
t_{NLIMIT}	Maximum time in NAP mode		10.0	µs	Figure 45
t_{REF}	Refresh interval		32	ms	Figure 51
t_{BURST}	Interval after PDN or NAP (with self-refresh) exit in which all banks of the RDRAM must be refreshed at least once.		200	µs	Figure 52
t_{CCTRL}	Current control interval	34 t_{CYCLE}	100ms	ms / t_{CYCLE}	Figure 53
t_{TEMP}	Temperature control interval		100	ms	Figure 54
t_{TCEN}	TCE command to TCAL command	150	-	t_{CYCLE}	Figure 54
t_{TCAL}	TCAL command to quiet window	2	2	t_{CYCLE}	Figure 54
$t_{TCQUIET}$	Quiet window (no read data)	140	-	t_{CYCLE}	Figure 54
t_{PAUSE}	RDRAM delay (no RSL operations allowed)		200.0	µs	page 28

a. MSE / MS are fields of the SKIP register. For this combination (skip override) the tDCW parameter range is effectively 0.0 to 0.0.
b. This parameter also applies to a -800 or -1066 part when operated with t_{CYCLE}=3.33ns.
c. This parameter also applies to a -1066 part when operated with t_{CYCLE}=2.50ns.
d. $t_{S,MIN}$ and $t_{H,MIN}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.
e. With $V_{IL,CMOS}$=0.5V_{CMOS}-0.4V and $V_{IH,CMOS}$=0.5V_{CMOS}+0.4V
f. With $V_{IL,CMOS}$=0.5V_{CMOS}-0.4V and $V_{IH,CMOS}$=0.5V_{CMOS}+0.4V
g. Effective hold becomes t_{H4}'=t_{H4}+[PDNXA•64•t_{SCYCLE}+$t_{PDNXB,MAX}$]-[PDNX•256•t_{SCYCLE}]
if [PDNX•256•t_{SCYCLE}] < [PDNXA•64•t_{SCYCLE}+$t_{PDNXB,MAX}$]. See Figure 48.

Electrical Conditions

Table 18: Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
T_J	Junction temperature under bias	manufacturer-specific values		°C
V_{DD}, V_{DDA}	Supply voltage (2.5v component) Supply voltage (1.8v component)	2.50 - 0.13 1.8 - 0.09	2.50 + 0.13 1.8 + 0.09	V V
$V_{DD,N}$, $V_{DDA,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMIT})	-	2.0	%
$v_{DD,N}$, $v_{DDA,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMIT})	-2.0	2.0	%
V_{CMOS}[a]	Supply voltage for CMOS pins (2.5V controllers) Supply voltage for CMOS pins (1.8V controllers)	V_{DD} 1.80 - 0.1	V_{DD} 1.80 + 0.2	V V
V_{REF}	Reference voltage	1.40 - 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input - low voltage @ t_{CYCLE}=3.33ns RSL data input - low voltage @ t_{CYCLE}=2.50ns RSL data input - low voltage @ t_{CYCLE}=1.875ns	V_{REF} - 0.5 V_{REF} - 0.5 V_{REF} - 0.5	V_{REF} - 0.2 V_{REF} - 0.2 V_{REF} - 0.15	V V V
V_{DIH}	RSL data input - high voltage[b] @ t_{CYCLE}=3.33ns RSL data input - high voltage[b] @ t_{CYCLE}=2.50ns RSL data input - high voltage[b] @ t_{CYCLE}=1.875ns	V_{REF} +0.2 V_{REF} +0.2 V_{REF} +0.15	V_{REF} +0.5 V_{REF} +0.5 V_{REF} +0.5	V V V
R_{DA}	RSL data asymmetry: $R_{DA} = (V_{DIH} - V_{REF}) / (V_{REF} - V_{DIL})$	0.67	1.00	-
V_{CM}	RSL clock input - common mode $V_{CM} = (V_{CIH}+V_{CIL})/2$	1.3	1.8	V
$V_{CIS,CTM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CTM,CTMN pins).	0.35	1.00	V
$V_{CIS,CFM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CFM,CFMN pins).	0.225	1.00	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3[c]	$V_{CMOS}/2$ - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$V_{CMOS}/2$ + 0.25	V_{CMOS}+0.3[d]	V

a. V_{CMOS} must remain on as long as V_{DD} is applied and cannot be turned off.
b. V_{DIH} is typically equal to V_{TERM} (1.8V±0.1V) under DC conditions in a system.
c. Voltage undershoot is limited to -0.7V for a duration of less than 5ns.
d. Voltage overshoot is limited toV_{CMOS} +0.7V for a duration of less than 5ns

Timing Characteristics

Table 19: Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_Q	CTM-to-DQA / DQB output time @ t_{CYCLE}=3.33ns CTM-to-DQA / DQB output time @ t_{CYCLE}=2.50ns CTM-to-DQA / DQB output time @ t_{CYCLE}=1.875ns	-0.350[a,c] -0.260[c] -0.195	+0.350[a,c] +0.260[b,c] +0.195[c]	ns ns ns	Figure 57 Figure 57 Figure 57
t_{QR}, t_{QF}	DQA / DQB output rise and fall times @ t_{CYCLE}=3.33ns DQA / DQB output rise and fall times @ t_{CYCLE}=2.50ns DQA / DQB output rise and fall times @ t_{CYCLE}=1.875ns	0.2 0.2 0.2	0.45 0.45 0.32	ns ns ns	Figure 57 Figure 57 Figure 57
t_{Q1}	SCK(neg)-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read data valid).	-	10	ns	Figure 60
t_{HR}	SCK(pos)-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read data hold).	2	-	ns	Figure 60
t_{QR1}, t_{QF1}	SIO_{OUT} rise / fall @ $C_{LOAD,MAX}$ = 20pF	-	12	ns	Figure 60
t_{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF	-	20	ns	Figure 60
t_{NAPXA}	NAP exit delay - phase A	-	50	ns	Figure 48
t_{NAPXB}	NAP exit delay - phase B	-	40	ns	Figure 48
t_{PDNXA}	PDN exit delay - phase A	-	4	µs	Figure 48
t_{PDNXB}	PDN exit delay - phase B	-	9000	t_{CYCLE}	Figure 48
t_{AS}	ATTN-to-STBY power state delay	-	1	t_{CYCLE}	Figure 46
t_{SA}	STBY-to-ATTN power state delay	-	0	t_{CYCLE}	Figure 46
t_{ASN}	ATTN / STBY-to-NAP power state delay	-	8	t_{CYCLE}	Figure 47
t_{ASP}	ATTN / STBY-to-PDN power state delay	-	8	t_{CYCLE}	Figure 47

a. This parameter also applies to a -800 or -711 part when operated with t_{CYCLE}=3.33ns.
b. This parameter also applies to a -1066 part when operated with t_{CYCLE}=2.50ns.
c. $t_{Q,MIN}$ and $t_{Q,MAX}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.

Electrical Characteristics

Table 20: Electrical Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
Θ_{JC}	Junction-to-Case thermal resistance	manufacturer-specific values		°C / Watt
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10	10	µA
I_{OH}	RSL output high current @ ($0 \le V_{OUT} \le V_{DD}$)	-10	10	µA
I_{ALL}	RSL I_{OL} current @ V_{OL} = 0.9V, $V_{DD,MIN}$, $T_{J,MAX}$[a]	30.0	90.0	mA
ΔI_{OL}	RSL I_{OL} current resolution step @ t_{CYCLE}=3.33ns RSL I_{OL} current resolution step @ t_{CYCLE}=2.50ns RSL I_{OL} current resolution step @ t_{CYCLE}=1.875ns	- - -	2.0 2.0 1.5	mA mA mA
r_{OUT}	Dynamic output impedance @ V_{OL}= 0.9V	150	-	Ω
$I_{OL,NOM}$	RSL I_{OL} current @ V_{OL} = 1.0V [b,c]	26.6	30.6	mA
$I_{OL\_A01,NOM}$	RSL I_{OL} current @ V_{OL} = 0.9V [b,d]	30.1	34.1	mA
$I_{I,CMOS}$	CMOS input leakage current @ ($0 \le V_{I,CMOS} \le V_{CMOS}$)	-10.0	10.0	µA
$V_{OL,CMOS}$	CMOS output voltage @ $I_{OL,CMOS}$= 1.0mA	-	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$= -0.25mA	V_{CMOS}-0.3	-	V

a. This measurement is made in manual current control mode; i.e. with all output device legs sinking current.
b. This measurement is made in automatic current control mode after at least 64 current control calibration operations to a device and after CCA and CCB are initialized to a value of 64. This value applies to all DQA and DQB pins.
c. This measurement is made in automatic current control mode in a 25Ω test system with V_{TERM}= 1.714V and V_{REF}= 1.357V and with the ASYMA and ASYMB register fields set to 0.
d. This measurement is made in automatic current control mode in a 25Ω test system with V_{TERM}= 1.714V and V_{REF}= 1.357V and with the ASYMA and ASYMB register fields set to 1.

RSL - Clocking

Figure 55 is a timing diagram which shows the detailed requirements for the RSL clock signals on the Channel.

The CTM and CTMN are differential clock inputs used for transmitting information on the DQA and DQB outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CTM edge to the falling CTM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CTM. The t_{CR} and t_{CF} rise- and fall-time parameters are measured at the 20% and 80% points.

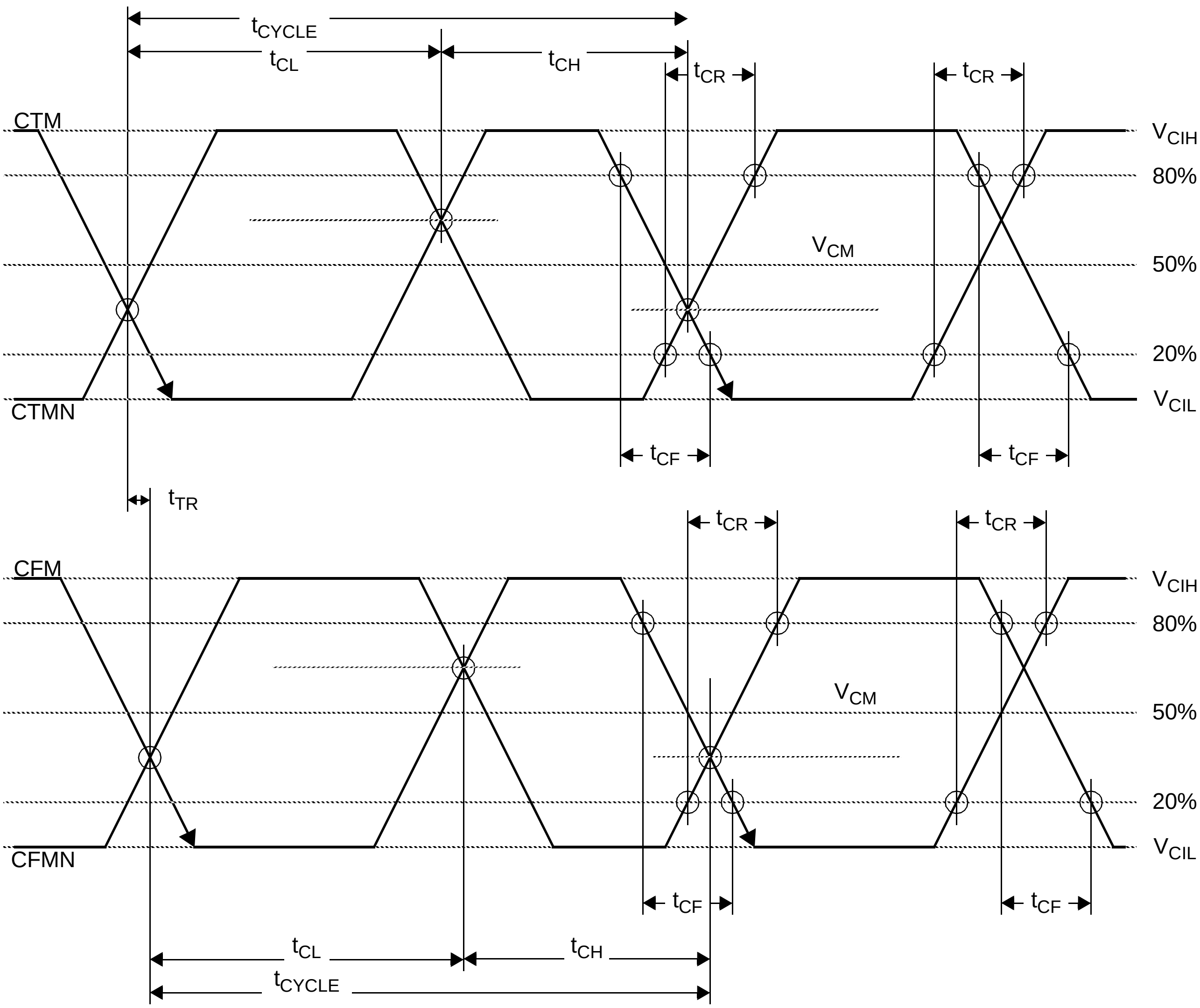


Figure 55: RSL Timing - Clock Signals

The CFM and CFMN are differential clock outputs used for receiving information on the DQA, DQB, ROW and COL outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CFM edge to the falling CFM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CFM. The t_{CR} and t_{CF} rise- and fall-time parameters are measured at the 20% and 80% points.

The t_{TR} parameter specifies the phase difference that may be tolerated with respect to the CTM and CFM differential clock inputs (the CTM pair is always earlier).

RSL - Receive Timing

Figure 56 is a timing diagram which shows the detailed requirements for the RSL input signals on the Channel.

The DQA, DQB, ROW, and COL signals are inputs which receive information transmitted by a Direct RAC on the Channel. Each signal is sampled twice per t_{CYCLE} interval. The set/hold window of the sample points is t_S/t_H. The sample points are centered at the 0% and 50% points of a cycle, measured relative to the crossing points of the falling CFM clock edge. The set and hold parameters are measured at the V_{REF} voltage point of the input transition.

The t_{DR} and t_{DF} rise- and fall-time parameters are measured at the 20% and 80% points of the input transition.

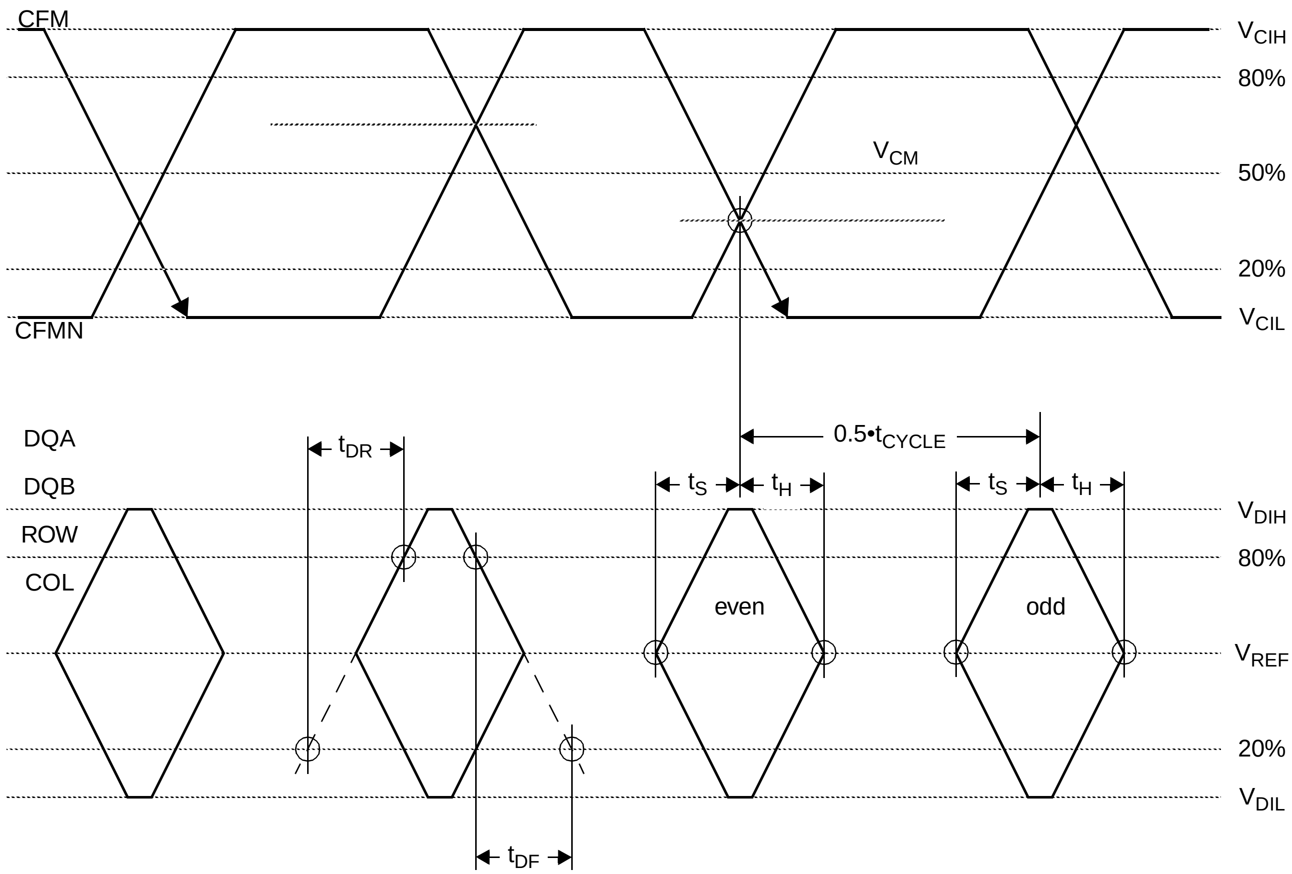


Figure 56: RSL Timing - Data Signals for Receive

RSL - Transmit Timing

Figure 57 is a timing diagram which shows the detailed requirements for the RSL output signals on the Channel.

The DQA and DQB signals are outputs to transmit information that is received by a Direct RAC on the Channel. Each signal is driven twice per t_{CYCLE} interval. The beginning and end of the even transmit window is at the 75% point of the previous cycle and at the 25% point of the current cycle. The beginning and end of the odd transmit window is at the 25% point and at the 75% point of the current cycle. These transmit points are measured relative to the crossing points of the falling CTM clock edge. The size of the actual transmit window is less than the ideal $t_{CYCLE}/2$, as indicated by the non-zero values of $t_{Q,MIN}$ and $t_{Q,MAX}$. The t_Q parameters are measured at the 50% voltage point of the output transition.

The t_{QR} and t_{QF} rise- and fall-time parameters are measured at the 20% and 80% points of the output transition.

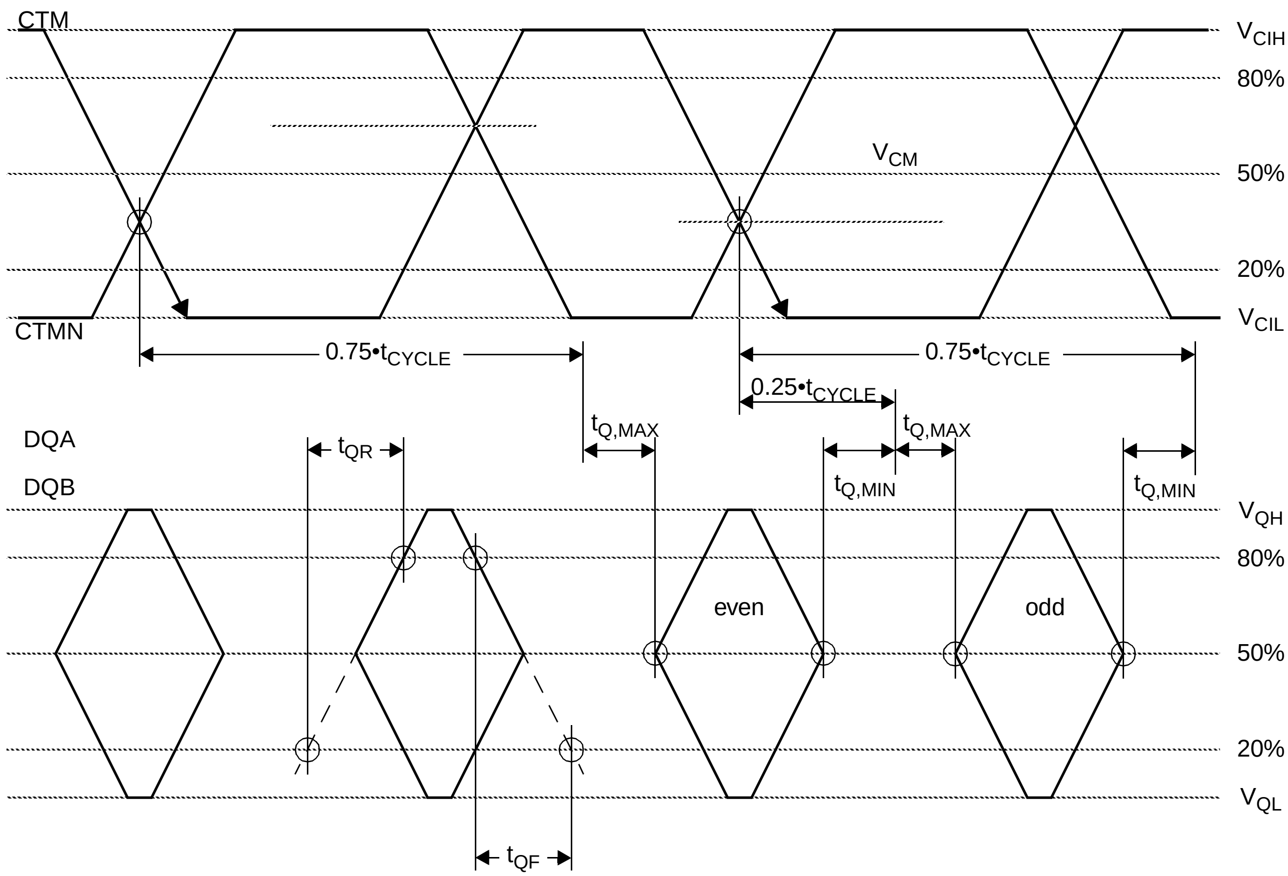


Figure 57: RSL Timing - Data Signals for Transmit

CMOS - Receive Timing

Figure 58 is a timing diagram which shows the detailed requirements for the CMOS input signals .

The CMD and SIO0 signals are inputs which receive information transmitted by a controller (or by another RDRAM's SIO1 output. SCK is the CMOS clock signal driven by the controller. All signals are high true.

The cycle time, high phase time, and low phase time of the SCK clock are t_{CYCLE1}, t_{CH1} and t_{CL1}, all measured at the 50% level. The rise and fall times of SCK, CMD, and SIO0 are t_{DR1} and t_{DF1}, measured at the 20% and 80% levels.

The CMD signal is sampled twice per t_{CYCLE1} interval, on the rising edge (odd data) and the falling edge (even data). The set / hold window of the sample points is t_{S1} / t_{H1}. The SCK and CMD timing points are measured at the 50% level.

The SIO0 signal is sampled once per t_{CYCLE1} interval on the falling edge. The set / hold window of the sample points is t_{S2} / t_{H2}. The SCK and SIO0 timing points are measured at the 50% level.

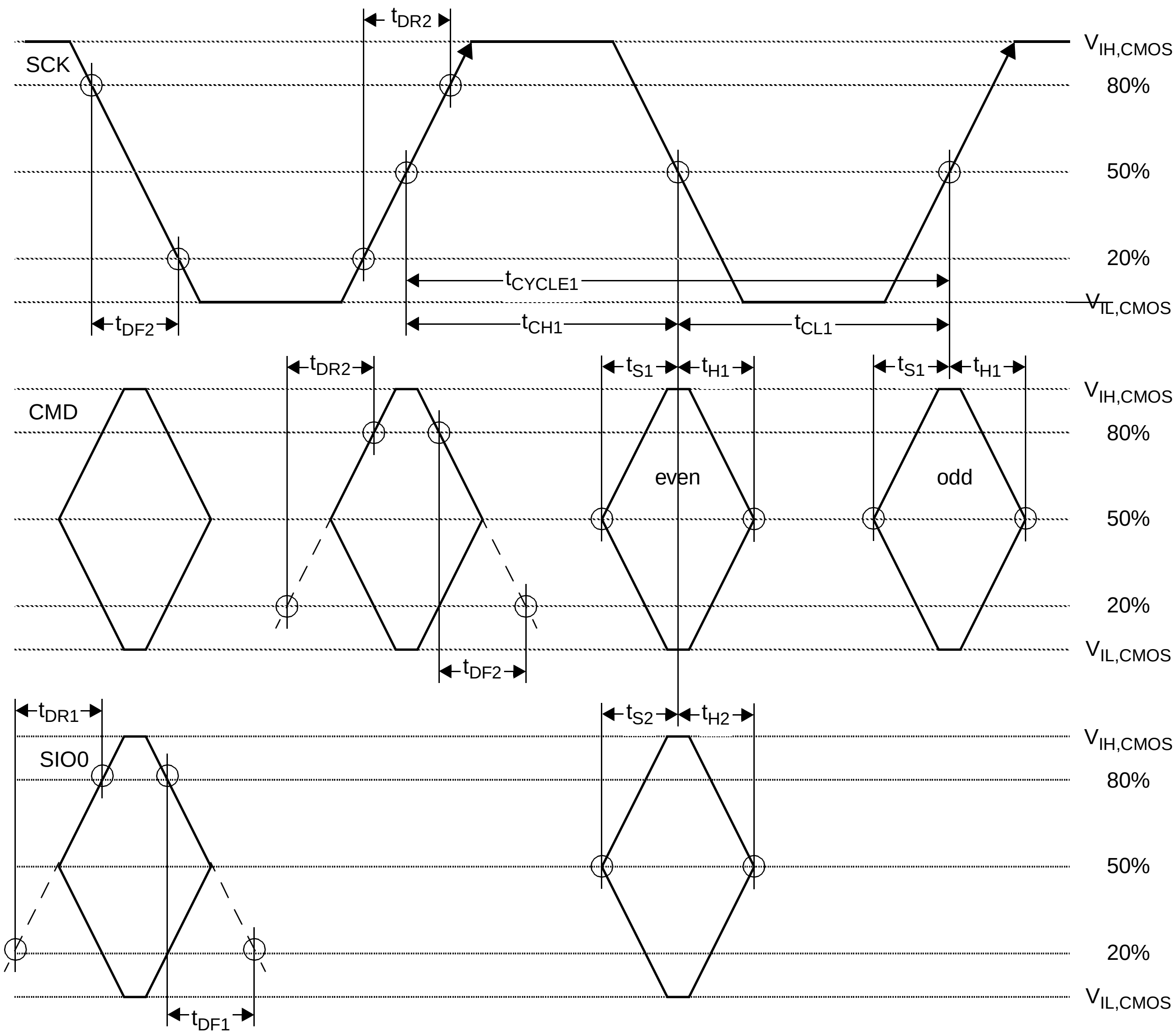


Figure 58: CMOS Timing - Data Signals for Receive

The SCK clock is also used for sampling data on RSL inputs in one situation. Figure 48 shows the PDN and NAP exit sequences. If the PSX field of the INIT register is one (see Figure 27), then the PDN and NAP exit sequences are broadcast; i.e. all RDRAMs that are in PDN or NAP will perform the exit sequence. If the PSX field of the INIT register is zero, then the PDN and NAP exit sequences are directed; i.e. only one RDRAM that is in PDN or NAP will perform the exit sequence.

The address of that RDRAM is specified on the DQA[5:0] bus in the set hold window t_{S3} / t_{H3} around the rising edge of SCK. This is shown in Figure 59. The SCK timing point is measured at the 50% level, and the DQA[5:0] bus signals are measured at the V_{REF} level.

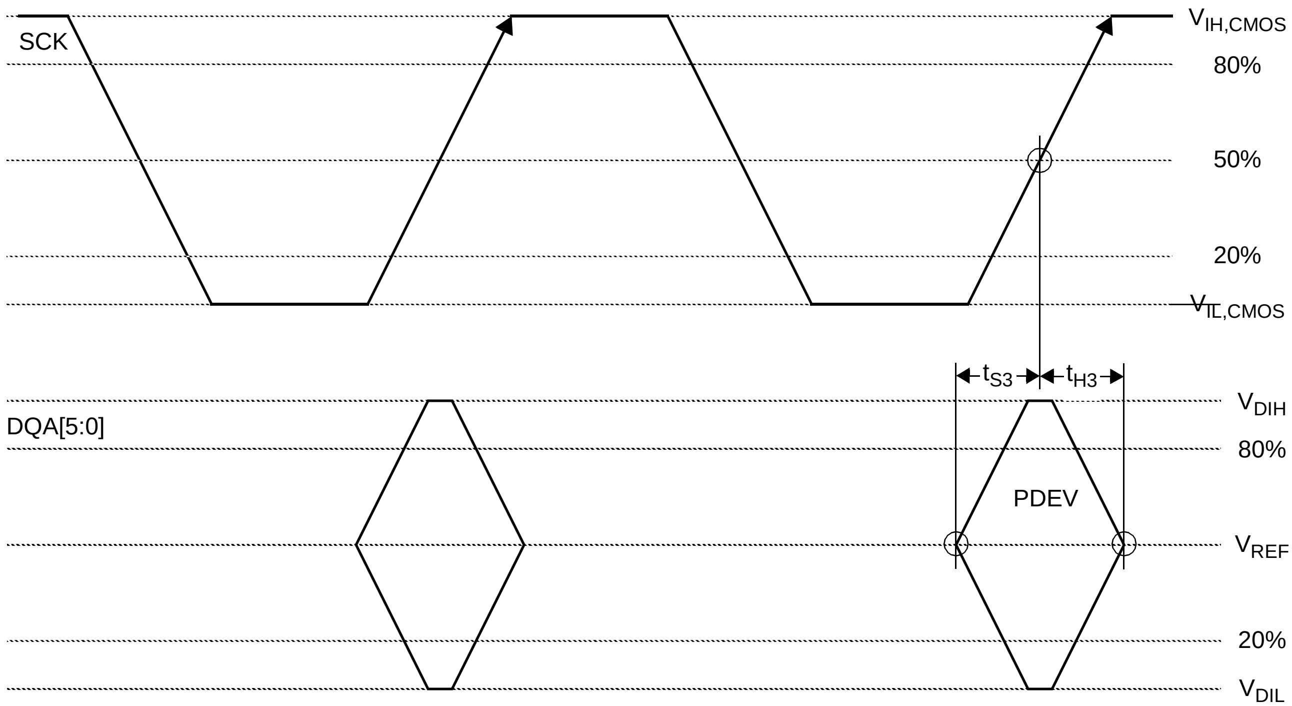


Figure 59: CMOS Timing - Device Address for NAP or PDN Exit

CMOS - Transmit Timing

Figure 60 is a timing diagram which shows the detailed requirements for the CMOS output signals. The SIO0 signal is driven once per t_{CYCLE1} interval on the falling edge. The clock-to-output window is $t_{Q1,MIN}$ / $t_{Q1,MAX}$. The SCK and SIO0 timing points are measured at the 50% level. The rise and fall times of SIO0 are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.

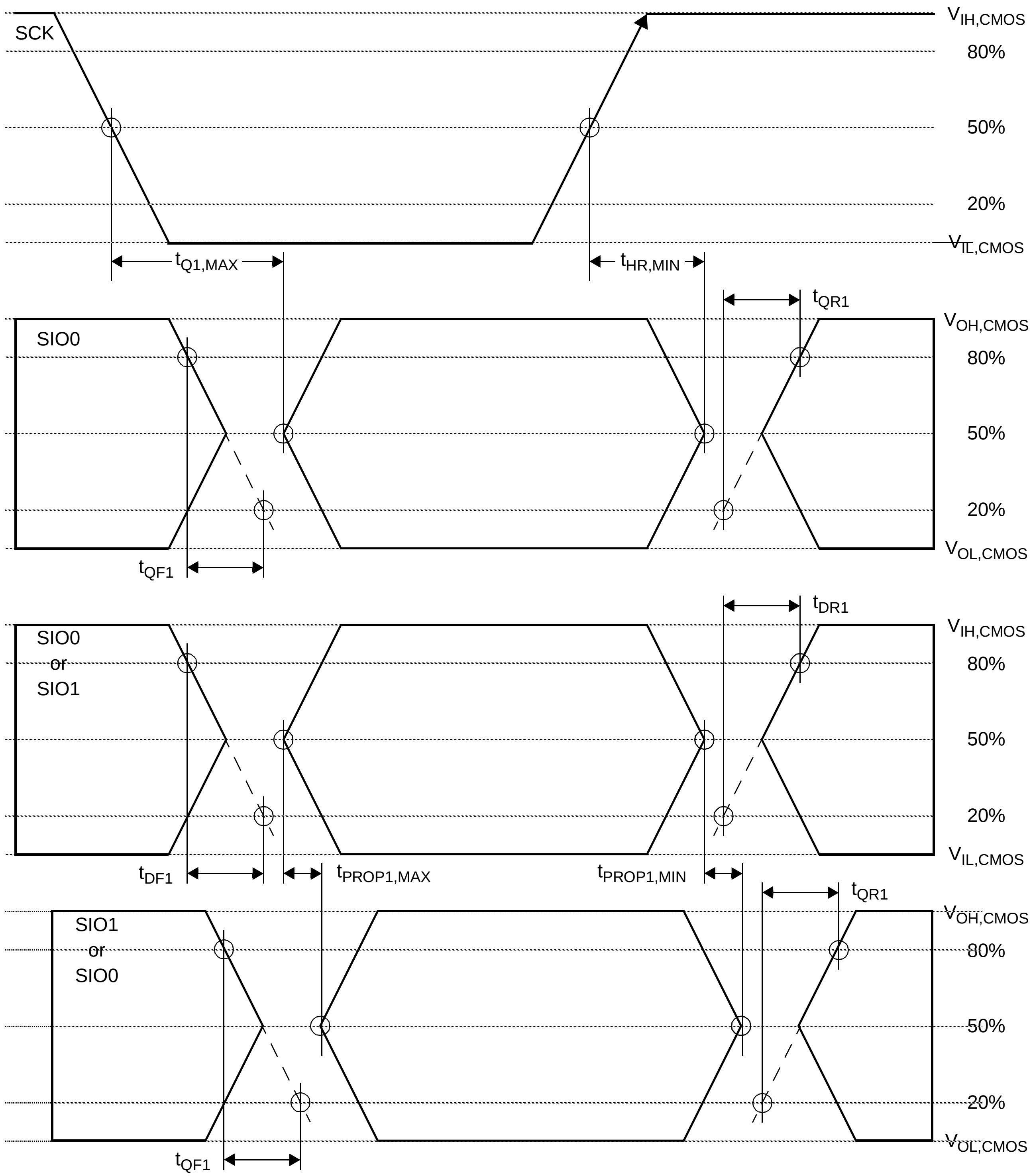


Figure 60: CMOS Timing - Data Signals for Transmit

Figure 60 also shows the combinational path connecting SIO0 to SIO1 and the path connecting SIO1 to SIO0 (read data only). The t_{PROP1} parameter specified this propagation delay. The rise and fall times of SIO0 and SIO1 inputs must be t_{DR1} and t_{DF1}, measured at the 20% and 80% levels. The rise and fall times of SIO0 and SIO1 outputs are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.

RSL - Domain Crossing Window

When read data is returned by the RDRAM, imformation must cross from the receive clock domain (CFM) to the transmit clock domain (CTM). The t_{TR} parameter permits the CFM to CTM phase to vary through an entire cycle; i.e. there is no restriction on the alignment of these two clocks. A second parameter t_{DCW} is needed in order to describe how the delay between a RD command packet and read data packet varies as a function of the t_{TR} value.

Figure 61 shows this timing for five distinct values of t_{TR}. Case A (t_{TR}=0) is what has been used throughout this document. The delay between the RD command and read data is t_{CAC}. As t_{TR} varies from zero to t_{CYCLE} (cases A through E), the command to data delay is (t_{CAC}-t_{TR}). When the t_{TR} value is in the range 0 to $t_{DCW,MAX}$, the command to data delay can also be (t_{CAC}-t_{TR}-t_{CYCLE}). This is shown as cases A' and B' (the gray packets). Similarly, when the t_{TR} value is in the range (t_{CYCLE}+$t_{DCW,MIN}$) to t_{CYCLE}, the command to data delay can also be (t_{CAC}-t_{TR}+t_{CYCLE}). This is shown as cases D' and E' (the gray packets). The RDRAM will work reliably with either the white or gray packet timing. The delay value is selected at initialization, and remains fixed thereafter.

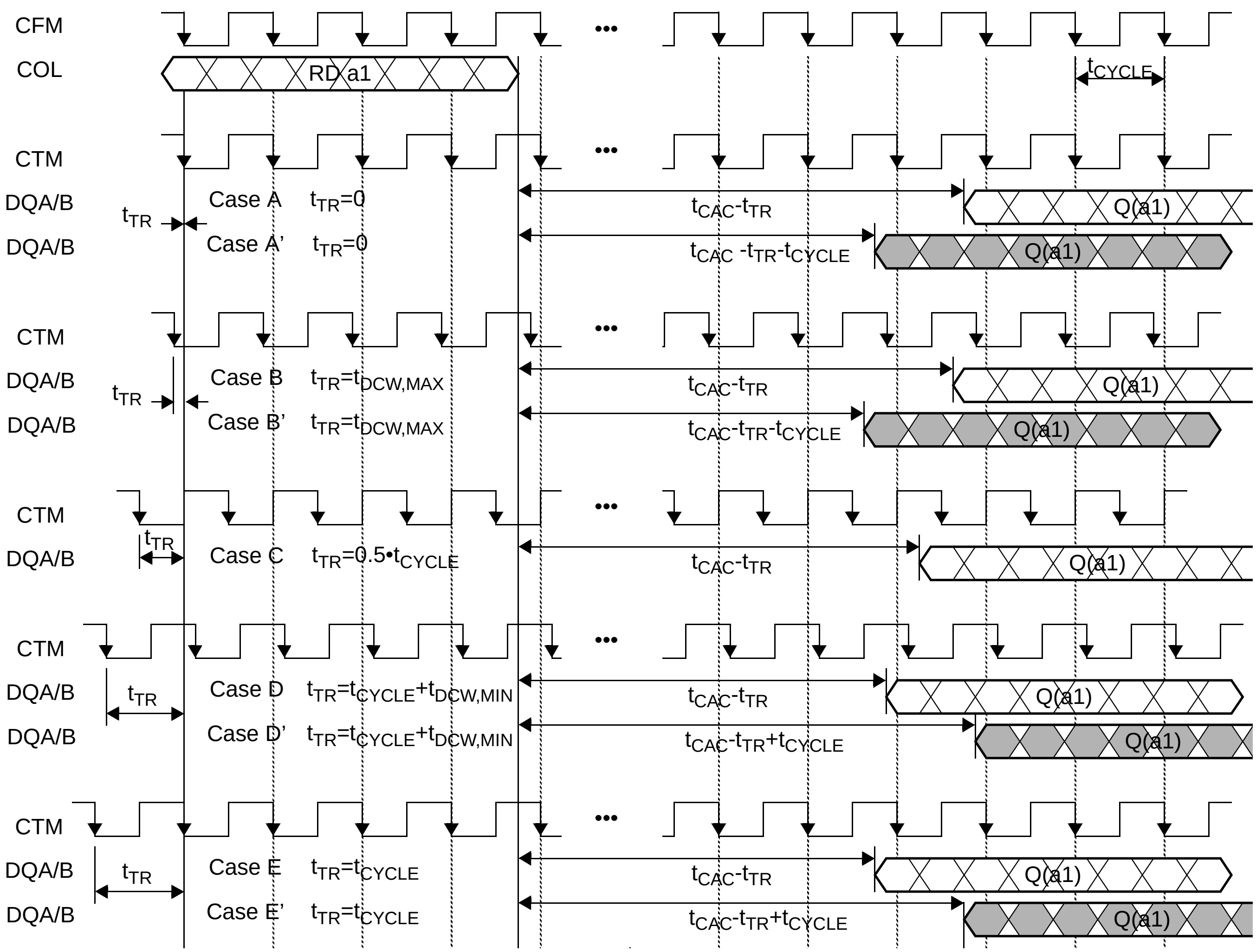


Figure 61: RSL Transmit - Crossing Read Domains

Timing Parameters

Table 21: Timing Parameter Summary

Parameter	Description	Min -35 -1066	Min -40 -800	Min -45 -800	Min -53 -600	Max	Units	Figure(s)
t_{RC}	Row Cycle time of RDRAM banks -the interval between ROWA packets with ACT commands to the same bank.	28	28	28	28	-	t_{CYCLE}	Figure 15 Figure 16
t_{RAS}	RAS-asserted time of RDRAM bank - the interval between ROWA packet with ACT command and next ROWR packet with PRER[a] command to the same bank.	20	20	20	20	64µs[b]	t_{CYCLE}	Figure 15 Figure 16
t_{RP}	Row Precharge time of RDRAM banks - the interval between ROWR packet with PRER[a] command and next ROWA packet with ACT command to the same bank.	8	8	8	8	-	t_{CYCLE}	Figure 15 Figure 16
t_{PP}	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER[a] commands to any banks of the same device.	8	8	8	8	-	t_{CYCLE}	Figure 12
t_{RR}	RAS-to-RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	8	-	t_{CYCLE}	Figure 13
t_{RCD}	RAS-to-CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command). Note - the RAS-to-CAS delay seen by the RDRAM core (t_{RCD-C}) is equal to $t_{RCD-C} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	9	7	9	7	-	t_{CYCLE}	Figure 15 Figure 16
t_{CAC}	CAS Access delay - the interval from RD command to Q read data. The equation for t_{CAC} is given in the TPARM register in Figure 39.	9	8	8	8	12	t_{CYCLE}	Figure 4 Figure 39
t_{CWD}	CAS Write Delay (interval from WR command to D write data.	6	6	6	6	6	t_{CYCLE}	Figure 4
t_{CC}	CAS-to-CAS time of RDRAM bank - the interval between successive COLC commands).	4	4	4	4	-	t_{CYCLE}	Figure 15 Figure 16
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	4	t_{CYCLE}	Figure 3
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	8	-	t_{CYCLE}	Figure 17
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLC packet with PREC command, or from COLX packet with PREX command to the equivalent ROWR packet with PRER. The equation for t_{OFFP} is given in the TPARM register in Figure 39.[c]	4	4	4	4	5	t_{CYCLE}	Figure 14 Figure 39
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	5	4	4	4	-	t_{CYCLE}	Figure 15
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	5	4	4	4	-	t_{CYCLE}	Figure 16

a. Or equivalent PREC or PREX command. See Figure 14.
b. This is a constraint imposed by the core, and is therefore in units of µs rather than t_{CYCLE}.
c. The programmed value of t_{OFFP} must be greater than or equal to $t_{RTP,MIN}$ and $t_{RDP,MIN}$. If not, the following cannot be used: autoprecharge commands (WRA or RDA) or PREX commands to the same bank as a read or retire in the same COL packet. See Figure 39.

Absolute Maximum Ratings

Table 22: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	- 0.3	V_{DD}+0.3	V
$V_{DD,ABS}$, $V_{DDA,ABS}$	Voltage on VDD and VDDA with respect to Gnd	- 0.5	V_{DD}+1.0	V
T_{STORE}	Storage temperature	- 50	100	°C

I_{DD} - Supply Current Profile

Table 23: Supply Current Profile[a]

I_{DD} value	RDRAM Power State and Steady- State Transaction Rates[b]	Min	Max@ t_{CYCLE} =3.33ns	Max@ t_{CYCLE} =2.50ns	Max@ t_{CYCLE} =1.875ns	Unit
$I_{DD,PDN}$	Device in PDN, self-refresh enabled and INIT.LSR=0.	-	6000	6000	6000	µA
$I_{DD,PDN,L}$	Device in PDN, self-refresh enabled and INIT.LSR=1.	-	2800	2800	2800	µA
$I_{DD,NAP}$	Device in NAP.	-	4.2	4.2	4.2	mA
$I_{DD,STBY}$	Device in STBY. This is the average for a device in STBY with (1) no packets on the Channel, and (2) with packets sent to other devices.	-	90	101	101	mA
$I_{DD,REFRESH}$	Device in STBY and refreshing rows at the $t_{REF,MAX}$ period.	-	95	110	110	mA
$I_{DD,ATTN}$	Device in ATTN. This is the average for a device in ATTN with (1) no packets on the Channel, and (2) with packets sent to other devices.	-	125	148	148	mA
$I_{DD,ATTN-W}$	Device in ATTN. ACT command every 8•t_{CYCLE}, PRE command every 8•t_{CYCLE}, WR command every 4•t_{CYCLE}, and data is 1100..1100	-	475(x16) 525 (x18)	575(x16) 635 (x18)	575(x16) 635 (x18)	mA
$I_{DD,ATTN-R}$	Device in ATTN. ACT command every 8•t_{CYCLE}, PRE command every 8•t_{CYCLE}, RD command every 4•t_{CYCLE}, and data is 1111..1111[c]	-	445(x16) 480 (x18)	530(x16) 575 (x18)	530(x16) 575 (x18)	mA

a. The numbers in this table are targets, not specifications.
b. CMOS interface consumes no power in all power states
c. This does not include the I_{OL} sink current. The RDRAM dissipates I_{OL}•V_{OL} in each output driver when a logic one is driven.

Table 24: Supply Current at Initialization[a]

Symbol	Parameter	Allowed Range of t_{CYCLE}	V_{DD}	Min	Max	Unit
$I_{DD,PWRUP,D}$	I_{DD} from power -on to SETR	3.33ns to 3.83ns 2.50ns to 3.32ns 1.875ns to 2.49ns	$V_{DD,MIN}$	-	150[b] 200[b] 200[b]	mA
$I_{DD,SETR,D}$	I_{DD} from SETR to CLRR	3.33ns to 3.83ns 2.50ns to 3.32ns 1.875ns to 2.49ns	$V_{DD,MIN}$	-	250[b] 332[b] 450[b]	mA

a. The numbers in this table are specifications, and must be met by all devices.
b. The supply current will be 150mA when t_{CYCLE} is in the range 15ns to 1000ns.

Capacitance and Inductance

Figure 62 shows the equivalent load circuit of the RSL and CMOS pins. The circuit models the load that the device presents to the Channel.

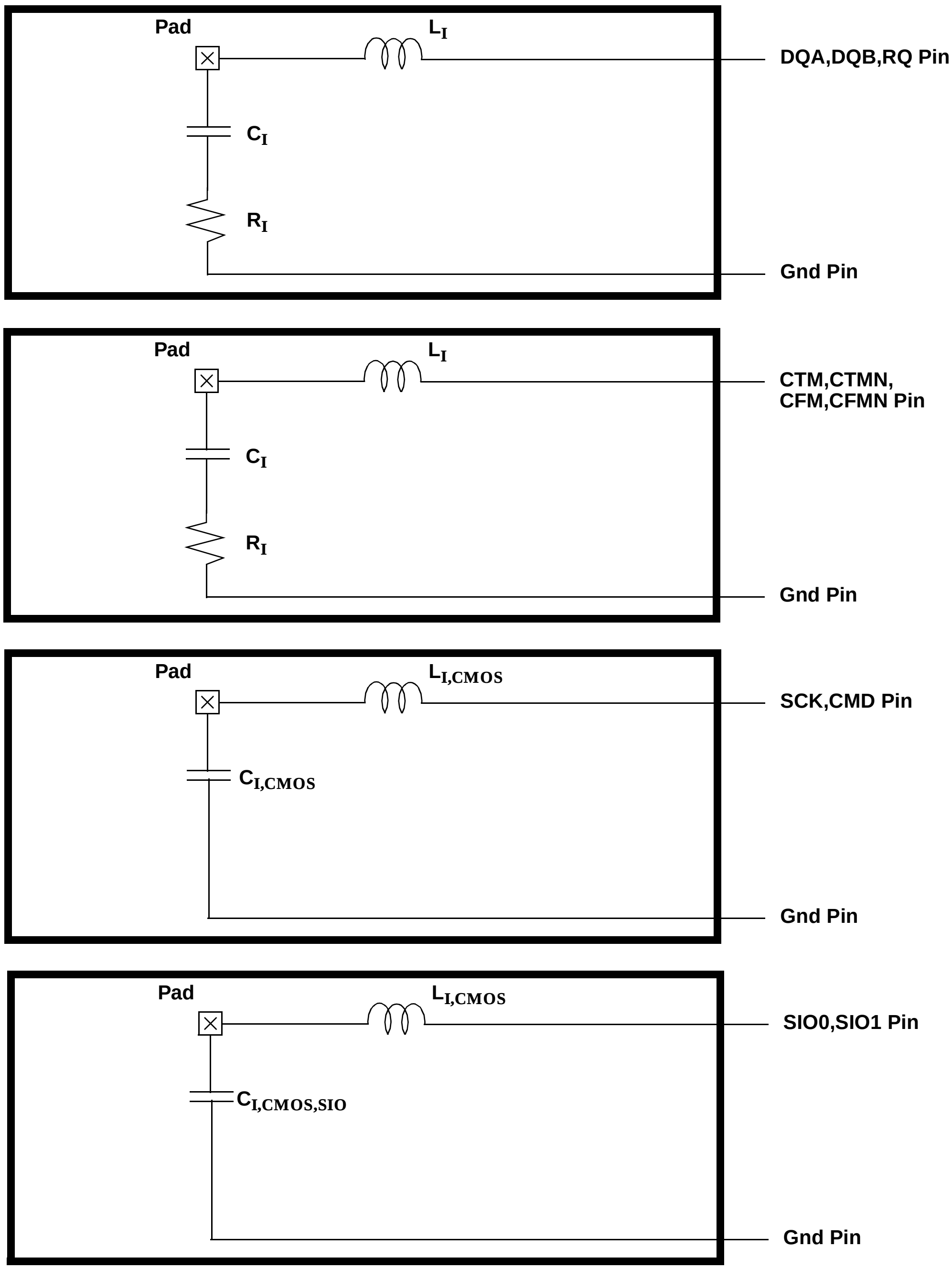


Figure 62: Equivalent Load Circuit for RSL Pins

This circuit does not include pin coupling effects that are often present in the packaged device. Because coupling effects make the effective single-pin inductance L_I, and capacitance C_I, a function of neighboring pins, these parameters are intrinsically data-dependent. For purposes of specifying the device electrical loading on the Channel, the effective L_I and C_I are defined as the worst-case values over all specified operating conditions.

L_I is defined as the effective pin inductance based on the device pin assignment. Because the pad assignment places each RSL signal adjacent to an AC ground (a Gnd or Vdd pin), the effective inductance must be defined based on this configuration. Therefore, L_I assumes a loop with the RSL pin adjacent to an AC ground.

C_I is defined as the effective pin capacitance based on the device pin assignment. It is the sum of the effective package pin capacitance and the IO pad capacitance.

Table 25: RSL Pin Parasitics

Symbol	Parameter and Conditions - RSL pins	Min	Max	Unit
L_I	RSL effective input inductance -1066 RSL effective input inductance -800 RSL effective input inductance -600	- - -	3.5 4.0 4.0	nH nH nH
L_{12}	Mutual inductance between any DQA or DQB RSL signals.		0.2	nH
	Mutual inductance between any ROW or COL RSL signals.		0.6	nH
ΔL_I	Difference in L_I value between any RSL pins of a single device.	-	1.8	nH
C_I	RSL effective input capacitance[a] -1066 RSL effective input capacitance[a] -800 RSL effective input capacitance[a] -600	2.0 2.0 2.0	2.3 2.4 2.6	pF pF pF
C_{12}	Mutual capacitance between any RSL signals.	-	0.1	pF
ΔC_I	Difference in C_I value between average of {CTM, CTMN, CFM, CFMN} and any RSL pins of a single device.	-	0.06	pF
R_I	RSL effective input resistance -1066 RSL effective input resistance -800 RSL effective input resistance -600	4 4 4	10 15 15	Ω Ω Ω

a. This value is a combination of the device IO circuitry and package capacitances measured at VDD=2.5V and f=400MHz with pin biased at 1.4V.

Table 26: CMOS Pin Parasitics

Symbol	**Parameter and Conditions - CMOS pins**	**Min**	**Max**	**Unit**
$L_{I,CMOS}$	CMOS effective input inductance		8.0	nH
$C_{I,CMOS}$	CMOS effective input capacitance (SCK,CMD)[a]	1.7	2.1	pF
$C_{I,CMOS,SIO}$	CMOS effective input capacitance (SIO1, SIO0)[a]	-	7.0	pF

a. This value is a combination of the device IO circuitry and package capacitances.

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Center-Bonded uBGA Package (16x6)

Figure 63 shows the form and dimensions of the recommended package for the 16x6 center-bonded CSP device class.

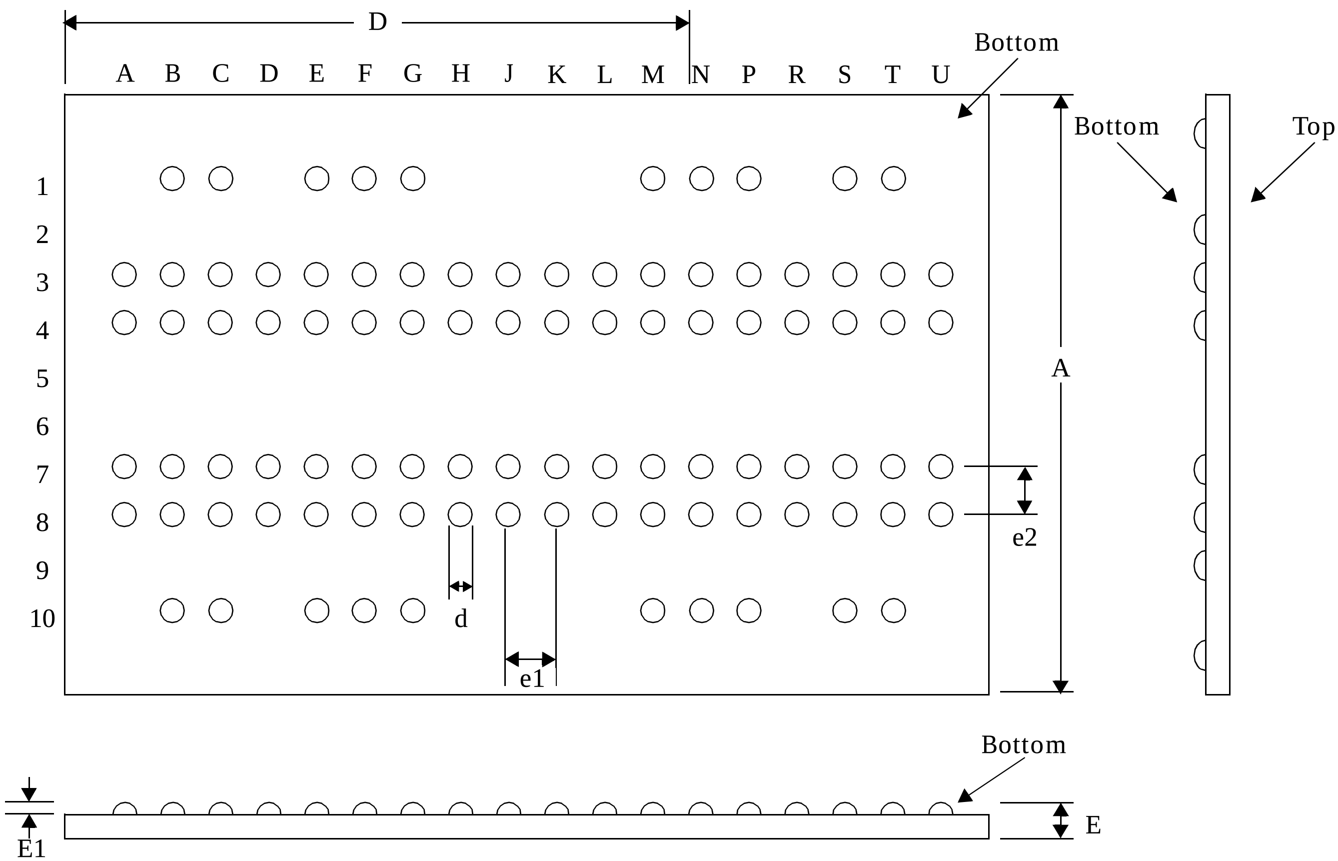

Figure 63: Center-Bonded uBGA Package

Table 27 lists the numerical values corresponding to dimensions shown in Figure 63.

Table 27: Center-Bonded uBGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
e1	Ball pitch (x-axis)	0.8	0.8	mm
e2	Ball pitch (y-axis)	0.8	0.8	mm
A	Package body length	note[a]	note[a]	-
D	Package body width	note[a]	note[a]	-
E	Package total thickness	0.65	1.20[b]	mm
E1	Ball height	0.20	0.43	mm
d	Ball diameter	0.33	0.50	mm

a. Package length and width vary with die size for chip scale packages.
b. The E,MAX parameter for SO-RIMM applications is 0.94mm.

Interleaved Device Mode

Interleaved Device Mode permits a group of eight RDRAMs on the Channel to collectively respond to a command. The purpose of this collective response is to limit the number of bits in each dualoct data packet which are read from or written to a single RDRAM device. This capability permits a memory controller to implement hardware for fault detection and correction that can tolerate the complete internal failure of one RDRAM device on a Channel.

The IDM bit of the INIT control register enables this fault tolerant operating mode. When it is set, the RDRAM will interpret the DR4..0 and DC4..0 fields of the ROW and COLC packets differently. Figure 64 shows the differences using an example system with eight RDRAMs.

The DEVID4..0 registers of these RDRAMs are initialized to “00000” through “00111’. However, when the IDM bit is set, only the upper two bits (DEVID4..3) will be compared to the DR4..3 and DC4..3 fields. This means that ROW and COLC packets will be executed by groups of eight RDRAMs, with a Channel containing from one to four of these groups. The low-order DR2..0 bits are not used when IDM is set, and the low-order DC2..0 bits have a modified function described below.

With IDM set, a directed ACT or PRE command in a ROW packet causes eight RDRAMs to perform the indicated operation. Likewise, when a RD or WR command is specified in a COLC command, the selected group of eight RDRAMs responds. When using IDM, devices must be added to the Channel in groups of eight. An application will typically make the IDM bit setting the same for all RDRAMs on a Channel.

The mechanism for indicating a broadcast ROW packet (DR4F and DR4T are both set to one) is not affected by the setting of the IDM bit; i.e. IDM mode does not change the broadcast ROW packet mechanism.

Likewise, the COLX fields (DX4..0, XOP4..0, and BX5..0) are not changed by IDM mode - all COLX packets are directed to a single device.

When the IDM bit is set, COLM packets should not be used (the M bit should be set to zero, selecting only COLX packets). This is because the mapping of bytes to RDRAM storage cells is changed by IDM mode.

Returning to Figure 64, the remaining fields of the ROW and COLC packets are interpreted in the same way regardless of the setting of the IDM bit - IDM mode does not affect these fields. Specifically, the BR5..0 and BC5..0 fields of the ROW and COLC packets are used to select one of the banks just as when IDM is not set. The R8..0 field of the ROW packet selects a row of the selected (BR5..0) bank to load into the bank’s sense amp. And the C6..0 field selects one dualoct of the selected (BC5..0) bank’s sense amp.

The IDM bit affects what is done with this selected dualoct. When IDM is not set, the dualoct is driven onto the Channel by the single selected RDRAM device. When IDM is set, each RDRAM of the eight device group selected by DC4..3 drives either 16 bits (x16 device) or 16 or 24 bits (x18 device) of the 144-bit dualoct. The bits driven are a function of the DEVID2..0 RDRAM register field, the DC2..0 COLC packet field, and the device width (x16 or x18). Figure 64 shows the mapping that is appropriate for DC2..0=000.

Figure 65 and Figure 66 show the mapping for all eight values of DC2..0. There are eight mappings, which are rotated among the eight devices using the following equation:

$$\text{Pin} = 7 - 4\bullet(\text{DEVID2}\wedge\text{DC2}) - 2\bullet(\text{DEVID1}\wedge\text{DC1}) - 1\bullet(\text{DEVID0}\wedge\text{DC0}) \qquad \text{(Eq 1)}$$

where “^” is the exclusive-or function. “Pin” is the pin number that is driven by the RDRAM with the DEVID2..0 value. For example, Pin=0 means the RDRAM drives DQA0 and DQB0, and so forth.

The DQA8 pin is always driven with DQA7, and DQB8 is always driven with DQB6 for x18 devices. For x16 devices, the DQA8 and DQB8 pins are not used.

For each of the eight mappings, the eight-RDRAM group supplies a complete dualoct. As the application steps through eight values of DC2..0, all the bits of the eight underlying dualocts will be accessed. Thus, an eight-RDRAM group appears to be a single RDRAM with eight times the normal page size, with the DC2..0 field providing the extra column addressing information (beyond what C6..0 provides).

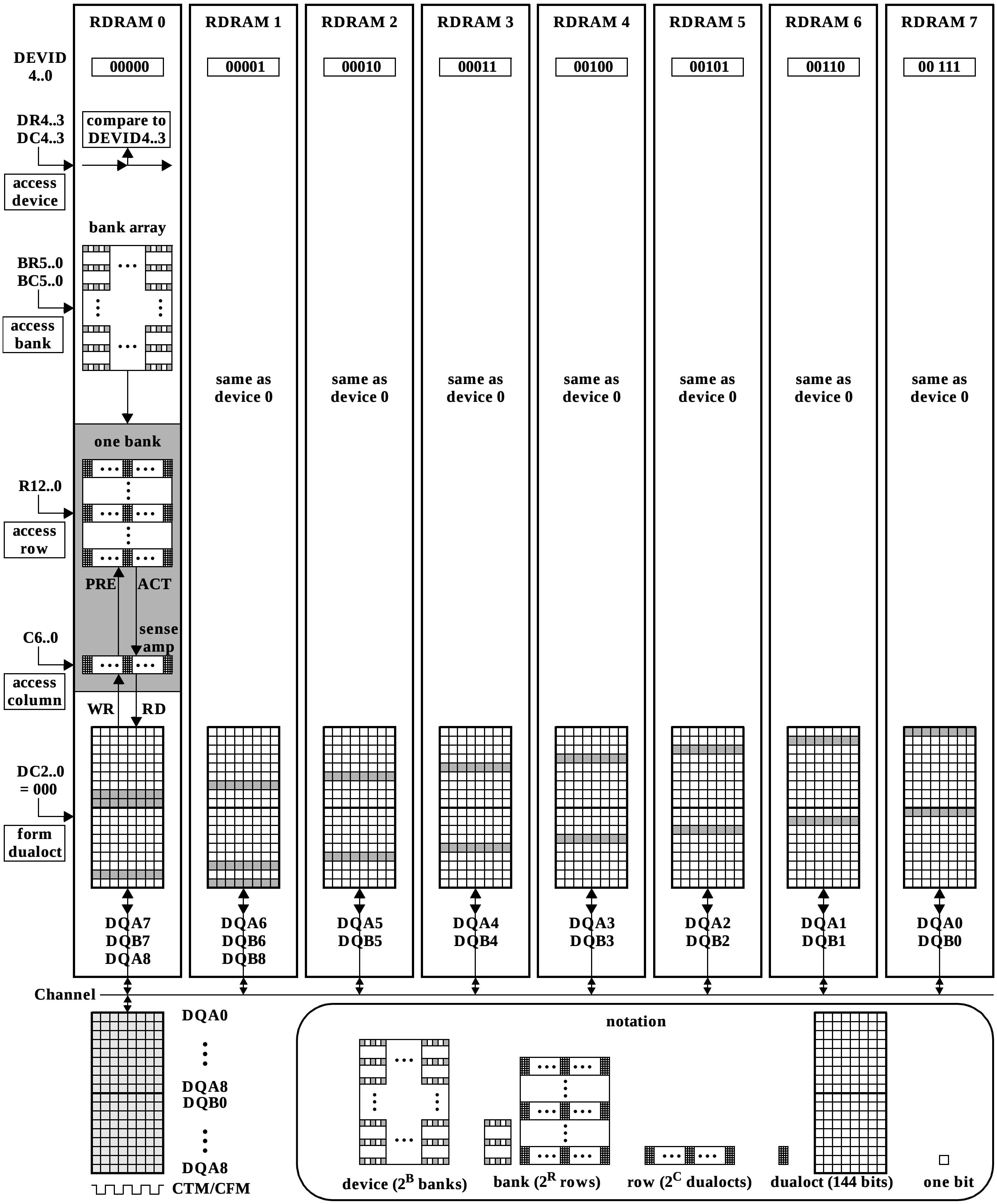

Figure 64: ACT, PRE, RD, and WR Commands for Eight RDRAM System with IDM=1

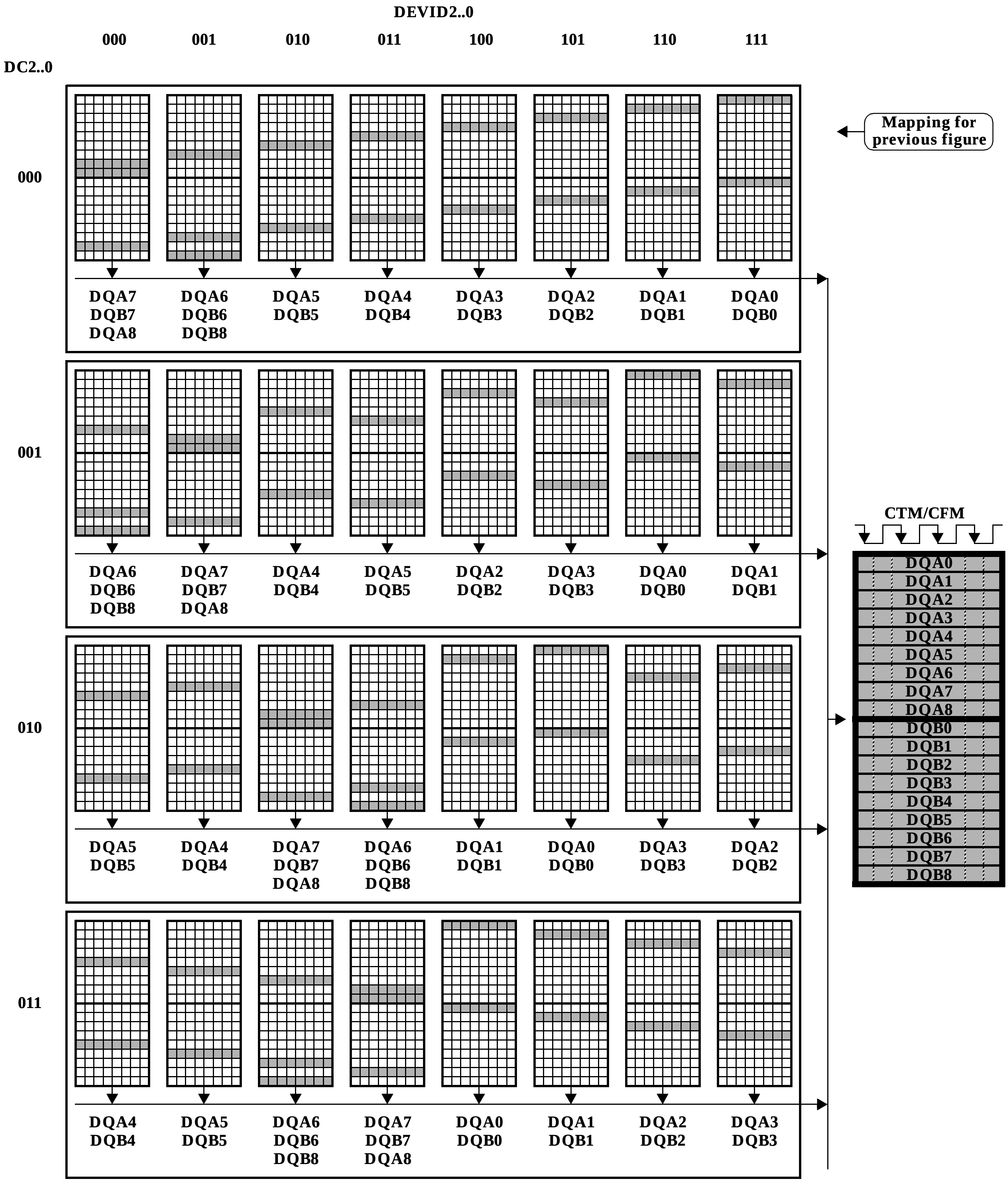

Figure 65: Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM=1

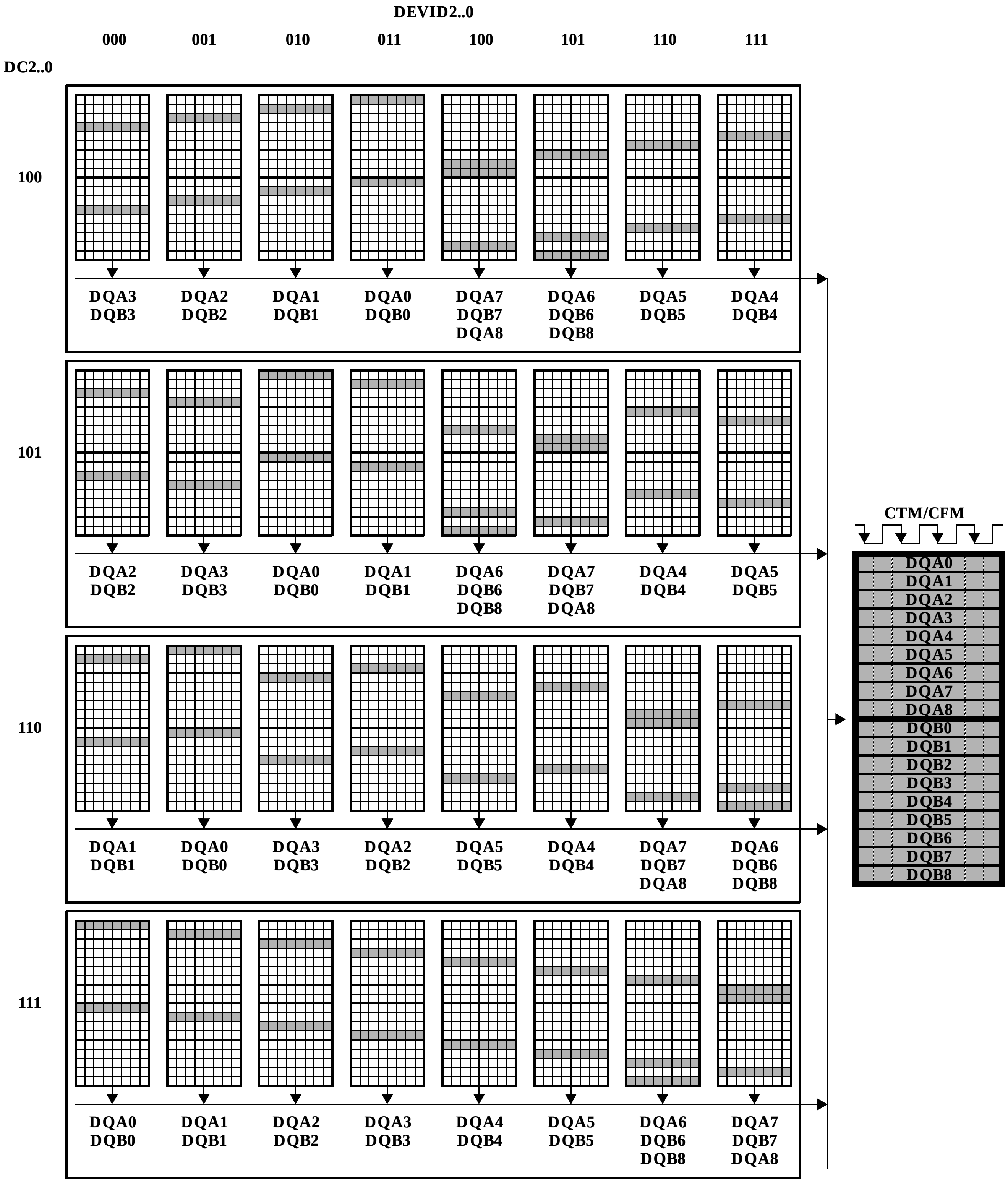

Figure 66: Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM=1 (continued)

Glossary of Terms

ACT	Activate command from AV field.
activate	To access a row and place in sense amp.
adjacent	Two RDRAM banks which share sense amps (also called doubled banks).
ASYM	CCA register field for RSL V_{OL}/V_{OH}.
ATTN	Power state - ready for ROW/COL packets.
ATTNR	Power state - transmitting Q packets.
ATTNW	Power state - receiving D packets.
AV	Opcode field in ROW packets.
bank	A block of $2^{RBIT} \cdot 2^{CBIT}$ storage cells in the core of the RDRAM.
BC	Bank address field in COLC packet.
BBIT	CNFGA register field - # bank address bits.
broadcast	An operation executed by all RDRAMs.
BR	Bank address field in ROW packets.
bubble	Idle cycle(s) on RDRAM pins needed because of a resource constraint.
BYT	CNFGB register field - 8/9 bits per byte.
BX	Bank address field in COLX packet.
C	Column address field in COLC packet.
CAL	Calibrate (I_{OL}) command in XOP field.
CBIT	CNFGB register field - # column address bits.
CCA	Control register - current control A.
CCB	Control register - current control B.
CFM,CFMN	Clock pins for receiving packets.
Channel	ROW/COL/DQ pins and external wires.
CLRR	Clear reset command from SOP field.
CMD	CMOS pin for initialization/power control.
CNFGA	Control register with configuration fields.
CNFGB	Control register with configuration fields.
COL	Pins for column-access control.
COL	COLC,COLM,COLX packet on COL pins.
COLC	Column operation packet on COL pins.
COLM	Write mask packet on COL pins.
column	Rows in a bank or activated row in sense amps have 2^{CBIT} dualocts column storage.
command	A decoded bit-combination from a field.
COLX	Extended operation packet on COL pins.
controller	A logic-device which drives the ROW/COL /DQ wires for a Channel of RDRAMs.
COP	Column opcode field in COLC packet.
core	The banks and sense amps of an RDRAM.
CTM,CTMN	Clock pins for transmitting packets.
current control	Periodic operations to update the proper I_{OL} value of RSL output drivers.
D	Write data packet on DQ pins.
DBL	CNFGB register field - doubled-bank.
DC	Device address field in COLC packet.
device	An RDRAM on a Channel.
DEVID	Control register with device address that is matched against DR, DC, and DX fields.
DM	Device match for ROW packet decode.
doubled-bank	RDRAM with shared sense amp.
DQ	DQA and DQB pins.
DQA	Pins for data byte A.
DQB	Pins for data byte B.
DQS	NAPX register field - PDN/NAP exit.
DR,DR4T,DR4F	Device address field and packet framing fields in ROWA and ROWR packets.
dualoct	16 bytes - the smallest addressable datum.
DX	Device address field in COLX packet.
field	A collection of bits in a packet.
INIT	Control register with initialization fields.
initialization	Configuring a Channel of RDRAMs so they are ready to respond to transactions.
LSR	CNFGA register field - low-power self-refresh.
M	Mask opcode field (COLM/COLX packet).
MA	Field in COLM packet for masking byte A.
MB	Field in COLM packet for masking byte B.
MSK	Mask command in M field.
MVER	Control register - manufacturer ID.
NAP	Power state - needs SCK/CMD wakeup.
NAPR	Nap command in ROP field.
NAPRC	Conditional nap command in ROP field.
NAPXA	NAPX register field - NAP exit delay A.
NAPXB	NAPX register field - NAP exit delay B.
NOCOP	No-operation command in COP field.
NOROP	No-operation command in ROP field.
NOXOP	No-operation command in XOP field.

NSR	INIT register field- NAP self-refresh.
packet	A collection of bits carried on the Channel.
PDN	Power state - needs SCK/CMD wakeup.
PDNR	Powerdown command in ROP field.
PDNXA	Control register - PDN exit delay A.
PDNXB	Control register - PDN exit delay B.
pin efficiency	The fraction of non-idle cycles on a pin.
PRE	PREC,PRER,PREX precharge commands.
PREC	Precharge command in COP field.
precharge	Prepares sense amp and bank for activate.
PRER	Precharge command in ROP field.
PREX	Precharge command in XOP field.
PSX	INIT register field - PDN/NAP exit.
PSR	INIT register field - PDN self-refresh.
PVER	CNFGB register field - protocol version.
Q	Read data packet on DQ pins.
R	Row address field of ROWA packet.
RBIT	CNFGB register field - # row address bits.
RD/RDA	Read (/precharge) command in COP field.
read	Operation of accesssing sense amp data.
receive	Moving information from the Channel into the RDRAM (a serial stream is demuxed).
REFA	Refresh-activate command in ROP field.
REFB	Control register - next bank (self-refresh).
REFBIT	CNFGA register field - ignore bank bits (for REFA and self-refresh).
REFP	Refresh-precharge command in ROP field.
REFR	Control register - next row for REFA.
refresh	Periodic operations to restore storage cells.
retire	The automatic operation that stores write buffer into sense amp after WR command.
RLX	RLXC,RLXR,RLXX relax commands.
RLXC	Relax command in COP field.
RLXR	Relax command in ROP field.
RLXX	Relax command in XOP field.
ROP	Row-opcode field in ROWR packet.
row	2^{CBIT} dualocts of cells (bank/sense amp).
ROW	Pins for row-access control
ROW	ROWA or ROWR packets on ROW pins.
ROWA	Activate packet on ROW pins.
ROWR	Row operation packet on ROW pins.
RQ	Alternate name for ROW/COL pins.
RSL	Rambus Signaling Levels.
SAM	Sample (I_{OL}) command in XOP field.
SA	Serial address packet for control register transactions w/ SA address field.
SBC	Serial broadcast field in SRQ.
SCK	CMOS clock pin..
SD	Serial data packet for control register transactions w/ SD data field.
SDEV	Serial device address in SRQ packet.
SDEVID	INIT register field - Serial device ID.
self-refresh	Refresh mode for PDN and NAP.
sense amp	Fast storage that holds copy of bank's row.
SETF	Set fast clock command from SOP field.
SETR	Set reset command from SOP field.
SINT	Serial interval packet for control register read/write transactions.
SIO0,SIO1	CMOS serial pins for control registers.
SOP	Serial opcode field in SRQ.
SRD	Serial read opcode command from SOP.
SRP	INIT register field - Serial repeat bit.
SRQ	Serial request packet for control register read/write transactions.
STBY	Power state - ready for ROW packets.
SVER	Control register - stepping version.
SWR	Serial write opcode command from SOP.
TCAS	TCLSCAS register field - t_{CAS} core delay.
TCLS	TCLSCAS register field - t_{CLS} core delay.
TCLSCAS	Control register - t_{CAS} and t_{CLS} delays.
TCYCLE	Control register - t_{CYCLE} delay.
TDAC	Control register - t_{DAC} delay.
TEST77	Control register - for test purposes.
TEST78	Control register - for test purposes.
TRDLY	Control register - t_{RDLY} delay.
transaction	ROW,COL,DQ packets for memory access.
transmit	Moving information from the RDRAM onto the Channel (parallel word is muxed).
WR/WRA	Write (/precharge) command in COP field.
write	Operation of modifying sense amp data.
XOP	Extended opcode field in COLX packet.

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Document DL0117-010 Version 0.1

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