

AC/DC to Logic Interface Hermetically Sealed Optocouplers

Technical Data

HCPL-576X*

5962 8947701

*See matrix for available extensions

Features

- Dual Marked with Device Part Number and DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-38534, Class H and K
- Hermetically Sealed 8-pin Dual In-Line Packages
- Performance Guaranteed over -55°C to +125°C
- ac or dc Input
- Programmable Sense Voltage
- Hysteresis
- HCPL-3700 Operating Compatibility
- Logic Compatible Output
- 1500 Vdc Withstand Test Voltage
- Thresholds Guaranteed over Temperature
- Thresholds Independent of LED Characteristics

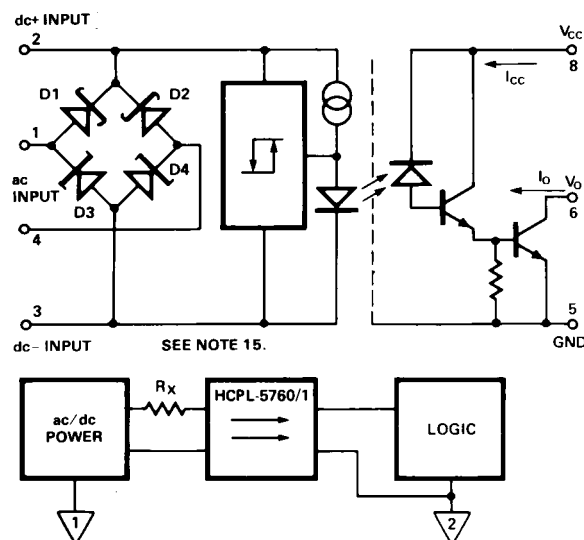
Applications

- Military and Space
- High Reliability Systems
- Transportation, Medical, and Life Critical Systems
- Limit Switch Sensing
- Low Voltage Detector
- ac/dc Voltage Sensing
- Relay Contact Monitor
- Relay Coil Voltage Monitor
- Current Sensing
- Microprocessor Interface
- Telephone Ring Detection
- Harsh Industrial Environments

Description

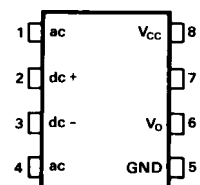
The HCPL-5760, HCPL-5761, and 5962-8947701 are single channel, hermetically sealed, voltage/current threshold detection optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product, or with full MIL-PRF-38534 Class Level H or K testing, or from the DESC Standard Military Drawing (SMD) 5962-89477. All devices

Schematic



TRUTH TABLE

INPUT	OUTPUT
$H(V_{TH} < V_{oc})(on)$	L
$L(V_{oc} < V_{TH})(off)$	H



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits.

Each unit contains a light emitting diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.6 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes

effects of any variation in optical coupling. Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

These units combine several unique functions in a single package, providing the user with an ideal component for computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

This is an eight pin DIP which may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each lead style.

Selection Guide—Package Styles and Lead Configuration Options

HP Part # and Options	
Commercial	HCPL-5760
MIL-PRF-38534 Class H	HCPL-5761
MIL-PRF-38534 Class K	HCPL-576K
Standard Lead Finish	Gold
Solder Dipped	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
Crew Cut/Gold Plate	Option #600
SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	8947701PX
Gold Plate	8947701PC
Solder Dipped	8947701PA
Butt Joint/Gold Plate	8947701YC
Butt Joint/Soldered	8947701YA
Gull Wing/Soldered	8947701XA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered	Available

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Temperature	-55°C to 125°C
Lead Solder Temperature	260°C for 10 s ^[2]
Average Input Current, I_{IN}	15 mA ^[3]
Surge Input Current, $I_{IN,SG}$	140 mA ^[3,4]
Peak Transient Input Current, $I_{IN,PK}$	500 mA ^[3,4]
Input Power Dissipation, P_{IN}	195 mW ^[5]
Total Package Power Dissipation, P_d	260 mW
Output Power Dissipation, P_O	65 mW
Average Output Current, I_O	40 mA
Supply Voltage, V_{CC} (Pins 8-5)	-0.5 min., 20 V max.
Output Voltage, V_O (Pins 6-5)	-0.5 min., 20 V max.

ESD Classification

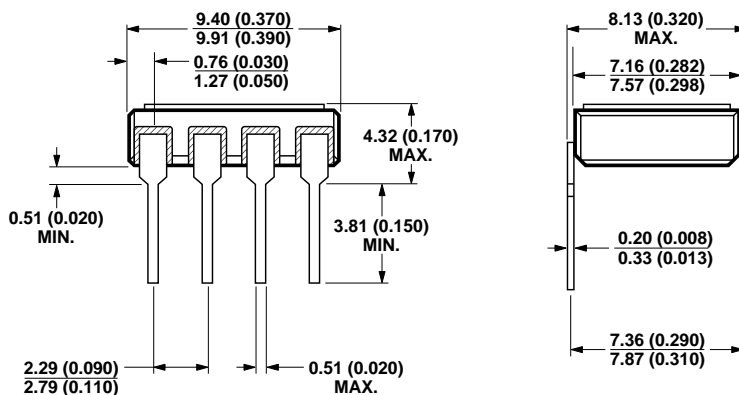
(MIL-STD-883, Method 3015) (ΔΔ), Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply	V_{CC}	3.0	18	V
Operating Frequency ^[1]	f	0	10	KHz

Outline Drawing

8 Pin DIP Through Hole



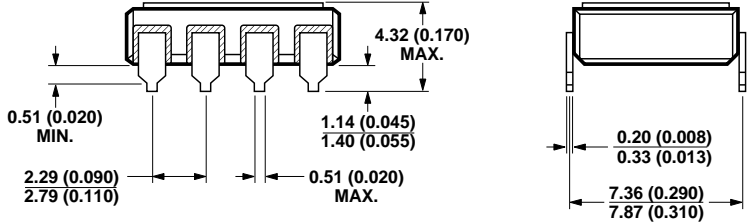
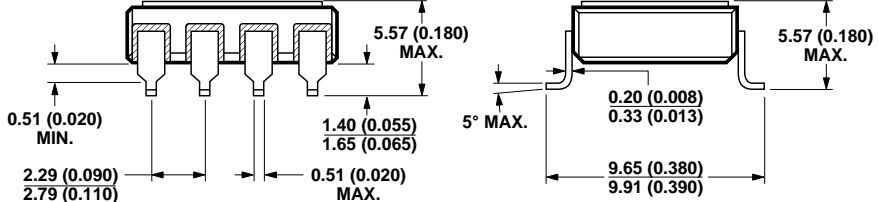
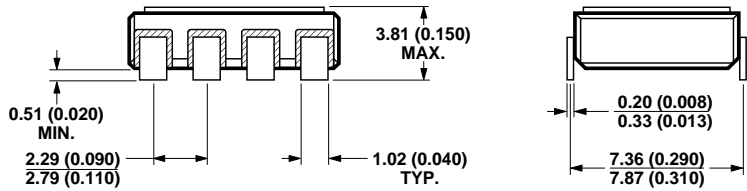
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking

HP LOGO	HP QYYWWZ	COMPLIANCE INDICATOR,*
HP P/N	XXXXXX	DATE CODE, SUFFIX (IF NEEDED)
DESC SMD*	XXXXXX	
DESC SMD*	XXX USA	COUNTRY OF MFR.
PIN ONE/	▲▲ 50434	HP FSCN*
ESD IDENT		

* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product.</p>  <p>Top view dimensions: 0.51 (0.020) MIN. (lead width), 2.29 (0.090) (lead pitch), 2.79 (0.110) (lead pitch), 1.14 (0.045) (lead pitch), 1.40 (0.055) (lead pitch), 0.51 (0.020) MAX. (lead width), 4.32 (0.170) MAX. (package width).</p> <p>Side view dimensions: 0.20 (0.008) (lead height), 0.33 (0.013) (lead height), 7.36 (0.290) (package length), 7.87 (0.310) (package length).</p>
200	<p>Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DESC Drawing part numbers contain provisions for lead finish.</p>
300	<p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads.</p>  <p>Top view dimensions: 0.51 (0.020) MIN. (lead width), 2.29 (0.090) (lead pitch), 2.79 (0.110) (lead pitch), 1.40 (0.055) (lead pitch), 1.65 (0.065) (lead pitch), 0.51 (0.020) MAX. (lead width), 5.57 (0.180) MAX. (package width).</p> <p>Side view dimensions: 5° MAX. (lead angle), 0.20 (0.008) (lead height), 0.33 (0.013) (lead height), 9.65 (0.380) (package length), 9.91 (0.390) (package length), 5.57 (0.180) MAX. (package width).</p>
600	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. Contact factory for the availability of this option on DESC part types.</p>  <p>Top view dimensions: 0.51 (0.020) MIN. (lead width), 2.29 (0.090) (lead pitch), 2.79 (0.110) (lead pitch), 1.02 (0.040) TYP. (lead pitch), 3.81 (0.150) MAX. (package width).</p> <p>Side view dimensions: 0.20 (0.008) (lead height), 0.33 (0.013) (lead height), 7.36 (0.290) (package length), 7.87 (0.310) (package length).</p>

Note: Dimensions in millimeters (inches).

Electrical Characteristics $T_A = -55^{\circ}\text{C}$ to 125°C , unless otherwise specified. See note 16.

Parameter		Symbol	Conditions	Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Input Threshold Current		I _{TH+}	V _{IN} = V _{TH+} ; V _{CC} = 4.5 V; V _O = 0.4 V; I _O ≥ 2.6 mA	1, 2, 3	1.75	2.5	3.20	mA		
		I _{TH-}	V _{IN} = V _{TH-} ; V _{CC} = 4.5 V; V _O = 2.4 V; I _{OH} ≤ 250 μA	1, 2, 3	0.93	1.3	1.62	mA		
Input Threshold Voltage	dc (Pins 2, 3)	V _{TH+}	V _{IN} = V ₂ – V ₃ ; Pins 1 & 4 Open V _{CC} = 4.5 V; V _O = 0.4 V; I _O ≥ 2.6 mA	1, 2, 3	3.18	3.6	4.10	V	1, 2	7
		V _{TH-}	V _{IN} = V ₂ – V ₃ ; Pins 1 & 4 Open V _{CC} = 4.5 V; V _O = 2.4 V; I _O ≤ 250 μA	1, 2, 3	1.90	2.5	3.00	V		
	ac (Pins 1, 4)	V _{TH+}	V _{IN} = V ₁ – V ₄ ; Pins 2 & 3 Open V _{CC} = 4.5 V; V _O = 0.4 V; I _O ≥ 2.6 mA	1, 2, 3	3.79	5.0	5.62	V		7, 8
		V _{TH-}	V _{IN} = V ₁ – V ₄ ; Pins 2 & 3 Open V _{CC} = 4.5 V; V _O = 2.4 V; I _O ≤ 250 μA	1, 2, 3	2.57	3.7	4.52	V		
Input Clamp Voltage		V _{IHC1}	V _{IHC1} = V ₂ – V ₃ ; V ₃ = GND; I _{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1, 2, 3	5.3	5.9	6.7	V	3	15
		V _{IHC2}	V _{IHC2} = V ₁ – V ₄ ; I _{IN} = 10 mA; Pins 2 & 3 Open	1, 2, 3	6.0	6.6	7.4	V		
		V _{IHC3}	V _{IHC3} = V ₂ – V ₃ ; V ₃ = GND; I _{IN} = 15 mA; Pins 1 & 4 Open	1, 2, 3		12.0	13.0	V		
Input Current		I _{IN}	V _{IN} = V ₂ – V ₃ = 5.0 V; Pins 1 & 4 Open	1, 2, 3	3.0	3.9	4.5	mA	4	
Logic Low Output Voltage		V _{OL}	V _{CC} = 4.5 V; I _{OL} = 2.6 mA	1, 2, 3		0.05	0.4	V	4	7
Logic High Output Current		I _{OH}	V _{OH} = V _{CC} = 18 V	1, 2, 3			250	μA		
Logic Low Supply Current		I _{CCL}	V ₂ – V ₃ = 5.0 V; V _O = Open; V _{CC} = 18 V	1, 2, 3		0.8	3.0	mA		
Logic High Supply Current		I _{CCH}	V _{CC} = 18 V; V _O = Open	1, 2, 3		0.001	20	μA	5	
Input-Output Insulation		I _{LO}	45% RH, t = 5 s; V _{LO} = 1500 Vdc; T _A = 25°C	1			1	μA		9, 10

Electrical Characteristics $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{ V}$, unless otherwise specified (continued).

Parameter	Symbol	Conditions		Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t _{PHL}	R _L = 1.8 kΩ, C _L = 15 pF		9, 10, 11		4	20	μs	6, 7	6, 11
Propagation Delay Time to Logic High Output Level	t _{PLH}	R _L = 1.8 kΩ, C _L = 15 pF		9, 10, 11		8	40	μs		6, 12
Logic High Common Mode Transient Immunity	CM _H	V _{CM} = 50 V	T _A = 25°C I _{IN} = 0 mA	9	1000	≥ 10,000		V/μs	8	13, 14, 17
		V _{CM} = 450 V				≥ 10,000				
Logic Low Common Mode Transient Immunity	CM _L	V _{CM} = 50 V	T _A = 25°C I _{IN} = 4 mA	9	1000	≥ 5,000		V/μs		
		V _{CM} = 250 V				≥ 5,000				

*All typical values are at $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$ unless otherwise noted.

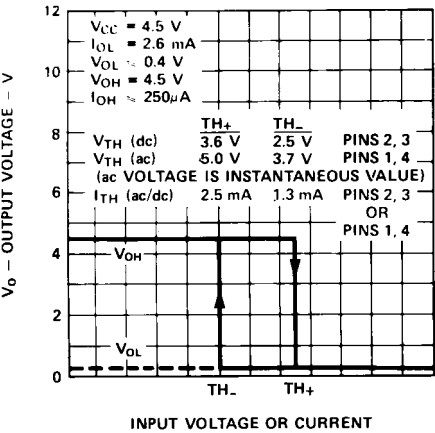


Figure 1. Typical Transfer Characteristics.

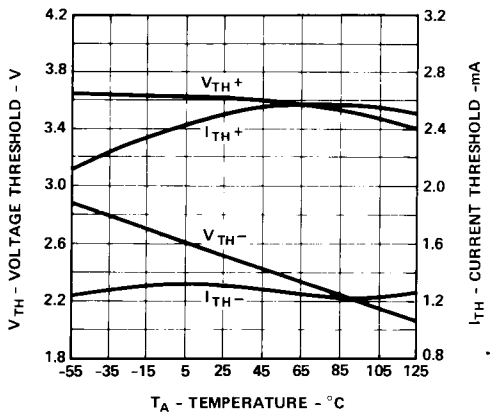


Figure 2. Typical dc Threshold Levels vs. Temperature.

Typical Characteristics All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Conditions	Fig.	Note
Hysteresis	I_{HYS}	1.2	mA	$I_{HYS} = I_{TH+} - I_{TH-}$	1	
	V_{HYS}	1.1	V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage	V_{ILC}	-0.76	V	$V_{ILC} = V_2 - V_3$; $V_3 = \text{GND}$; $I_{IN} = -10\text{ mA}$		
Bridge Diode Forward Voltage	$V_{D1,2}$	0.62		$I_{IN} = 3\text{ mA}$ (see schematic)		
	$V_{D3,4}$	0.73				
Input-Output Resistance	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500\text{ Vdc}$		9
Input-Output Capacitance	C_{I-O}	2.0	pF	$f = 1\text{ MHz}$, $V_{I-O} = 0\text{ Vdc}$		
Input Capacitance	C_{IN}	50	pF	$f = 1\text{ MHz}$; $V_{IN} = 0\text{ V}$, Pins 2 & 3, Pins 1 & 4 Open		
Output Rise Time (10-90%)	t_r	10	μs		7	
Output Fall Time (90-10%)	t_f	0.5	μs		7	

Notes:

- Maximum operating frequency is defined when output waveform (Pin 6) attains only 90% of V_{CC} with $R_L = 1.8\text{ k}\Omega$, $C_L = 15\text{ pF}$ using a 5 V square wave input signal.
- Measured at a point 1.6 mm below seating plane.
- Current into/out of any single lead.
- Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN} , must be observed.
- Derate linearly above 100°C free-air temperature at a rate of $4.26\text{ mW}/^\circ\text{C}$. Maximum input power dissipation of 195 mW allows an input IC junction temperature of 150°C at an ambient temperature of $T_A = 125^\circ\text{C}$ with a typical thermal resistance from junction to ambient of $\theta_{JAi} = 235^\circ\text{C}/\text{W}$. The typical thermal resistance from junction to case is equal to $170^\circ\text{C}/\text{W}$. Excessive P_{IN} and T_J may result in device degradation.
- The 1.8 k Ω load represents 1 TTL unit load of 1.6 mA and the 4.7 k Ω pull-up resistor.
- Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+} . Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-} .
- The ac voltage is instantaneous voltage.
- Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, Pins 5, 6, 7, 8 connected together.
- This is a momentary withstand test, not an operating condition.
- The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 7).
- The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 7).
- Common mode transient immunity in Logic High level is the maximum tolerable dV_{CM}/dt of the common mode voltage, V_{CM} , to ensure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode voltage, V_{CM} , to ensure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{ V}$). See Figure 8.
- In applications where dV_{CM}/dt may exceed 50,000 V/ μs (such as static discharge), a series resistor, R_{CC} , should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω .
- D_1 and D_2 are Schottky diodes; D_3 and D_4 are zener diodes.
- Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and Class H parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively.)
- Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.

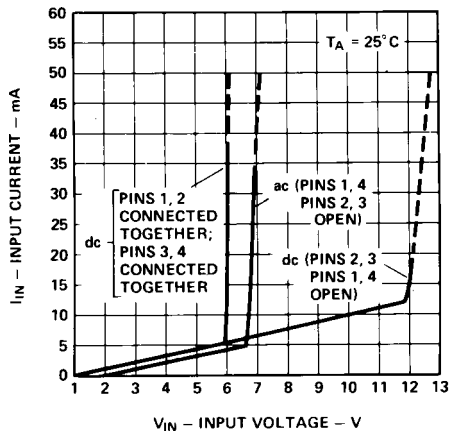


Figure 3. Typical Input Characteristics, I_{IN} vs. V_{IN} . (AC Voltage is Instantaneous Value.)

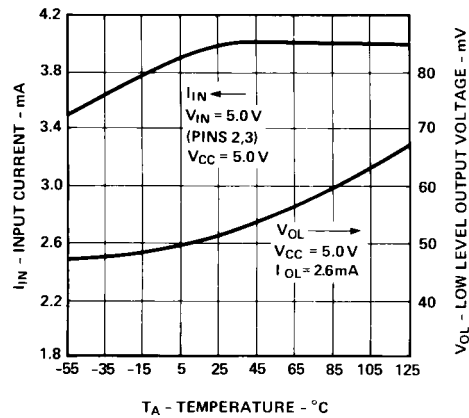


Figure 4. Typical Input Current, I_{IN} , and Low Level Output Voltage, V_{OL} , vs. Temperature.

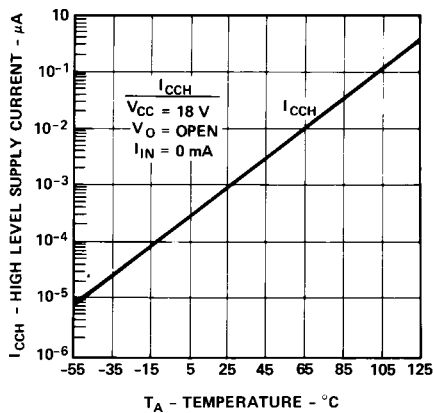


Figure 5. Typical High Level Supply Current, I_{CCH} vs. Temperature.

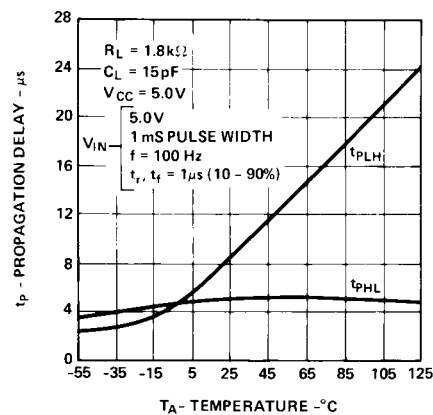


Figure 6. Typical Propagation Delay vs. Temperature.

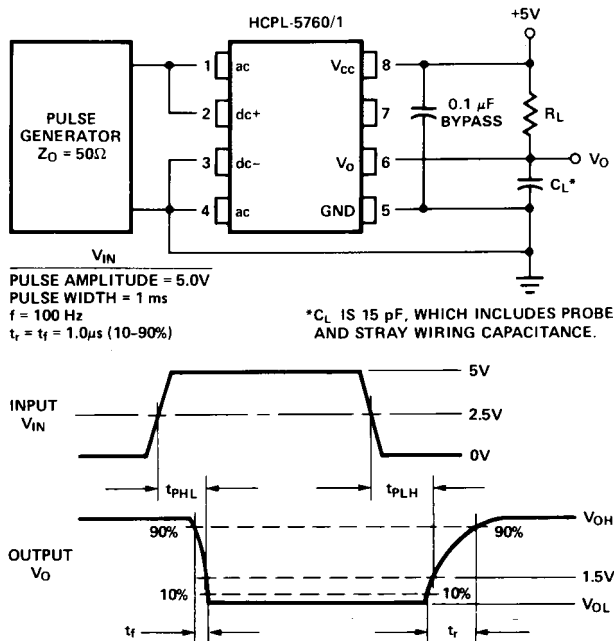


Figure 7. Switching Test Circuit.

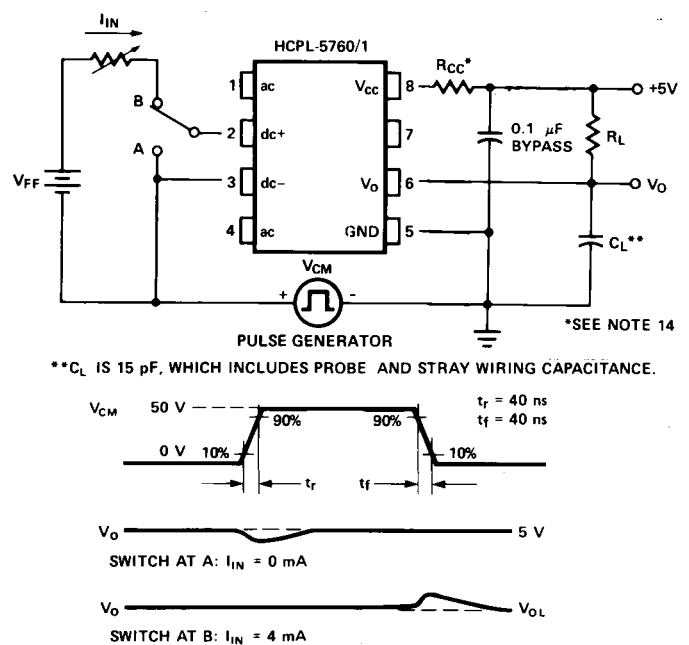


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Electrical Considerations

The HCPL-5760, HCPL-5761, or 5962-89477 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x , to determine larger external threshold voltage levels. For a desired external threshold voltage, V_{\pm} , a corresponding typical value of R_x can be obtained from Figure 10. Specific calculation of R_x can be obtained from Equation (1) of Figure 11. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 11 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts with a relay or switch, the HCPL-5760/1, or 5962-89477 combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 3). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where dV_{CM}/dt may be extremely large (such as static discharge), a series resistor, R_{CC} , should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively

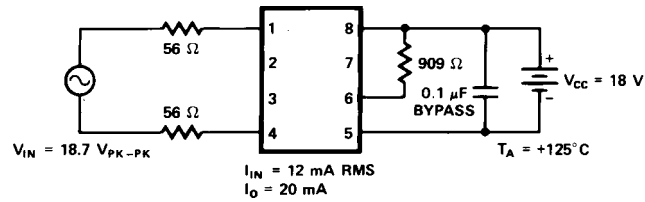


Figure 9. Operating Circuit for Burn-In and Steady State Life Tests.

high surge currents. See note 14 for determination of R_{CC} . In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μF to 0.1 μF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 k Ω and 20 μF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_- , R_x can be determined without use of R_p via

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (1)$$

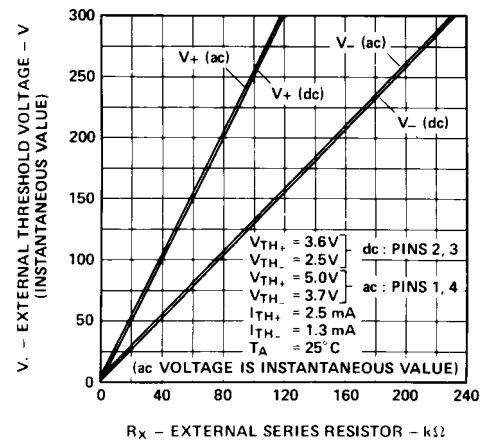


Figure 10. Typical External Threshold Characteristic, V_{\pm} vs. R_x .

For two specifically selected external threshold voltage levels, V_+ and V_- , the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met:

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-} (V_+) - V_{TH+} (V_-)}{I_{TH+} (V_{TH-}) - I_{TH-} (V_{TH+})} \quad (2)$$

$$R_p = \frac{V_{TH-} (V_+) - V_{TH+} (V_-)}{I_{TH+} (V_- - V_{TH-}) + I_{TH-} (V_{TH+} - V_+)} \quad (3)$$

See Application Note 1004 for more information.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H devices are also in compliance with DESC drawing 5962-89477.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

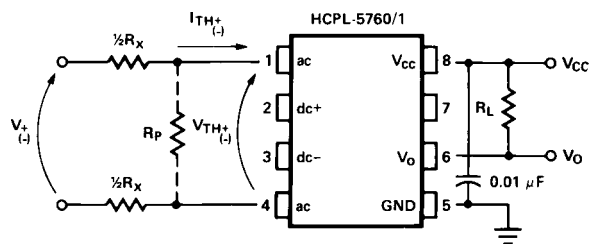


Figure 11. External Threshold Voltage Level Selection.