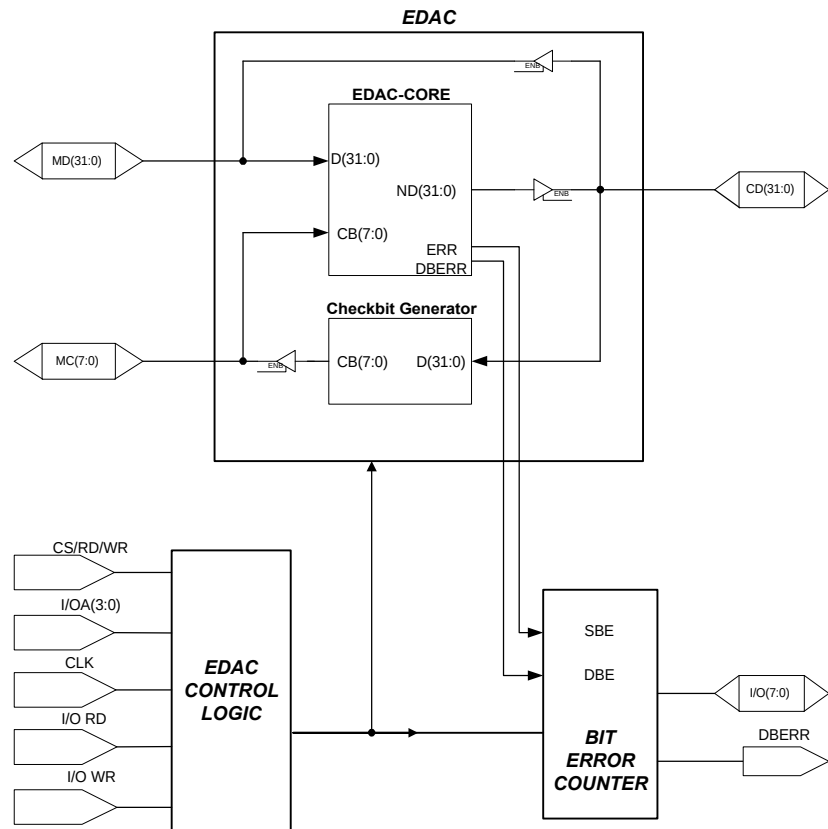
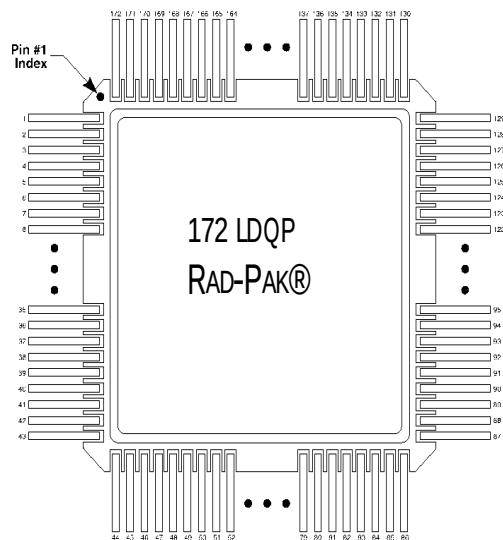




FEATURES:

- Operates as 8, 16, or 32 bit EDAC
- No single event latchup > 100 MeV/mg/cm²
- Single event upset $\geq$ IE = 10 upsets/day
- Total dose hardness 100 krad (Si) typical
- Package:
 - 172 pin RAD-PAK® quad flat pack
 - Weight: 20 grams
- Cascadable to 64 bit EDAC
- Flow-thru architecture
- Super-high speed
- Single and double bit error detection
- Single bit error counter
- Single bit auto-correct
- Double bit error counter
- No Read-Modify-Write required
- Absolute minimum gate usage

DESCRIPTION:

Space Electronics' 48D32DRP high speed CMOS DRAM EDAC (Error Detection and Correction) features a minimum 100 kilorad (Si) total dose tolerance. The 48D32DRP does not require Read-Modify-Write to memory for partial word writes, thus can be used as an 8, 16, or 32 bit EDAC. These partial-word writes may be done in single bus cycle without performance penalties. The 48D32DRP incorporates four separate byte-wide EDAC modules in parallel. Each module is broken down into two main blocks -- the check bit generator (CBG) and the read/correct data (CORR). The unique flow-thru architecture achieves 25ns from data in (MD) to corrected data out (CD). Two readable error counters allow single-bit error (ERR) and double-bit error (DBERR) tracking. Error signals can be internally masked via two mask bits. Capable of surviving space environments, the DRAM EDAC is ideal for satellite, spacecraft, and space probe missions. The RAD-PAK® technology incorporates radiation shielding in the micro-circuit package. It eliminates box shielding while providing lifetime in orbit. The DRAM EDAC is available with packaging and screening up to Class S.

TABLE 1. 48D32DRP PIN DESCRIPTION

NAME	SYMBOL	I/O	FUNCTION
Memory Data Bus	MD0-7, MD8-15, MD16-23, MD24-31	I/O	These I/O pines accept 8, or 16, or 32 bit data word from main memory for error detection and/or correction.
Memory CheckBit Bus	MC0-7, MC8-15, MC16-23, MC24-31	I/O	The memory checkbits of 8, or 16, or 32 bits pins accept checkbits from the checkbit memory for error detection and/or correction. They also output corrected checkbits to checkbit memory when the 48D32DRP is used in bi-directional configuration.
CPU Data Bus	CD0-7, CD8-15, CD16-23, CD24-31	I/O	Data from MD0-31 appears at these pins corrected when in memory read mode. Partial-writes are done without read-modify-writes.
Memory Read Bus	MEM_RD0-3	I	Allows read select for four SRAM modules when performing data writes to memory.
Memory Write Bus	MEM_WR0-3	I	Allows write select for four SRAM modules when performing data writes to memory.
I/O Read	IO_RD	I	Selects the internal I/O registers for read.
I/O Write	IO_WR	I	Selects the internal I/O registers for write.
SRAM Chip Select Bus	SRAM_CS0-3	I	Selects memory modules 0 to 3 for read or write modules.
Clock A	CLKIN_A	I	System clock for 48D32DRP.
Clock B	CLKIN_B	I	Internal error counter clock.
Reset	RESET	I	Global reset. Clears 48D32DRP EDAC cores to all zeros.
I/O Address Bus	IO_A0-2	I	Internal I/O register address bus.
Error Counter Bus	IO_OUT0-7	I/O	Internal I/O register data bus.
Double Bit Error	DBERR	O	Indicates a double bit error has occurred.

TABLE 2. 48D32DRP ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Voltage Supply	V_{CC}	-0.5	+7.0	V
Input Voltage	V_I	-0.5	$V_{CC} + 0.5$	V
Output Voltage	V_O	-0.5	$V_{CC} + 0.5$	V
I/O Source/Sink Current ²	I_{IO}	-20	+20	mA
Storage Temperature	T_{STG}	-65	+150	°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Condition.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5$ or less than GND -0.5V, the internal protection diode will be forward-biased and can draw excessive current.

TABLE 3. 48D32DRP RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNITS
Temperature Range ¹	-55	+125	°C
Power Supply Tolerance	-10	+10	%V _{CC}

1. Case temperature (T_C) is used.

TABLE 4. 48D32DRP DC ELECTRICAL SPECIFICATIONS

SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	LIMIT		UNITS
			MIN	MAX	
V _{OH} ¹	I _{OH} = -4 mA	1,2,3	3.7	--	V
V _{OL} ¹	I _{OL} = 4 mA	1,2,3	--	+0.4	V
V _{IH}		1,2,3	2.2	V _{CC} + 3	V
V _{IL}		1,2,3	-0.3	+0.8	V
Input Transition Time t _R , t _F ²		--	--	+500	ns
C _{IO} , I/O Capacitance ²		4	--	+20	pF
I _{IH} , I _{IL}	V _{IN} = V _{CC} or GND, V _{CC} = 5.5V	1,2,3	-10	+10	μA
I _{OZH} , I _{OZL}	V _{OUT} = V _{CC} or GND, V _{CC} = 5.5V	1,2,3	-10	+10	μA
I _{CC} Standby ³		1,2,3	--	25	mA
I _{CC} Active ^{3,4}		1,2,3	--	325 typ	mA

1. Only one output tested at a time. V_{CC} = min.

2. Not tested, for information only.

3. All outputs unloaded. All inputs = V_{CC} or GND.

4. At 50 MHz.

TABLE 5. 48D32DRP AC ELECTRICAL CHARACTERISTICS

PROPAGATION DELAY FROM INPUT	TO OUTPUT			UNIT
	CD DATA OUT	ERR SINGLE BIT ERROR	DBERR SINGLE BIT ERROR	
MD Data In	25 max	25 max	25 max	nS

TABLE 6. 48D32DRP PIN ASSIGNMENT

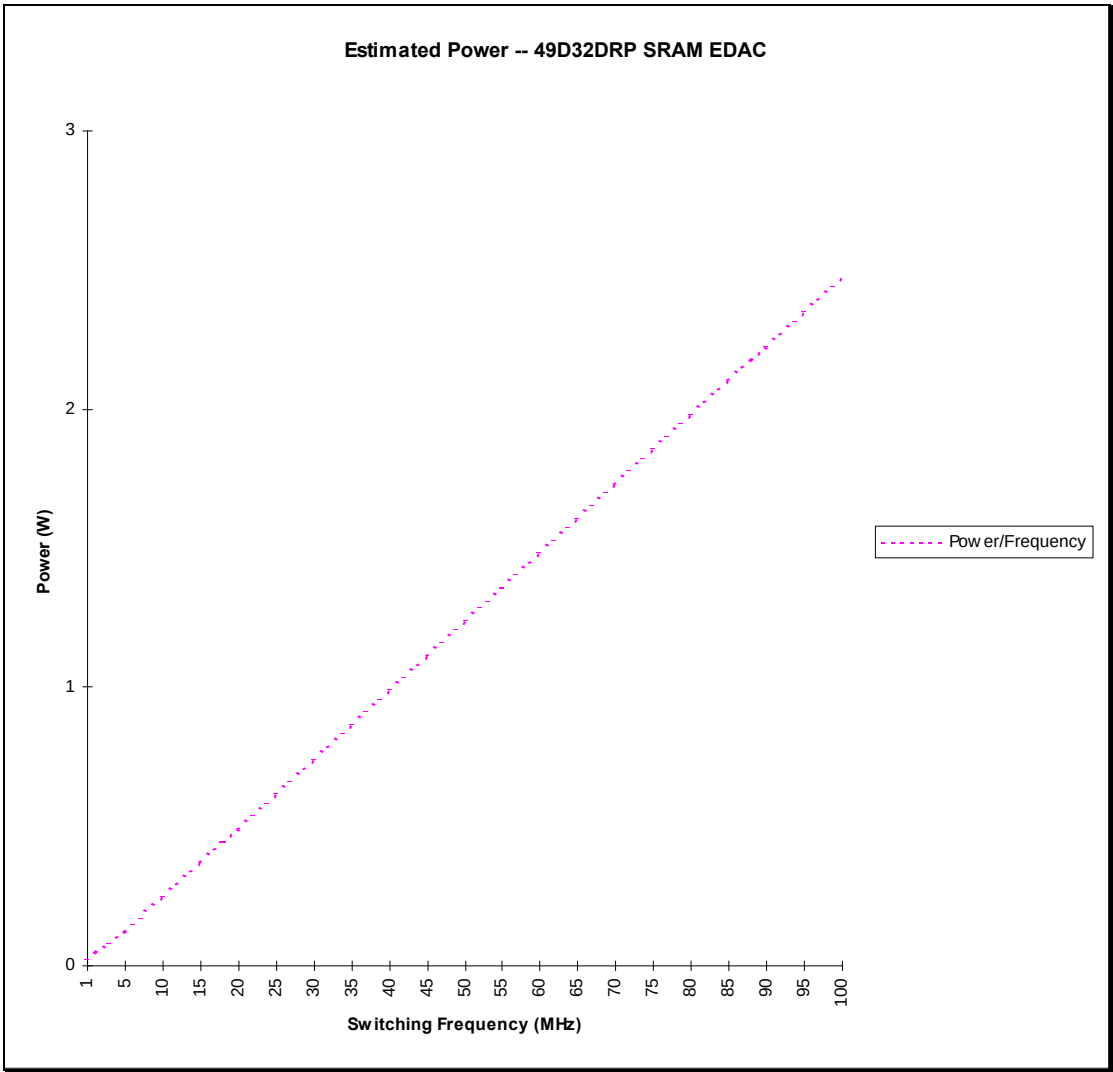
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
GND	--	59	MC6	118	CD2

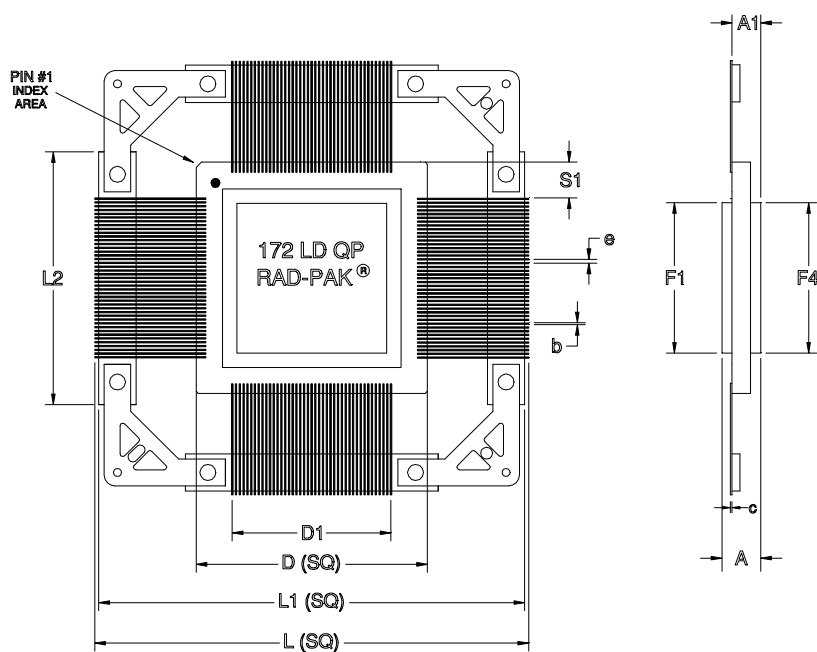
TABLE 6. 48D32DRP PIN ASSIGNMENT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	--	60	MC7	119	CD3
2	MD0	61	MC8	120	CD4
3	MD1	62	MC9	121	CD5
4	MD2	63	MC10	122	CD6
5	MD3	64	MC11	123	GND
6	MD4	65	GND	124	CD7
7	GND	66	V _{cc}	125	CD8
8	MD5	67	NC	126	CD9
9	MD6	68	MC12	127	CD10
10	MD7	69	MC13	128	CD11
11	MEM_RD0	70	MC14	129	CD12
12	V _{cc}	71	MC15	GND	--
13	MEM_RD1	72	MC16	130	CD13
14	MD8	73	MC17	131	(SDI)*
15	MD9	74	MC18	132	CD14
16	MD10	75	GND	133	CD15
17	GND	76	MC19	134	SRAM_CS0
18	MD11	77	MC20	135	SRAM_CS1
19	MD12	78	MC21	136	V _{cc}
20	MD13	79	I)_RD	137	SRAM_CS2
21	MD14	80	V _{cc}	138	SRAM_CS3
22	GND	81	IO_WR	139	CD16
23	V _{cc}	82	MC22	140	CD17
24	V _{cc}	82	MC23	141	GND
25	MD15	84	MC24	142	CD18
26	MEM_RD2	85	MC25	143	CD19
27	V _{cc}	86	MC26	144	CD20
28	MEM_RD3	GND	--	145	CD21
29	MD16	87	MC27	146	CD22
30	MD17	88	MC28	147	CD23
31	MD18	89	MC29	148	CD24
32	GND	90	MC30	149	NC
33	MD19	91	MC31	150	CLKIN
34	MD20	92	IO_OUT_D0	151	V _{cc}
35	MD21	93	IO_OUT_D1	152	GND
36	MD22	94	IO_OUT_D2	153	CD25
37	GND	95	IO_OUT_D3	154	SPARE4

TABLE 6. 48D32DRP PIN ASSIGNMENT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
38	MD23	96	IO_OUT_D4	155	CD26
39	MD24	97	IO_OUT_D5	156	CD27
40	MD25	98	GND	157	CD28
41	MD26	99	IO_OUT_D6	158	CD29
42	MD27	100	IO_OUT_D7	159	CD30
43	MD28	101	IO_A0	160	CD31
GND	--	102	IO_A1	161	GND
44	MD29	103	GND	162	NC
45	MD30	104	IO_A2	163	NC
46	MD31	105	CS_IO	164	NC
47	MEM_WR0	106	GND	165	NC
48	MEM_WR1	107	V _{CC}	166	V _{CC}
49	MEM_WR2	108	GND	167	NC
50	V _{CC}	109	V _{CC}	168	NC
51	MEM_WR3	110	V _{CC}	169	NC
52	MC0	111	DBERR	170	NC
53	MC1	112	RESET	171	NC
54	MC2	113	V _{CC}	172	NC
55	GND	114	NC	GND	--
56	MC3	115	CD0	GND	--
57	MC4	116	CD1		
58	MC5	117	CD2		





172 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.116	0.133	0.146
b	0.007	0.008	0.013
c	0.004	0.006	0.009
D	1.138	1.150	1.162
D1	1.050 BSC		
e	0.025 BSC		
S1	0.013	0.046	--
F1	0.890	0.895	0.900
F4	0.881	0.890	0.899
L	2.500	2.520	2.540
L1	2.485	2.500	2.505
L2	1.690	1.700	1.710
A1	0.079	0.091	0.103
N	172		

Q172-01

Note: All dimensions in inches

Important Notice:

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