

CMOS DUAL UP COUNTERS

FEATURES

- ◆ Two Independent 4-Bit Counters
- ◆ Internally Synchronous for High Speed
- ◆ Dual BCD (4518B) and Dual Binary (4520B) Configurations
- ◆ Direct Reset
- ◆ Logic Edge-Clocked Design
- ◆ Trigger from either Edge of Clock Signal
- ◆ Static Operation— DC to 5MHz @ 10Vdc

DESCRIPTION

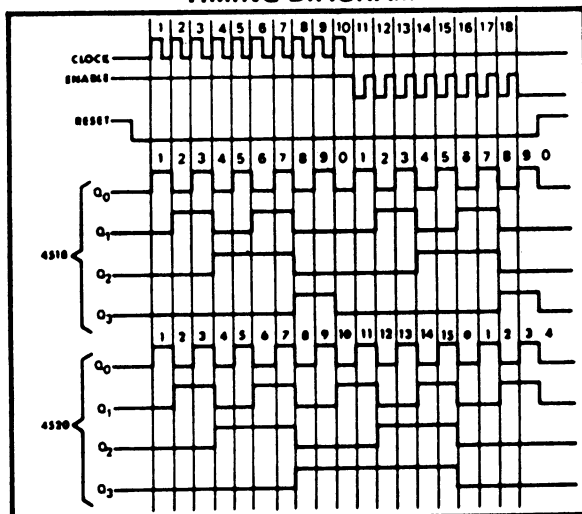
The 4518B Dual BCD Counter and the 4520B Dual Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type-D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the 4518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

TRUTH TABLE

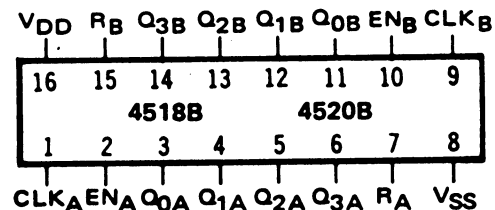
CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

TIMING DIAGRAM



CONNECTION DIAGRAM (all packages)

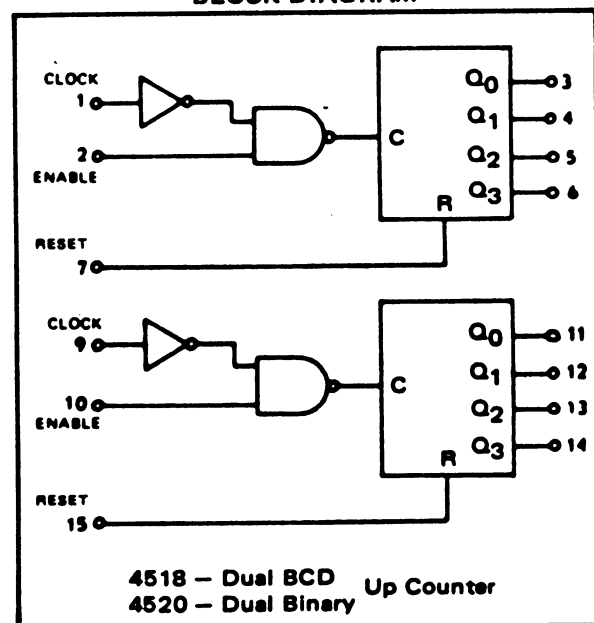


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ³		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C

= -40°C for E

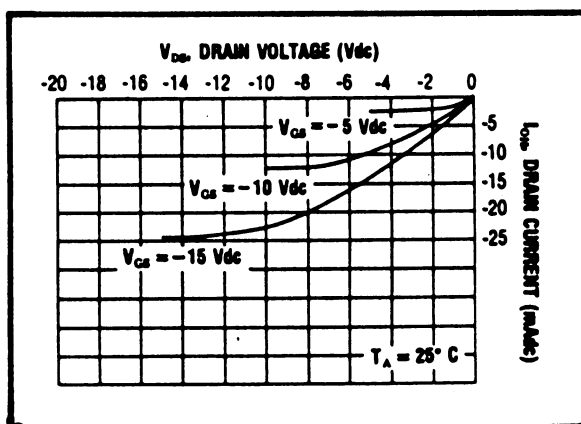
T_{HIGH} = +125°C for C

= +85°C for E

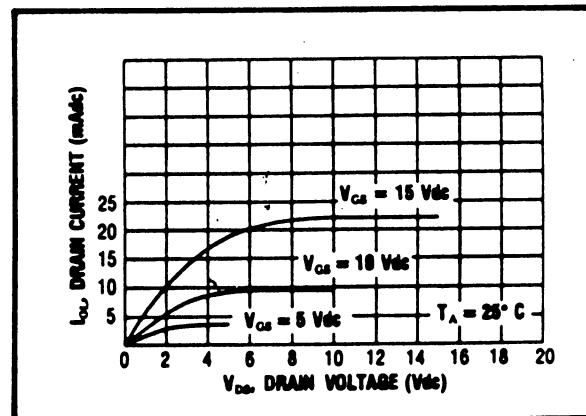
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock or Clock Enable	t _{PLH} , t _{PHL}	5 10 15	— — —	225 100 80	450 200 160	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	100 50 35	200 100 70	ns
MINIMUM CLOCK ENABLE PULSE WIDTH	PW _{CE}	5 10 15	— — —	200 100 70	400 200 140	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	1.5 3.0 4.0	3.0 6.0 8.0	— — —	MHz
MAXIMUM CLOCK OR CLOCK ENABLE RISE & FALL TIME ¹	t _{CL} , t _{CL}	5 10 15	15 5 5	— — —	— — —	μs
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5 10 15	— — —	225 100 80	450 200 160	ns
MINIMUM RESET PULSE WIDTH	PW _R	5 10 15	— — —	120 50 40	240 100 80	ns
RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	100 50 40	200 100 80	ns

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

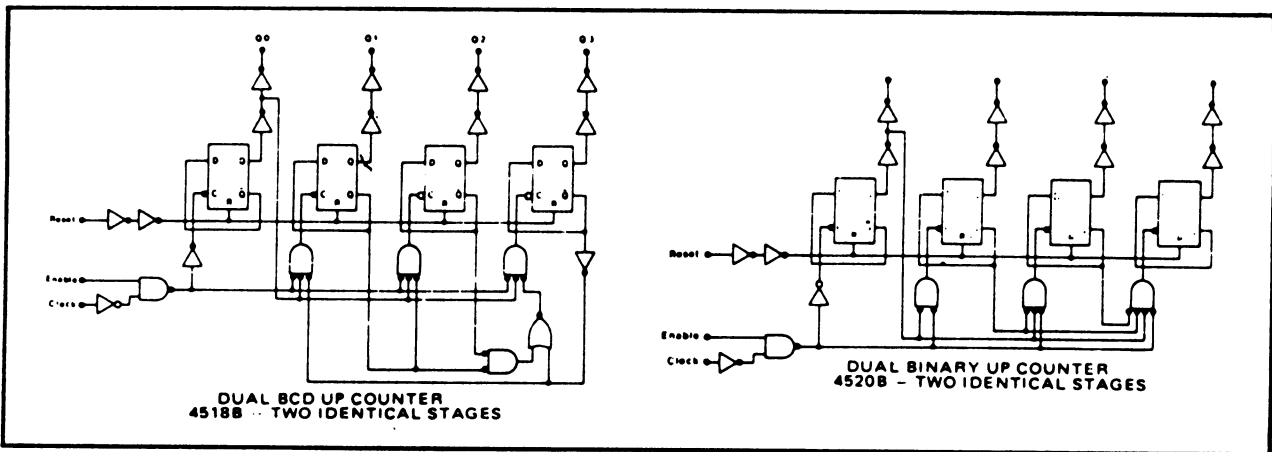


Typical P-Channel
Source Current Characteristics

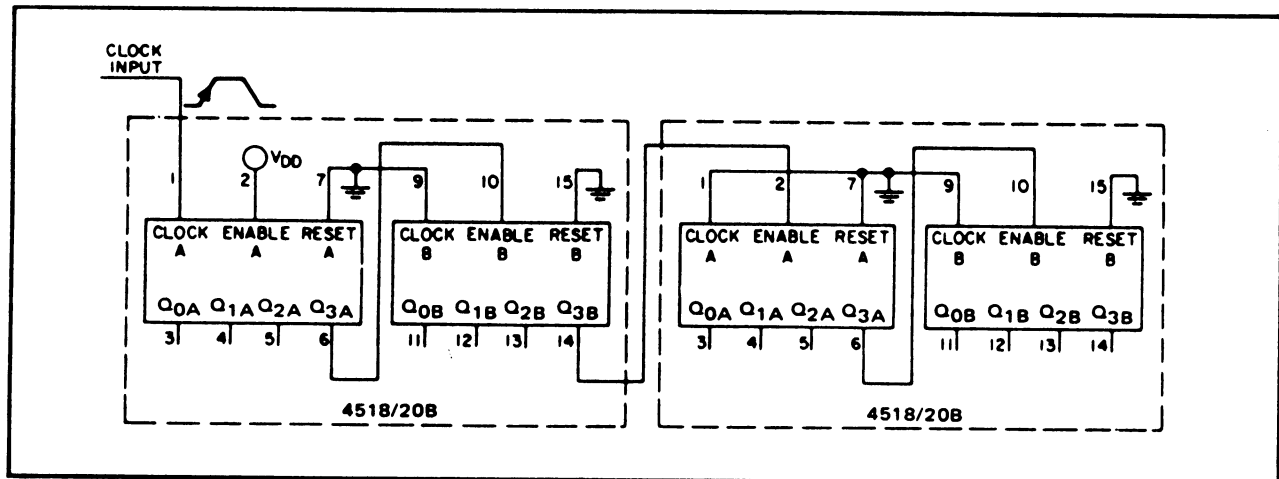


Typical N-Channel
Sink Current Characteristics

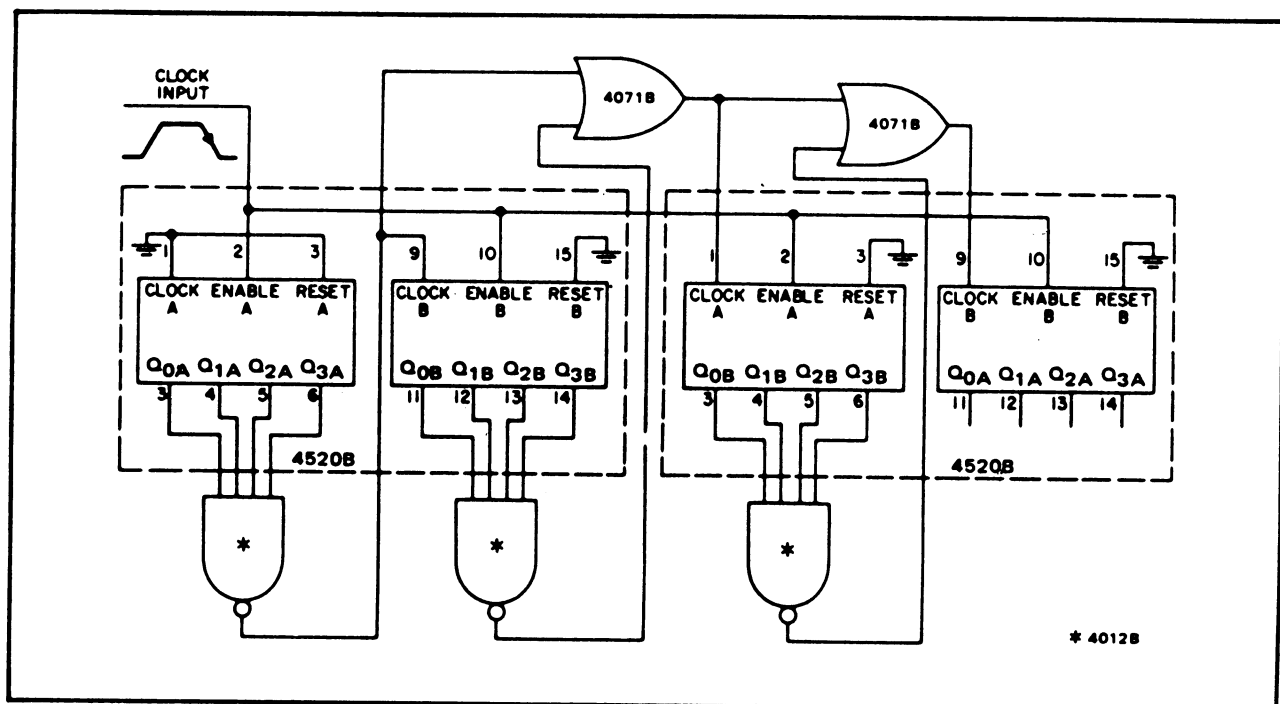
LOGIC DIAGRAMS



APPLICATIONS INFORMATION



Ripple cascading of four counters with positive-edge triggering.



Synchronous cascading of four binary counters with negative-edge triggering.