

CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- ◆ **High-Current Sourcing Bipolar Outputs (Up to 25 mA)**
- ◆ **Latched Storage of Input Code**
- ◆ **Blanking Input for Display Intensity Modulation**
- ◆ **Lamp Test Provision**
- ◆ **Readout Blanking for Illegal Input Combinations**

DESCRIPTION

The 4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

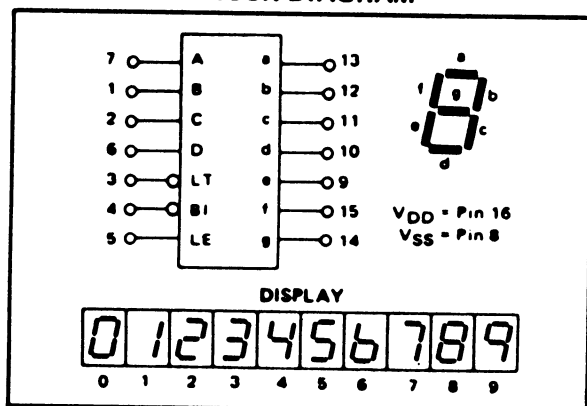
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	0	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	0	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	0	0	1	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*	*	*	*	*	*	*	*

X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

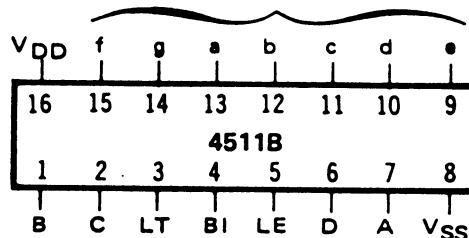
BLOCK DIAGRAM



CONNECTION DIAGRAM

(all packages)

Segment Outputs



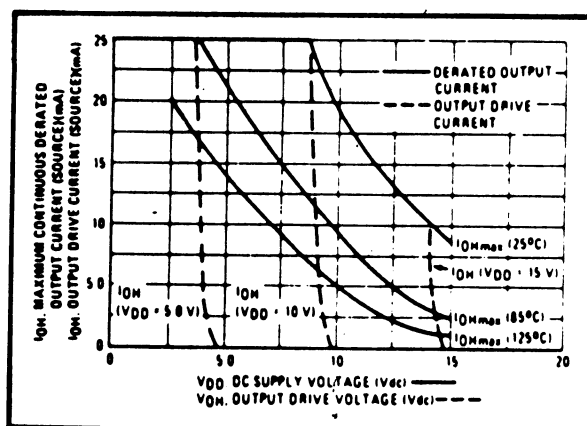
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
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Operating Temperature T_A

C	-55 to +125 °C
E	-40 to +85 °C



Typical P-Channel Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+ 25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA _{dc}
			—	10	—	0.1	10	—	300	
OUTPUT DRIVE VOLTAGE	V _{OUT}	I _{OH} = 0 mA _{dc} — 5 — 10 — 15 — 20 — 25	4.99	—	4.99	5.0	—	4.95	—	V _{dc}
			—	—	—	4.25	—	—	—	
			—	—	3.9	4.13	—	—	—	
			—	—	—	3.95	—	—	—	
			—	—	3.4	3.75	—	—	—	
			—	—	—	3.5	—	—	—	
		I _{OH} = 0 mA _{dc} — 5 — 10 — 15 — 20 — 25	9.99	—	9.99	10	—	9.95	—	V _{dc}
			—	—	—	9.25	—	—	—	
			—	—	9.0	9.15	—	—	—	
			—	—	—	9.03	—	—	—	
			—	—	8.6	8.90	—	—	—	
			—	—	—	8.75	—	—	—	
		I _{OH} = 0 mA _{dc} — 5 — 10 — 15 — 20 — 25	14.99	—	14.99	15	—	14.96	—	V _{dc}
			—	—	—	14.25	—	—	—	
			—	—	14.0	14.18	—	—	—	
			—	—	—	14.08	—	—	—	
			—	—	13.6	13.95	—	—	—	
			—	—	—	13.80	—	—	—	
OUTPUT LOW (SINK) CURRENT	I _{OL}	V _{OL} = 0.4V	1.2	—	0.9	1.5	—	0.7	—	mA _{dc}
		V _{OL} = 0.5V	1.9	—	1.7	4.0	—	1.4	—	
		V _{OL} = 1.5V	10.0	—	9.0	11.0	—	7.5	—	
		V _{IN} = V _{SS} or V _{DD}	—	—	—	—	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "40006 Series Family Specifications".
² T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t _{PLH}	5	—	520	ns
		10	—	210	
		15	—	150	
	t _{PHL}	5	—	660	ns
		10	—	260	
		15	—	180	
From Blanking Input	t _{PLH}	5	—	300	ns
		10	—	125	
		15	—	100	
	t _{PHL}	5	—	500	ns
		10	—	200	
		15	—	160	
From Lamp Test Input	t _{PLH}	5	—	300	ns
		10	—	120	
		15	—	90	
	t _{PHL}	5	—	325	ns
		10	—	130	
		15	—	95	
OUTPUT TRANSITION TIME	t _{TLH}	5	—	170	ns
		10	—	120	
		15	—	100	
	t _{THL}	5	—	400	ns
		10	—	225	
		15	—	200	
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	—	90	ns
		10	—	40	
		15	—	20	
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	90	ns
		10	—	40	
		15	—	20	
MINIMUM LATCH ENABLE PULSE WIDTH	PW _{LE}	5	—	260	ns
		10	—	110	
		15	—	65	

LOGIC DIAGRAM

