

CMOS 8-STAGE BINARY COUNTER

FEATURES

- ◆ 8-Stage Synchronous Counter
- ◆ Buffered Outputs from all 8 Stages
- ◆ Direct Reset
- ◆ Fully Static Operation — DC to 8MHz @ 10Vdc

DESCRIPTION

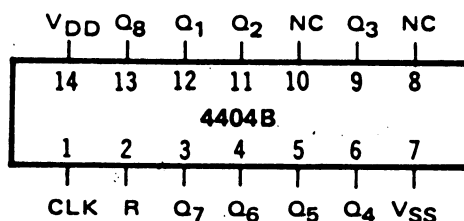
The 4404B consists of eight synchronous, single-phase clocked counting stages, with the Q output of each stage accessible. The counter is reset to all "zeroes" by a high level on the Reset line. Each stage of the counter utilizes a master-slave flip-flop configuration. The state of the counter is advanced one step in binary order on the negative-going transition of the input clock pulse.

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

CONNECTION DIAGRAM (all packages)



Add suffix for package:

C 14-pin Cerdip

E 14-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

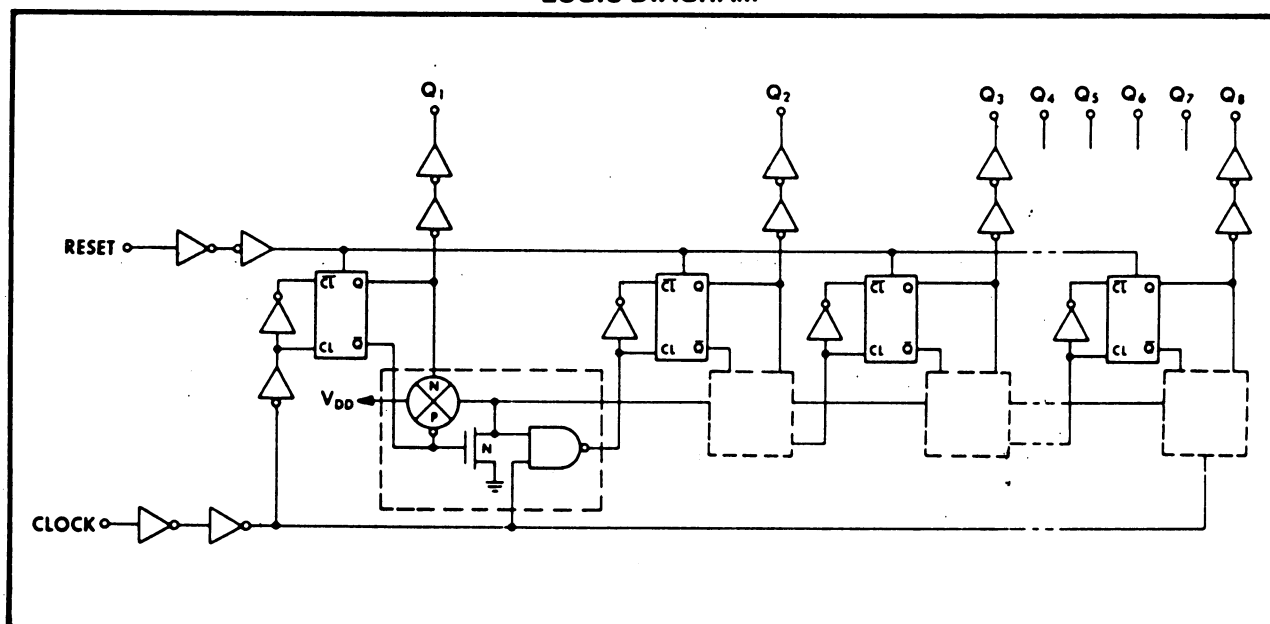
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C -55 to +125 °C

E -40 to +85 °C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	
			—	—	—	—	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C

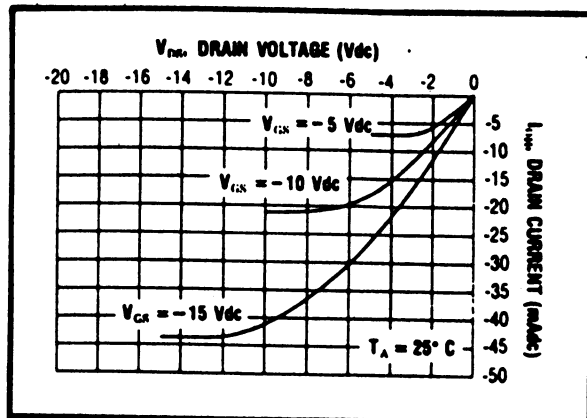
= -40°C for E

T_{HIGH} = +125°C for C

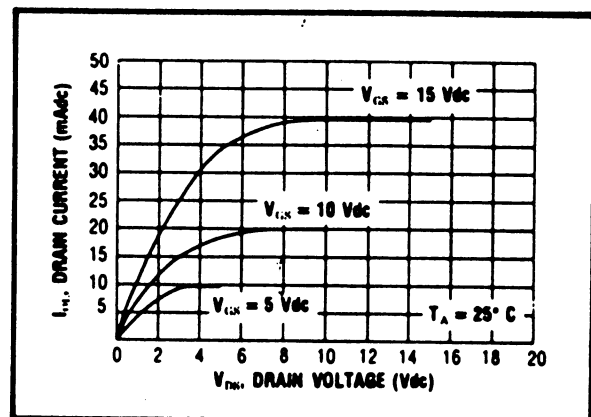
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{Dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5 10 15	— — —	250 125 100	500 250 200	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	125 65 50	250 130 100	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	2.0 4.0 5	4.0 8.0 10	— — —	MHz
MAXIMUM CLOCK RISE AND FALL TIME	t _{CL} , t _{CL}	5 10 15	15 5 3	— — —	— — —	μs
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5 10 15	— — —	175 75 60	350 150 120	ns
MINIMUM RESET PULSE WIDTH	PW _R	5 10 15	— — —	100 50 40	200 100 80	ns
RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	200 90 65	400 180 130	ns



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics