R&E INTERNATIONAL, INC.

CMOS 4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of All Stages
- J-$\overline{K}$ Serial Inputs to First Stage
- Asynchronous True/Complement Control of all Outputs
- Asynchronous Reset
- Static Operation – DC to 6MHz @ 10Vdc

DESCRIPTION

The 4035B is a Four-Stage Clocked Serial Register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is high. In the parallel or serial mode information is transferred on positive Clock transitions.

When the True/Complement control is high, the true contents of the register are available at the output terminals. When the True/Complement control is low, the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the Clock signal.

J$\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements, particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common Reset is also provided.

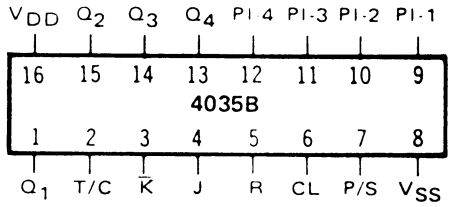
This device may be used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, and sample-and-hold registers.

TRUTH TABLE

	t_{n-1} (Inputs)				t_n (Outputs)
CL	J	$\overline{K}$	R	Q_{n-1}	Q_n
⎍	0	X	0	0	0
⎍	1	X	0	0	1
⎍	X	0	0	1	0
⎍	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ Toggle Mode
⎍	X	1	0	1	1
⎎	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 16-pin Cerdip

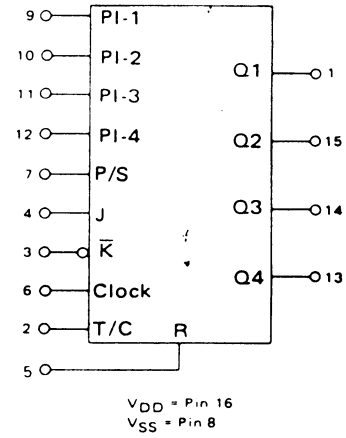
E 16-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

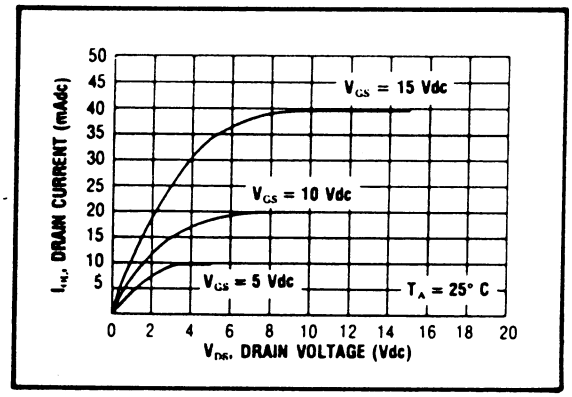
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

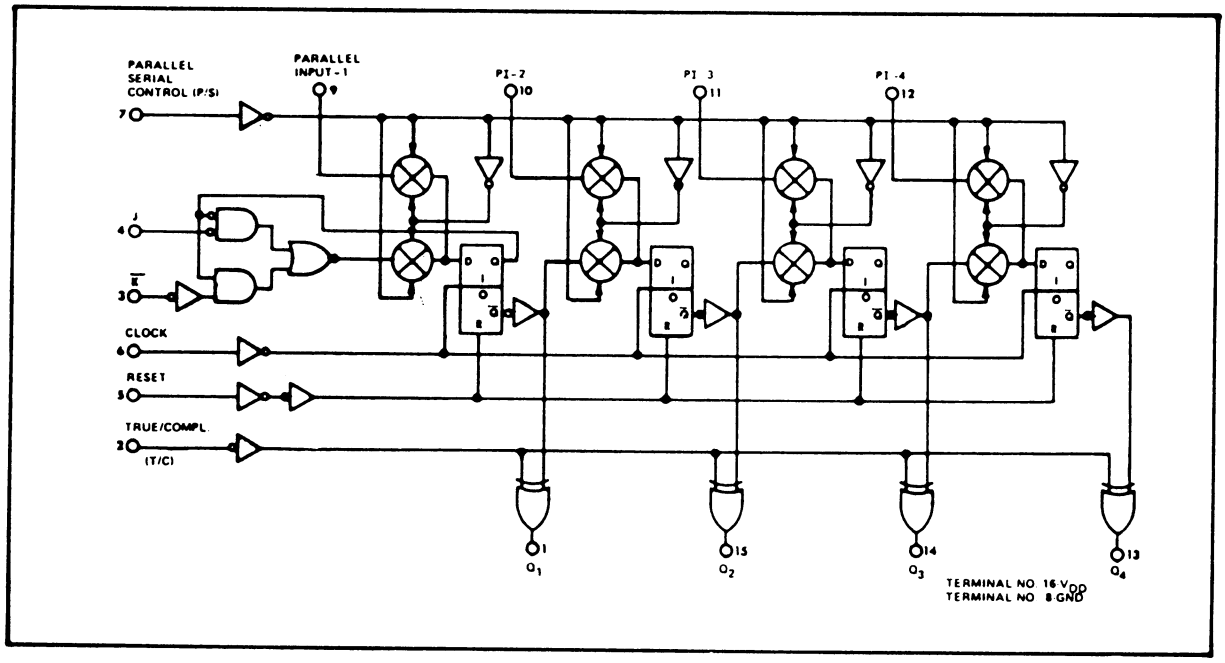
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock Input	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
From T/C Input	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	100	200	ns
		10	–	45	90	
		15	–	30	60	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	4.0	–	MHz
		10	5.0	10.0	–	
		15	6.0	12.0	–	
MAXIMUM CLOCK RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME J, K Inputs	t_{setup}	5	–	110	220	ns
		10	–	40	80	
		15	–	30	60	
P/S, Parallel Inputs	t_{setup}	5	–	70	140	ns
		10	–	25	50	
		15	–	20	40	
MINIMUM HOLD TIME J, K inputs	t_{hold}	5	–	-25	25	ns
		10	–	-10	10	
		15	–	- 5	5	
P/S, Parallel Inputs	t_{hold}	5	–	-25	25	ns
		10	–	-10	10	
		15	–	- 5	5	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	230	460	ns
		10	–	120	240	
		15	–	90	180	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	125	250	ns
		10	–	55	110	
		15	–	40	80	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

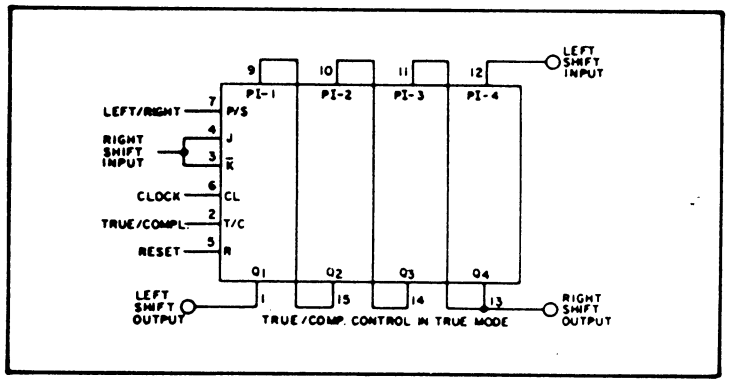


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION



Shift Left/Shift Right Register