

8-BIT ADDRESSABLE LATCH

FEATURES

- Serial data input
- Active parallel output
- Storage register capability
- Master clear
- Can function as demultiplexer

APPLICATIONS

- Multi-line decoders
- A/D converters

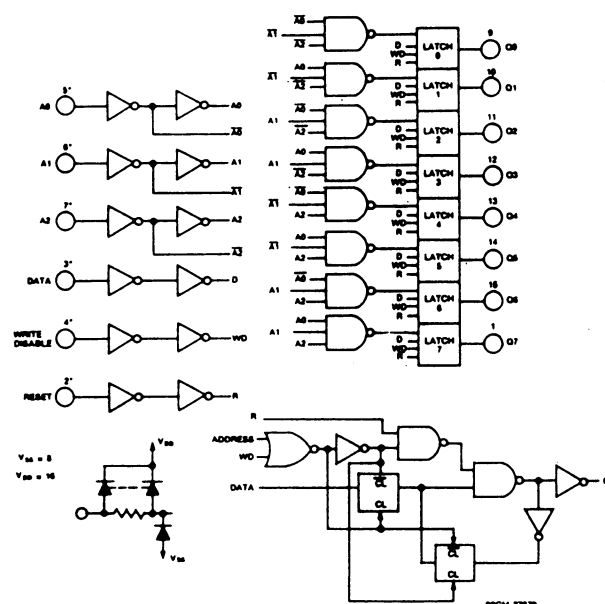
DESCRIPTION

The 4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

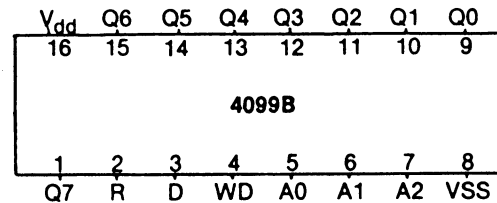
A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

LOGIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COSMOS PROTECTION NETWORK

CONNECTION DIAGRAM



TRUTH TABLE

WD	R	Addressed Latch	Unaddressed Latch
0	0	D	Holds previous data
0	1	D	0
1	0	Holds previous data	
1	1	0	0

TIMING DIAGRAMS

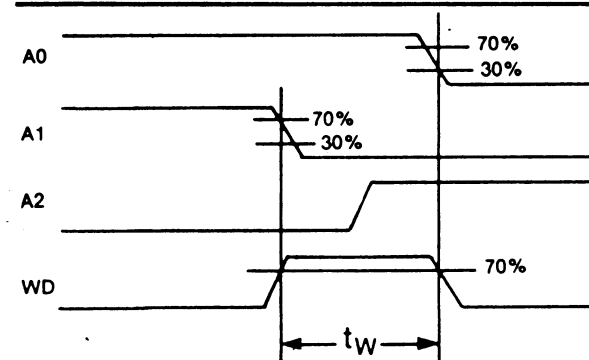


Fig. 1 — Definition of WRITE DISABLE ON time.

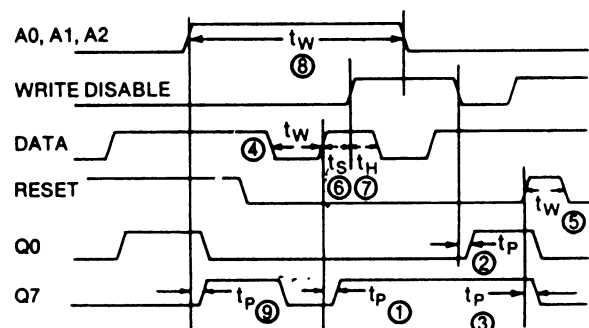


Fig. 2 — Master timing diagram.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 2}

PARAMETER	V _{DD}	I _{LOW2}		+ 25°C			T _{HIGH}		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE I _{DD} CURRENT	5	—	5	—	0.02	5	—	150	μ A
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	

DYNAMIC CHARACTERISTICS

T_A = 25° C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 K

CHARACTERISTIC	SEE FIG 2*	V _{DD} (V)	LIMITS ALL PACKAGE TYPES TYP. MAX.	UNITS
Propagation Delay: t _{PLH} , t _{PHL}	(1)	5 10 15	200 75 50	400 150 100
Data to Output WRITE DISABLE to Output. t _{PLH} , t _{PHL}	(2)	5 10 15	200 80 60	400 160 120
Reset to Output, t _{PHL}	(3)	5 10 15	175 80 65	350 160 130
Address to Output, t _{PLH} , t _{PHL}	(9)	5 10 15	225 100 75	450 200 150
Transition Time, T _{THL} , (Any Output) t _{TLH}		5 10 15	100 50 40	200 100 80
Minimum Pulse Width, t _W Data	(4)	5 10 15	100 50 40	200 100 80
Address	(8)	5 10 15	200 100 65	400 200 125
Reset	(5)	5 10 15	75 40 25	150 75 50
Minimum Setup Time, t _s Data to WRITE DISABLE	(6)	5 10 15	50 25 20	100 50 35
Minimum Hold Time, t _H Data to WRITE DISABLE	(7)	5 10 15	75 40 25	150 75 50
Average Input Capacitance C ₁	Any Input		5	—
				pF

*Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 1).