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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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Silicon N-Channel/P-Channel Complementary Power MOS FET Array



ADE-208-1212 (Z) 1st. Edition Mar. 2001

Application

High speed power switching

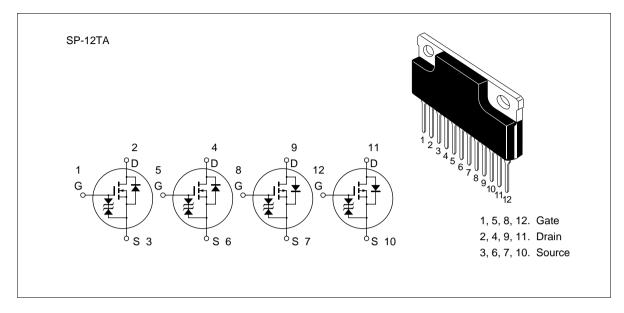
Features

Low on-resistance

N-channel: $R_{DS(on)} \le 0.17$, $V_{GS}=10$ V, $I_D=4$ A P-channel: $R_{DS(on)} \le 0.2$, $V_{GS}=-10$ V, $I_D=-4$ A

- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



Absolute Maximum Ratings $(Ta = 25^{\circ}C)$

		Ratings			
Item	Symbol	Nch	Pch	 Unit	
Drain to source voltage	$V_{\scriptscriptstyle DSS}$	60	-60	V	
Gate to source voltage	$V_{\sf GSS}$	±20	±20	V	
Drain current	I _D	8	-8	Α	
Drain peak current	I _{D(pulse)} *1	32	-32	A	
Body to drain diode reverse drain current	I _{DR}	8	-8	А	
Channel dissipation	Pch (Tc = 25°C)*2	32		W	
Channel dissipation	Pch*2	4		W	
Channel temperature	Tch	150		°C	
Storage temperature	Tstg	-55 to -	+150	°C	

Notes: 1. PW \leq 10 µs, duty cycle \leq 1%

2. 4 devices operation

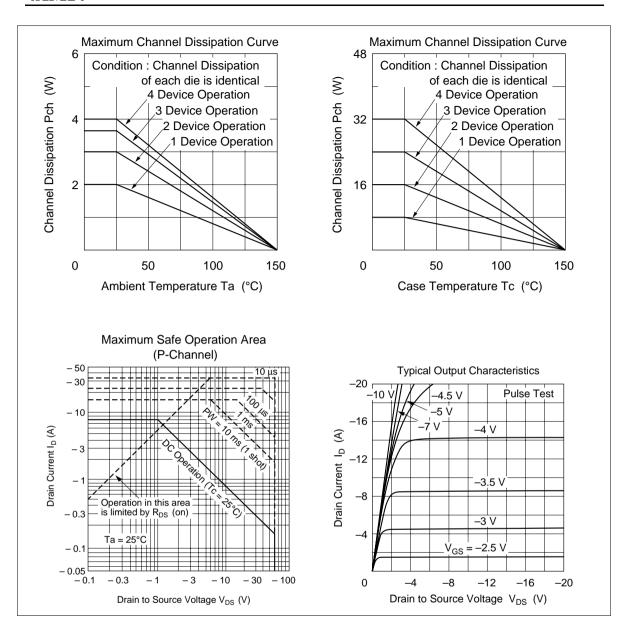
Electrical Characteristics (Ta = 25°C) (1 Unit)

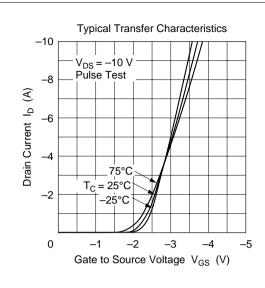
	Symbol	N channel		P channel					
Item		Min	Тур	Max	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60		_	-60	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20		_	±20	_	_	V	$I_{G} = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I _{GSS}	_		±10	_	_	±10	μΑ	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_		250	_	_	-250	μΑ	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0		2.0	-1.0	_	-2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source	R _{DS(on)}	_	0.13	0.17	_	0.15	0.2	Ω	$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
on state resistance		_	0.18	0.24	_	0.20	0.27	Ω	$I_D = 4 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	y _{fs}	3.5	5.5	_	3.5	6.0	_	S	$I_D = 4 \text{ A}, V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	Ciss	_	400	_	_	900	_	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$
Output capacitance	Coss	_	220	_	_	460	_	pF	f = 1 MHz
Reverse transfer capacitance	Crss	_	60	_	_	130	_	pF	_
Turn-on delay time	t _{d(on)}	_	5	_	_	8	_	ns	$I_D = 4 A, V_{GS} = 10 V,$
Rise time	t _r	_	45	_	_	50	_	ns	$R_L = 7.5 \Omega$
Turn-off delay time	$t_{d(off)}$	_	150	_	_	180	_	ns	_
Fall time	t _f	_	85	_	_	95	_	ns	=
Body to drain diode forward voltage	V_{DF}	_	1.2	_	_	-1.2	_	V	$I_F = 8 A, V_{GS} = 0$
Body to drain diode reverse recovery time	t _{rr}	_	120	_	_	185	_	ns	$I_F = 8 \text{ A}, V_{GS} = 0,$ $dIF/dt = 50 \text{ A/}\mu\text{s}$
Note: 1. Pulse Test									

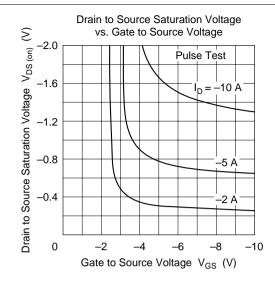
Note: 1. Pulse Test

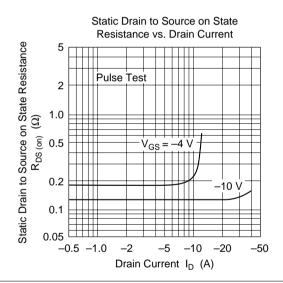
Polarity of test conditions for P channel device is reversed.

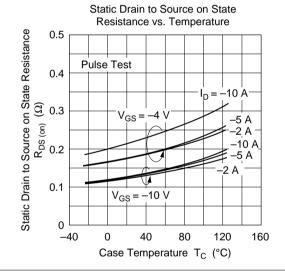
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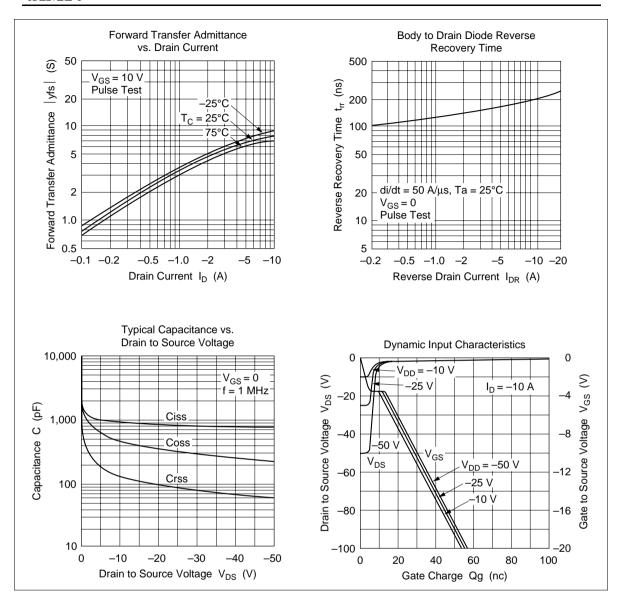


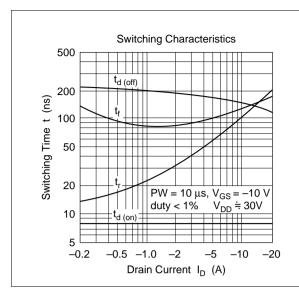


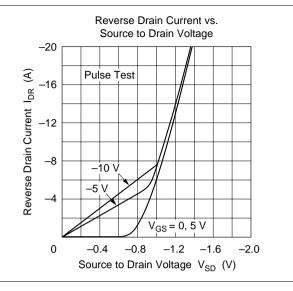


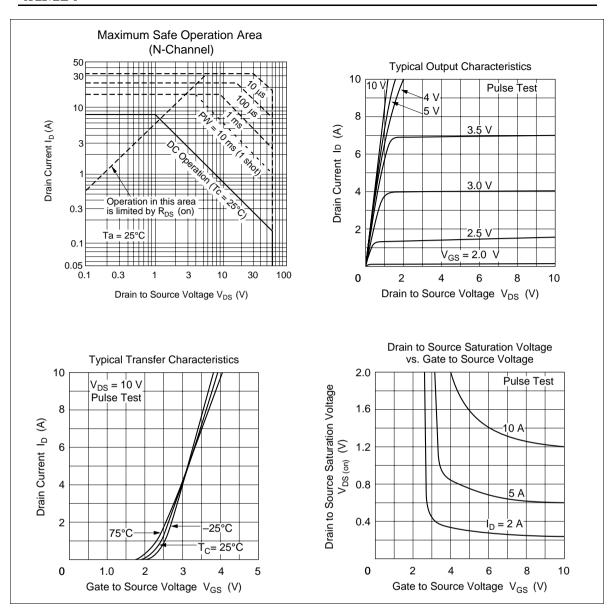


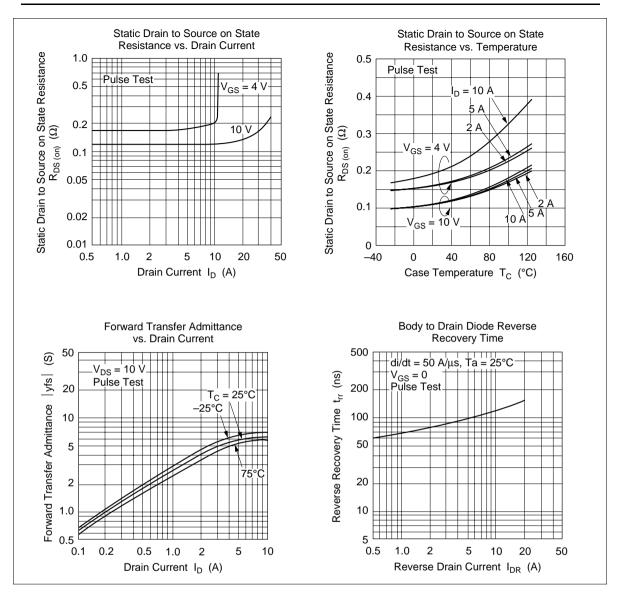


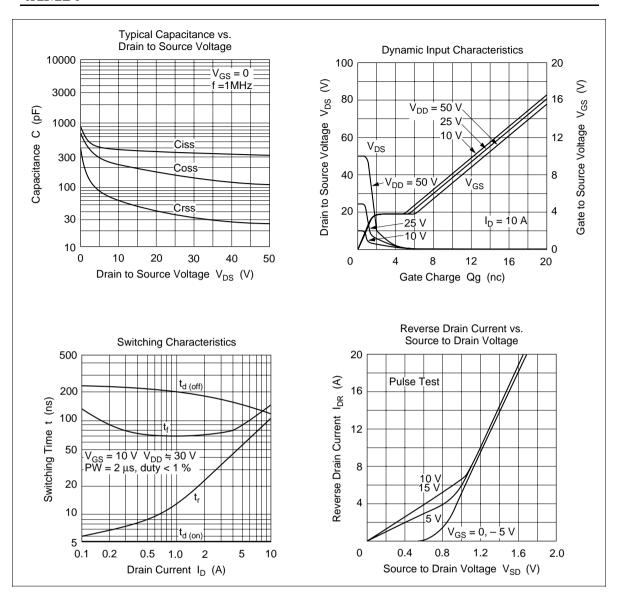




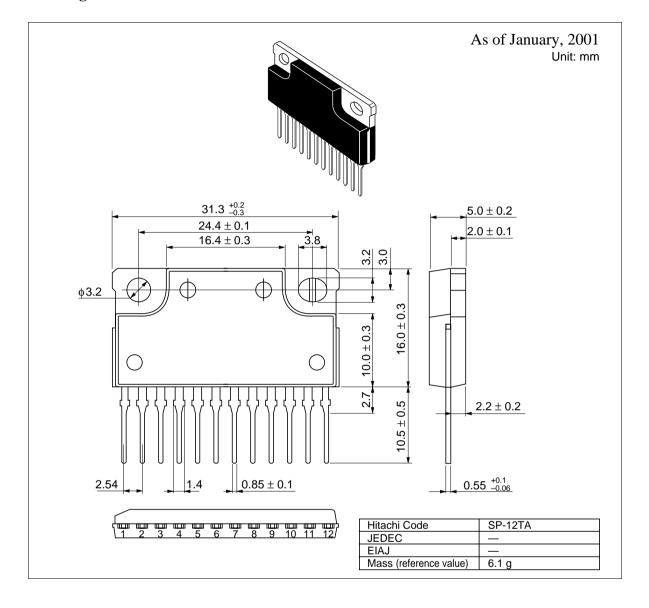








Package Dimensions



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