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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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Silicon N-Channel/P-Channel Power MOS FET Array



ADE-208-1211 (Z) 1st. Edition Mar. 2001

Application

High speed power switching

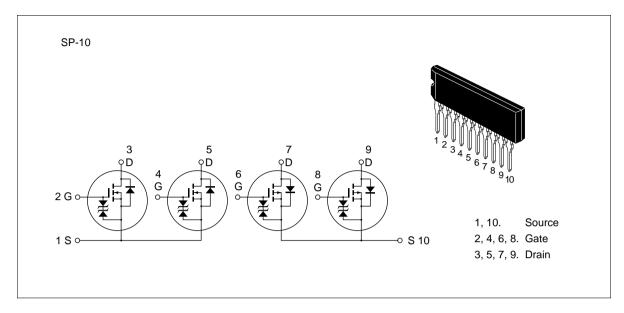
Features

• Low on-resistance

N-channel: $R_{DS(on)} \le 0.4$, $V_{GS}=10$ V, $I_D=1.5$ A P-channel: $R_{DS(on)} \le 0.45$, $V_{GS}=-10$ V, $I_D=-1.5$ A

- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

		Rating		
Item	Symbol	Nch	Pch	Unit
Drain to source voltage	$V_{\scriptscriptstyle DSS}$	60	-60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I _D	3	-3	A
Drain peak current	I _{D(pulse)} *1	12	-12	A
Body to drain diode reverse drain current	I _{DR}	3	-3	A
Channel dissipation	Pch (Tc = 25°C)*2	28		W
Channel dissipation	Pch*2	4		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to -	+150	°C

Notes: 1. PW \leq 10 μ s, duty cycle \leq 1%

2. 4 Devices operation

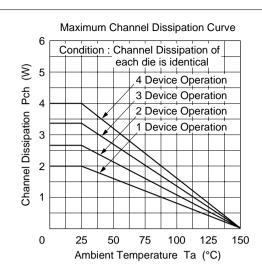
Electrical Characteristics (Ta = 25°C) (1 Unit)

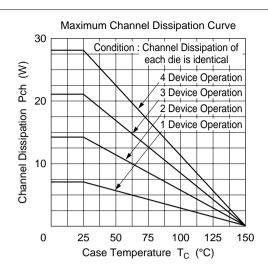
		N cha	annel		P channel				
Item	Symbol	Min	Тур	Max	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	_	_	-60	_	_	V	$I_{D} = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	_	_	±20	_	_	V	$I_{G} = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I _{GSS}	_	_	±10	_	_	±10	μΑ	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	250	_		-250	μΑ	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	_	2.0	-1.0		-2.0	V	$I_{D} = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{ ext{DS(on)}}$	_	0.25	0.35	_	0.28	0.4	Ω	$I_D = 1.5 \text{ A},$ $V_{GS} = 10 \text{ V}^{*1}$
		_	0.35	0.5	_	0.4	0.55	Ω	$I_D = 1.5 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	y _{fs}	1.5	2.5	_	1.5	2.5	_	S	$I_D = 1.5 \text{ A},$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	Ciss	_	240	_	_	400	_	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$
Output capacitance	Coss	_	115	_	_	240	_	pF	f = 1 MHz
Reverse transfer capacitance	Crss	_	35	_	_	70	_	pF	_
Turn-on delay time	t _{d(on)}	_	4	_	_	5	_	ns	$I_D = 1.5 \text{ A}, V_{GS} = 10 \text{ V},$
Rise time	t _r	_	20	_	_	25	_	ns	$R_L = 20 \Omega$
Turn-off delay time	t _{d(off)}	_	80	_	_	180	_	ns	_
Fall time	t _f	_	40	_	_	80	_	ns	_
Body to drain diode forward voltage	V_{DF}	_	1.2	_	_	-1.1	_	V	$I_F = 3 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t _{rr}	_	75	_	_	140	_	ns	$I_F = 3 \text{ A}, V_{GS} = 0,$ $dIF/dt = 50 \text{ A/}\mu\text{s}$

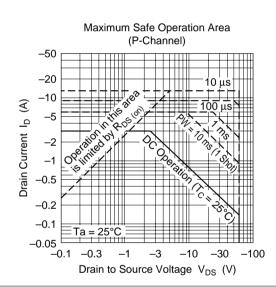
Note: 1. Pulse Test

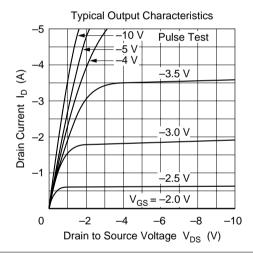
Polarity of test conditions for P channel device is reversed.

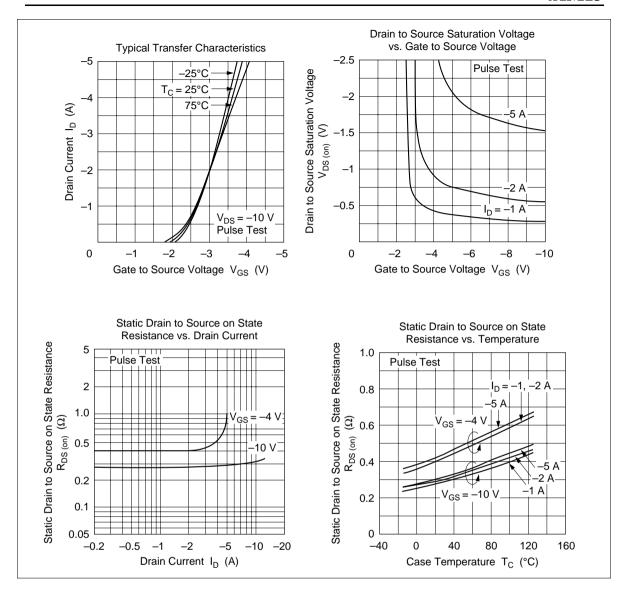
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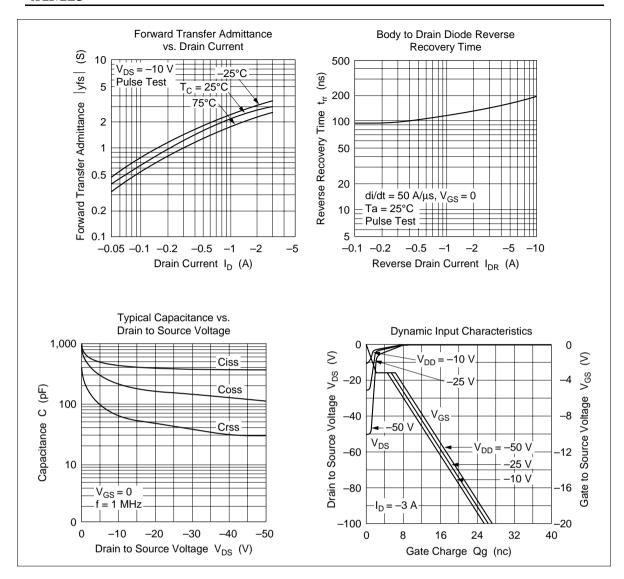


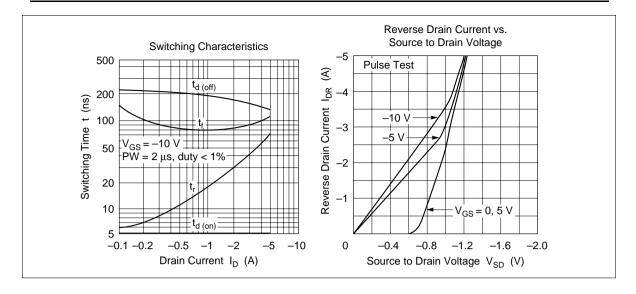


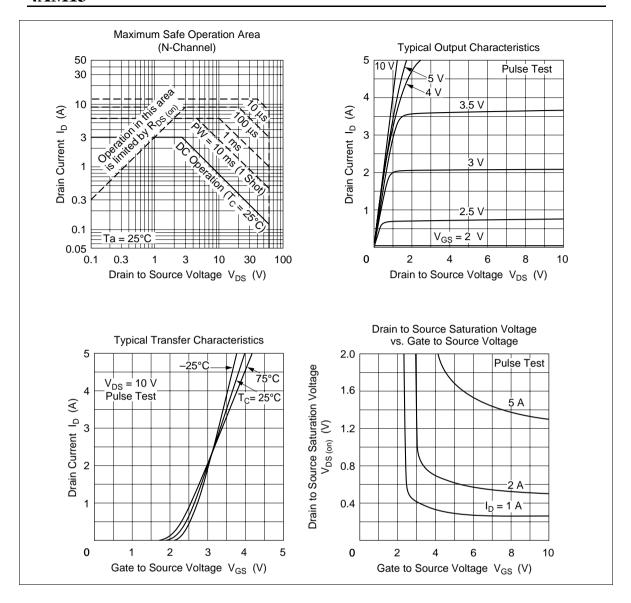


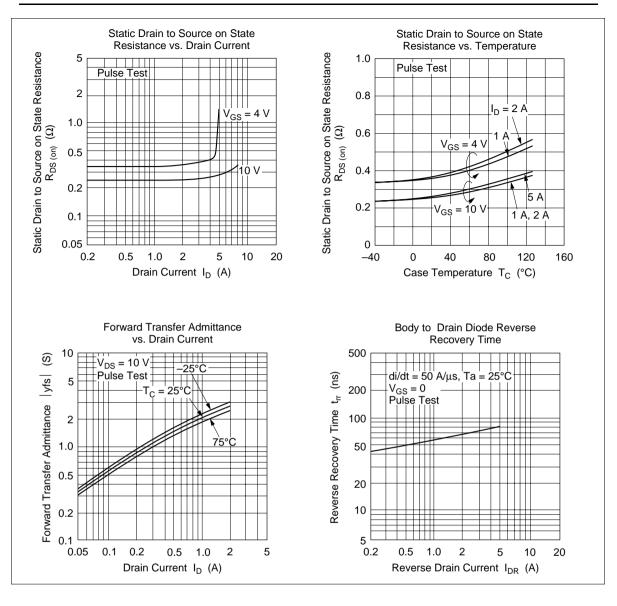


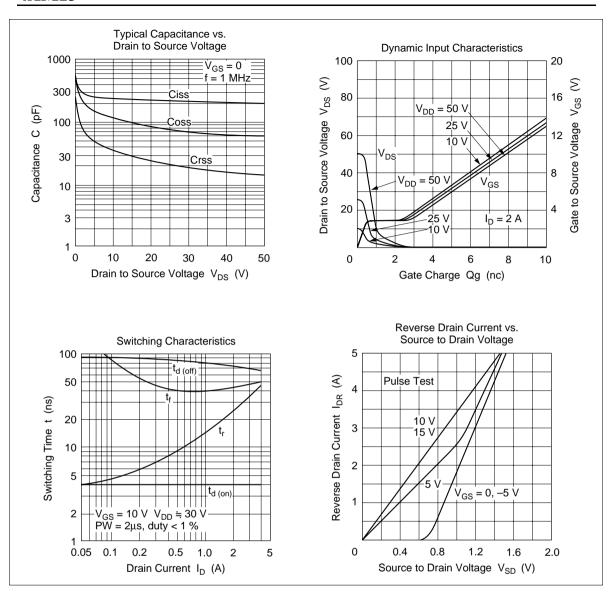




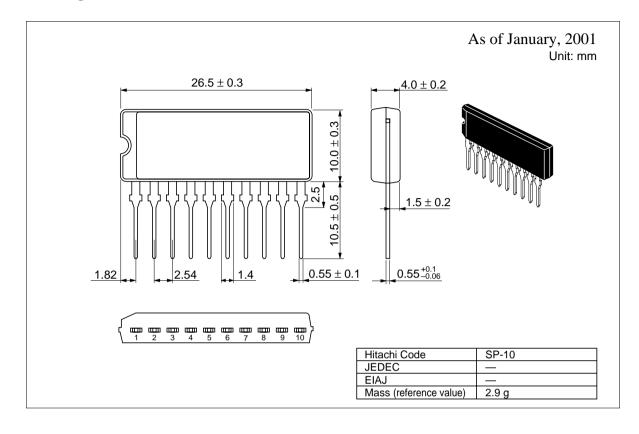








Package Dimensions



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