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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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4AK27

Silicon N Channel MOS FET
High Speed Power Switching

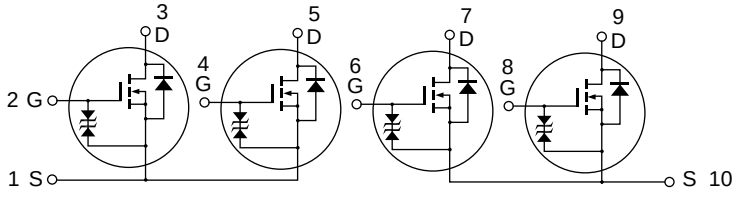
ADE-208-728 (Z)
1st. Edition
Mar. 2001

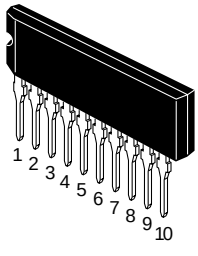
Features

- Low on-resistance
  $R_{DS(on)} \leq 0.15\Omega$, V_{GS} = 10V, I_D = 3.0A
- 4V gate drive devices.
- High density mounting

Outline

SP-10





1, 10. Source
2, 4, 6, 8. Gate
3, 5, 7, 9. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$ Note1	20	A
Body-drain diode reverse drain current	I_{DR}	5	A
Avalanche current	I_{AP}	5	A
Avalanche energy1	E_{AR}	2.1	mJ
Channel dissipation	Pch(Tc=25˚C) Note2	28	W
Channel dissipation	Pch Note2	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

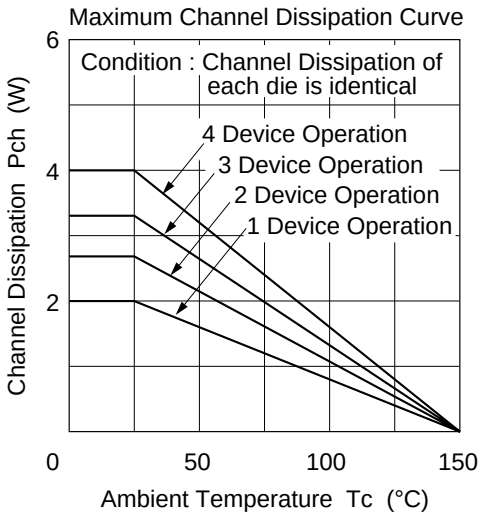
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. 4 devices poeration
3. Value at Tch=25˚C, Rg ≥ 50Ω

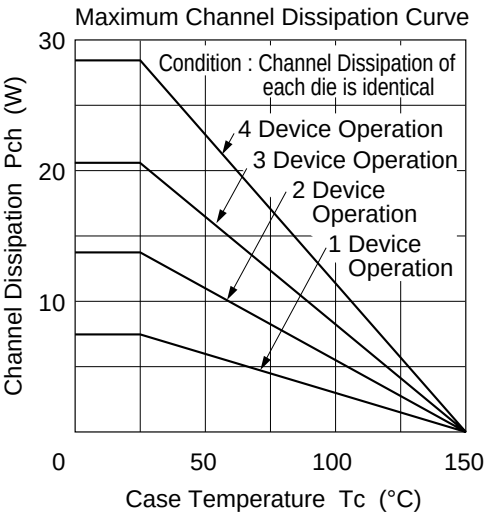
Electrical Characteristics (Ta = 25°C)

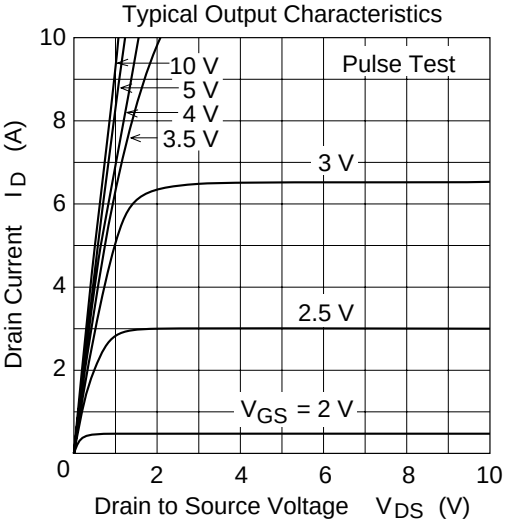
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 3A, V_{GS} = 10V [Note4]
Static drain to source on state resistance	$R_{DS(on)}$	—	0.15	0.2	Ω	I_D = 3A, V_{GS} = 4V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.5	—	S	I_D = 3A, V_{DS} = 10V [Note4]
Input capacitance	Ciss	—	390	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10V, I_D = 3A
Rise time	t_r	—	42	—	ns	R_L = 10Ω
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	
Fall time	t_f	—	55	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = 5A, V_{GS} = 0 diF/ dt =50A/µs

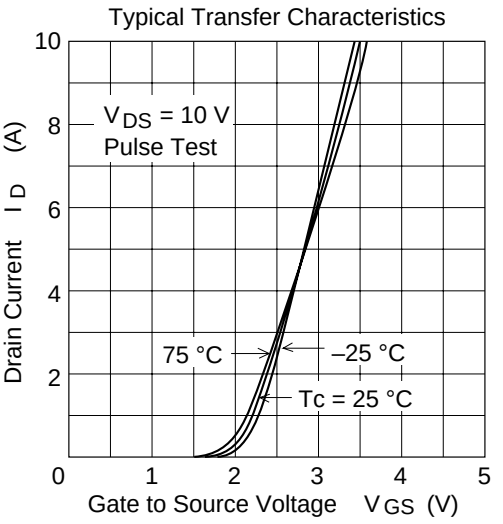
Note: 4. Pulse test

Main Characteristics

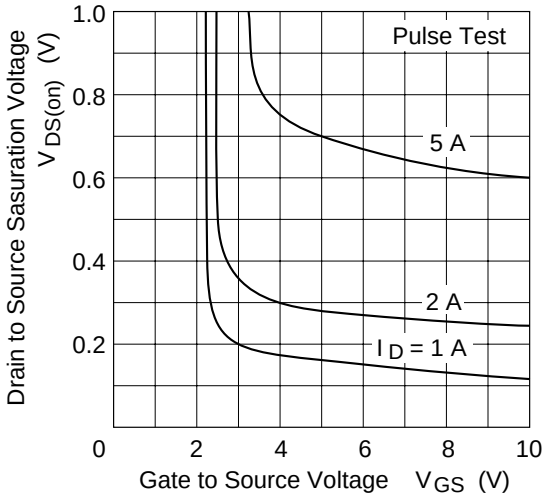




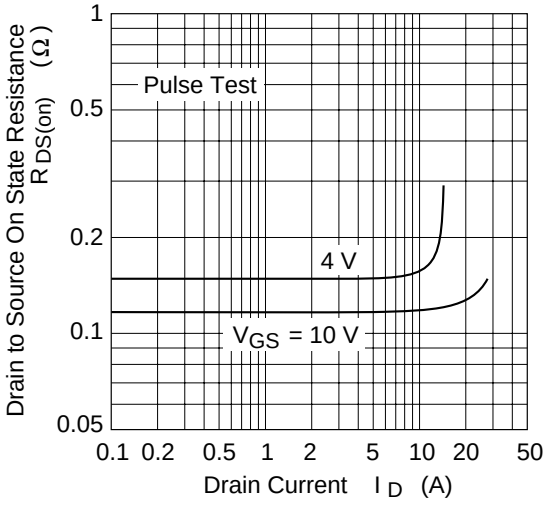




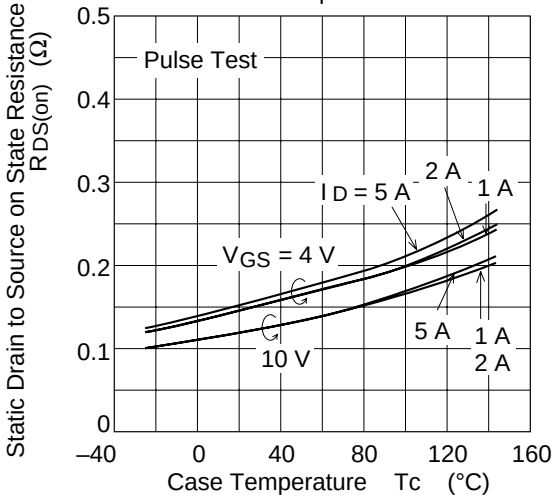
Drain to Source Saturation Voltage vs. Gate to Source Voltage



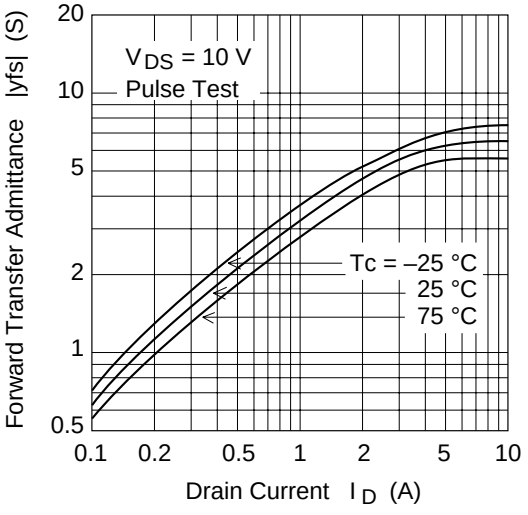
Static Drain to Source State Resistance vs. Drain Current



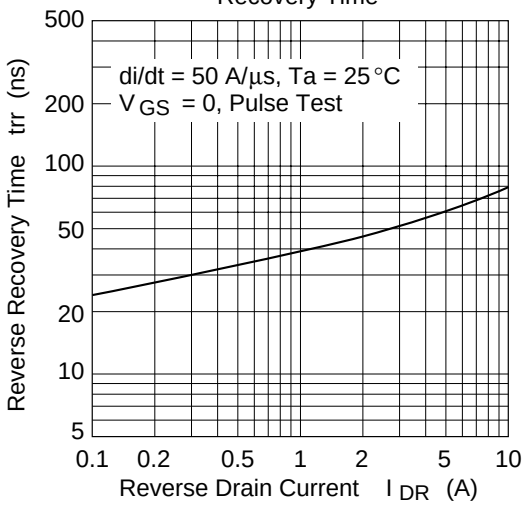
Static Drain to Source on State Resistance vs. Temperature



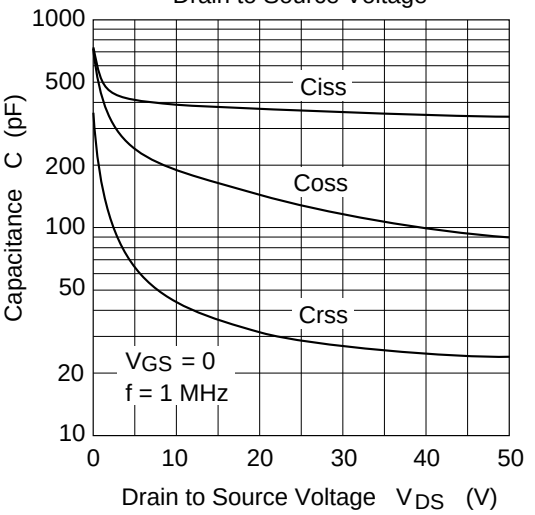
Forward Transfer Admittance vs. Drain Current



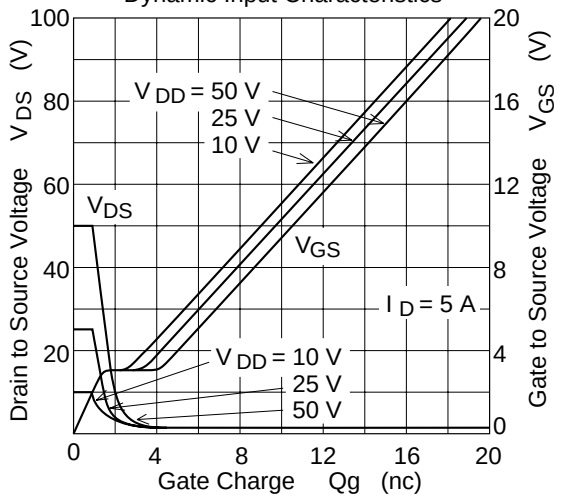
Body to Drain Diode Reverse Recovery Time



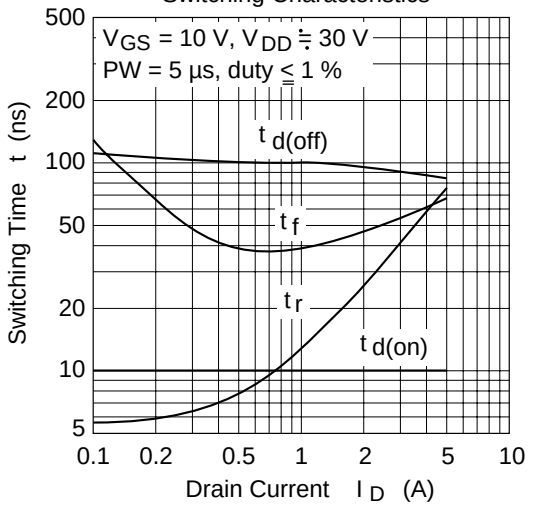
Typical Capacitance vs. Drain to Source Voltage



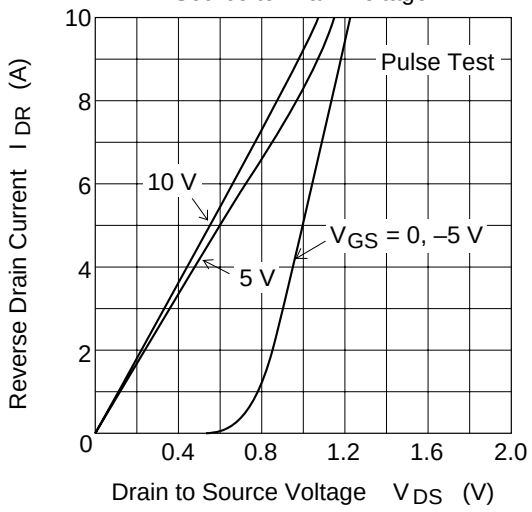
Dynamic Input Characteristics



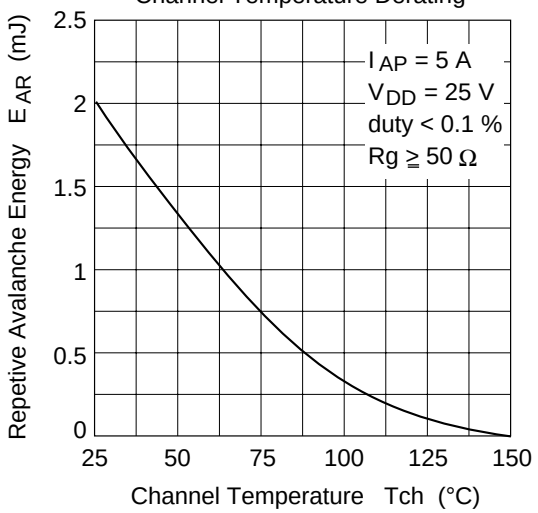
Switching Characteristics



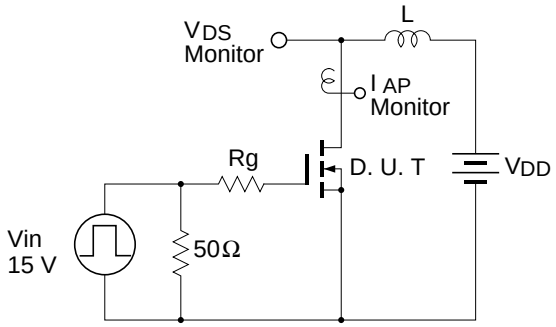
Reverse Drain Current vs.
Source to Drain Voltage



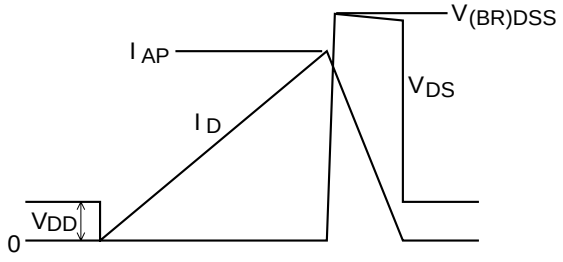
Maximun Avalanche Energy vs.
Channel Temperature Derating



Avalanche Test Circuit and Waveform



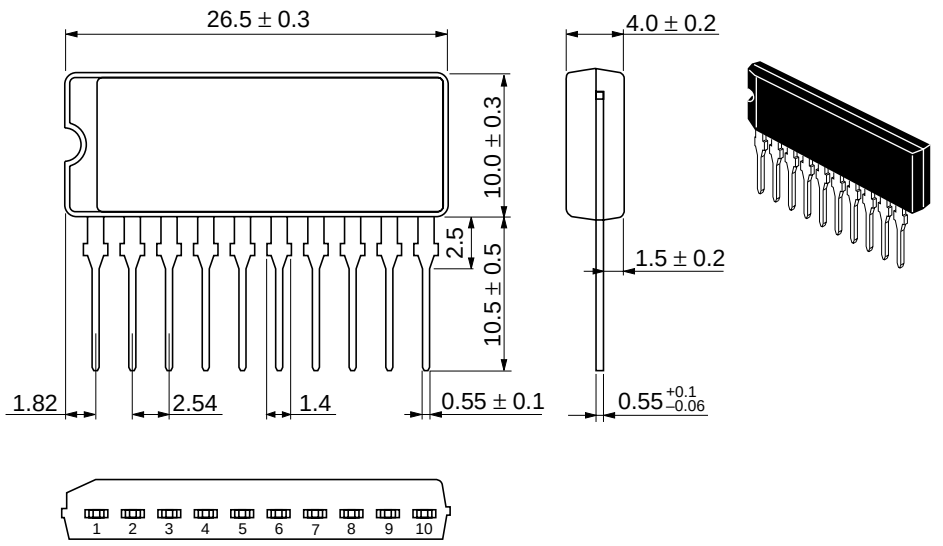
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SP-10
JEDEC	—
EIAJ	—
Mass (reference value)	2.9 g

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