To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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4AK26

Silicon N-Channel Power MOS FET Array

ADE-208-1208 (Z)
1st. Edition
Mar. 2001

Application

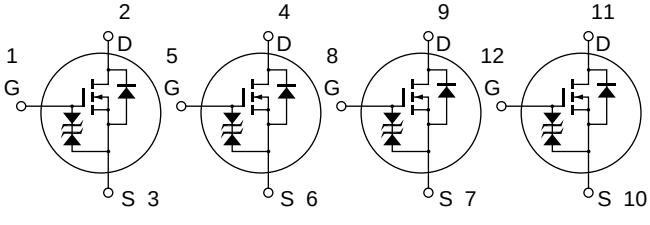
High speed power switching

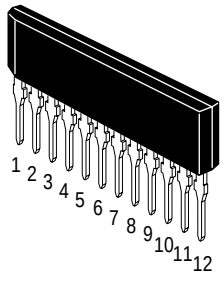
Features

- Low on-resistance
  $R_{DS(on)} \leq 0.06$, V_{GS} = 10 V, I_D = 5 A
  $R_{DS(on)} \leq 0.075$, V_{GS} = 4 V, I_D = 5 A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for motor driver and solenoid driver and lamp driver

Outline

SP-12





1, 5, 8, 12. Gate
2, 4, 9, 11. Drain
3, 6, 7, 10. Source

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*[1]	32	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch (Tc = 25°C)*[2]	28	W
Channel dissipation	Pch*[2]	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

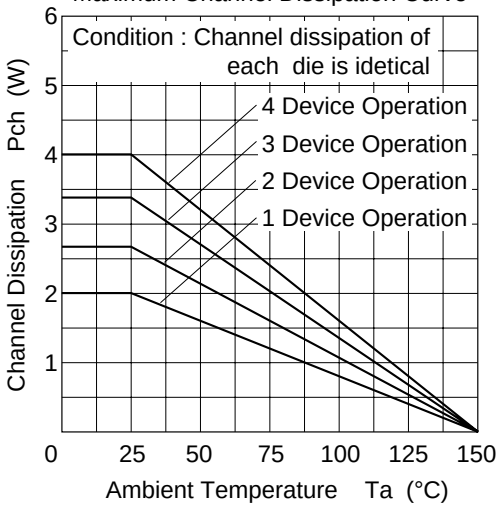
Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 4 Devices operation

Electrical Characteristics (Ta = 25°C)

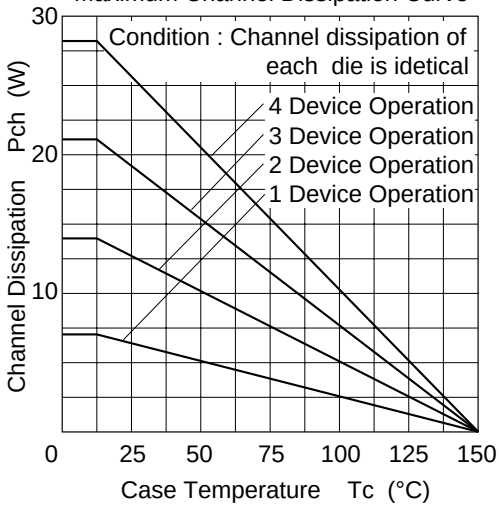
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.045	0.06	Ω	I_D = 5 A V_{GS} = 10 V*[1]
		—	0.056	0.075	Ω	I_D = 5 A V_{GS} = 4 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	10	12	—	S	I_D = 5 A V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	720	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	220	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 10 A
Rise time	t_r	—	95	—	ns	V_{GS} = 10 V
Turn-off delay time	$t_{d(off)}$	—	300	—	ns	R_L = 3 Ω
Fall time	t_f	—	170	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.05	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	110	—	µs	I_F = 10 A, V_{GS} = 0, dIF/dt = 50 A/µs

Note: 1. Pulse Test

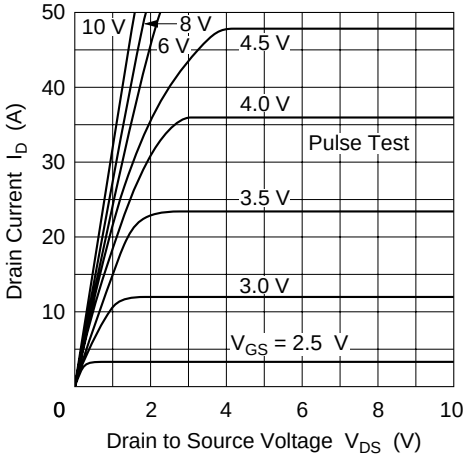
Maximum Channel Dissipation Curve



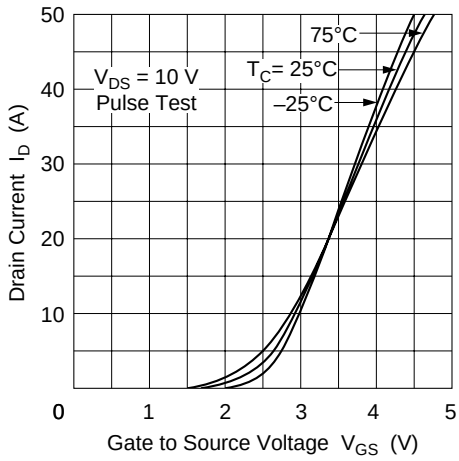
Maximum Channel Dissipation Curve



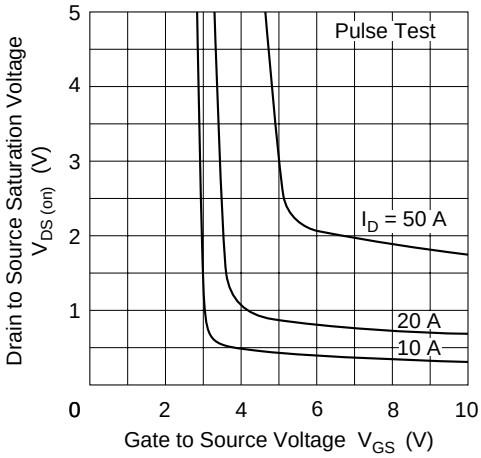
Typical Output Characteristics



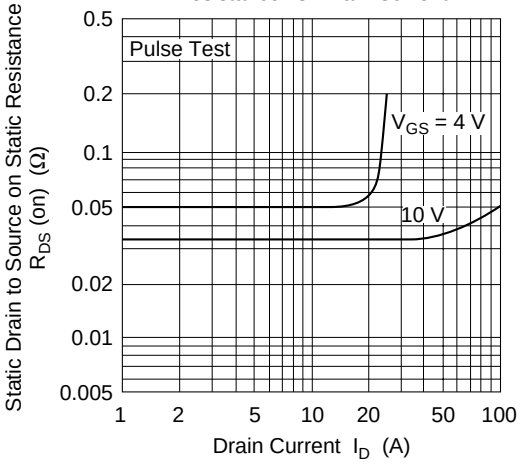
Typical Transfer Characteristics



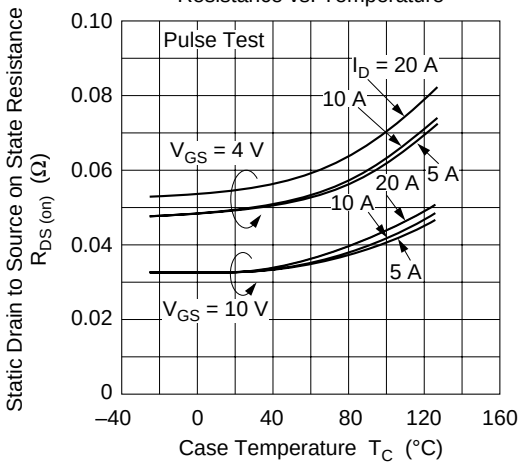
Drain to Source Saturation Voltage vs. Gate to Source Voltage



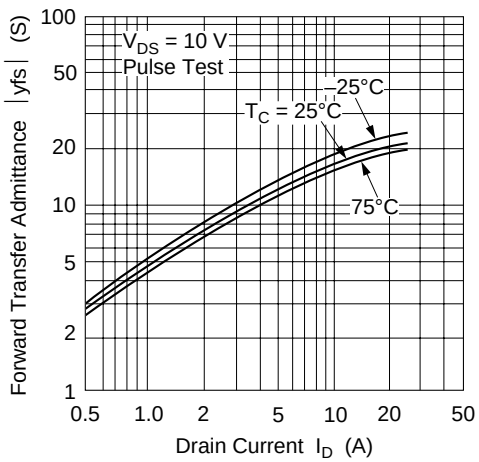
Static Drain to Source on State Resistance vs. Drain Current



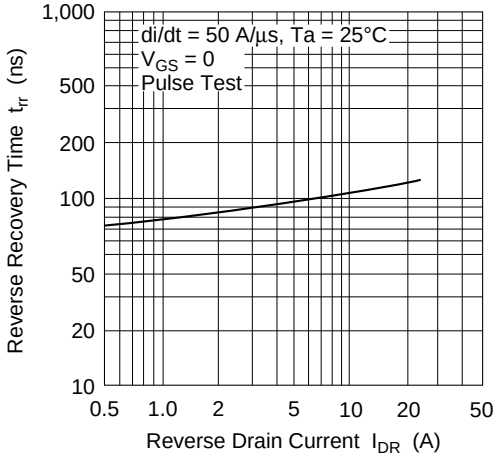
Static Drain to Source on State Resistance vs. Temperature



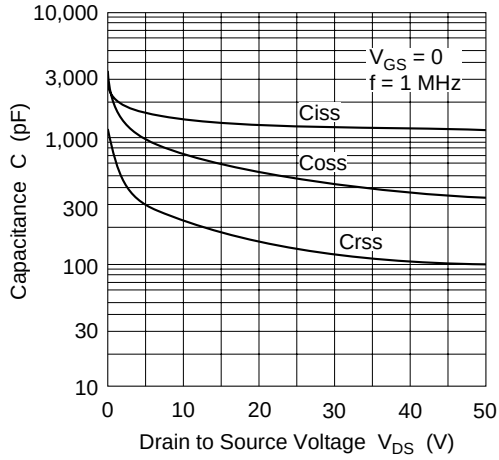
Forward Transfer Admittance vs. Drain Current



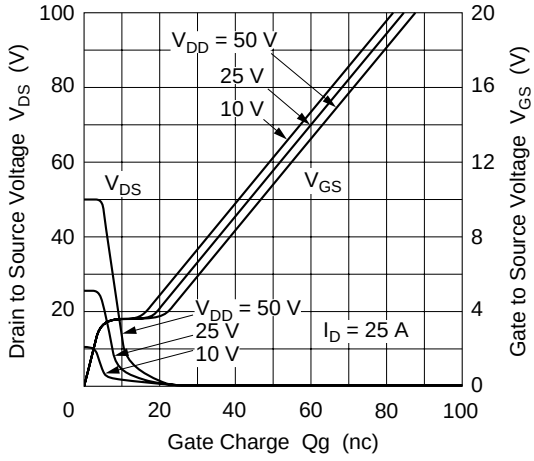
Body to Diode Reverse Recovery Time



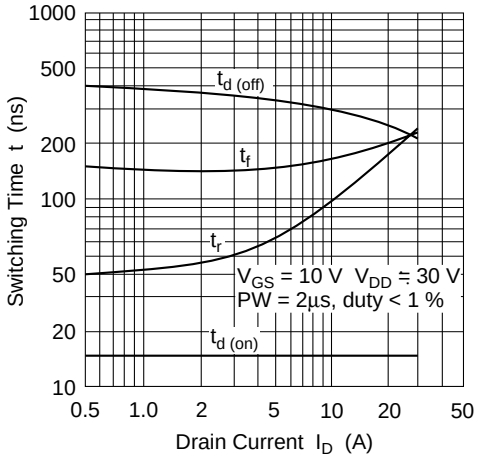
Typical Capacitance vs. Drain to Source Voltage

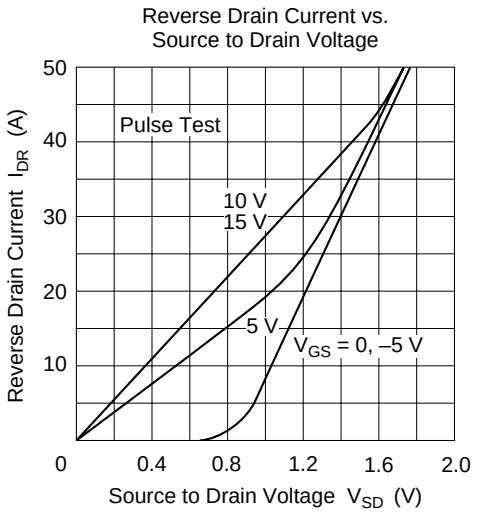


Dynamic Input Characteristics



Switching Characteristics

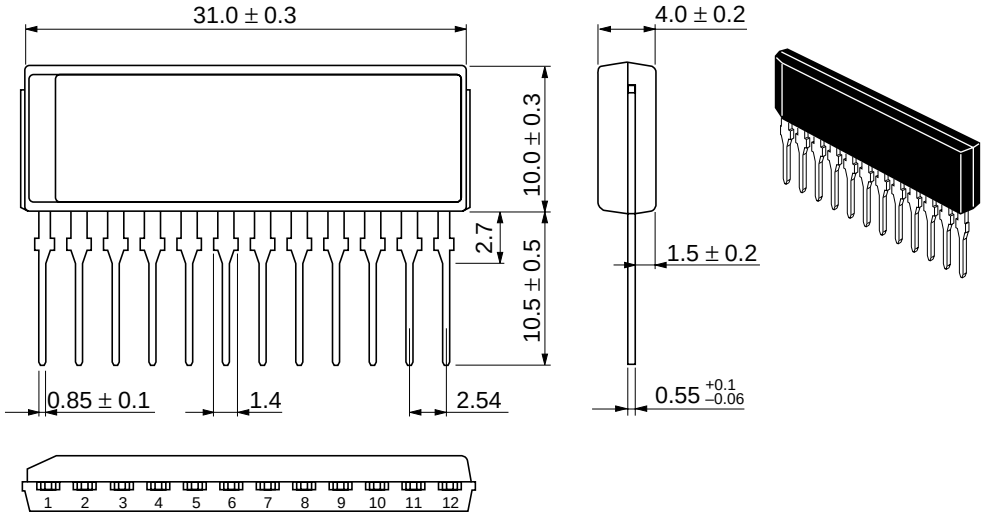



Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SP-12
JEDEC	—
EIAJ	—
Mass (reference value)	3.6 g

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