Product Brief
October 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

497AE and 1215E Boundary-Scan Master 2

Features

- The BSM2 is available in 2 versions:
  - — The 497AE is available in a 28-pin SOJ package.
  - — The 1215E device is available in a 48-pin TQFP package.
- The 497AE and 1215E differ in the following capabilities:
  - — The 497AE has an 8-bit data bus and no user I/O signals.
  - — The 1215E has a 16-bit data bus and 3 user I/O signals.
- Selectable between two operational modes:
  - — 497AA compatiblity mode
  - — Advanced operational mode (497AE)
- 3.3 V power supply, but fully 5 V (TTL) tolerant for all inputs and outputs
- Dedicated 8 kbits test data in (TDI) and test data out (TDO) buffers; FIFO or fully addressable
- Simple and flexible host interface options:
  - — 497AE, synchronous or asynchronous 8-bit data bus
  - — 1215E, 16-bit asynchronous data bus for maximum throughput
- Self-timing interface to a microprocessor/microcontroller
- Automatic test mode select (TMS) sequence generation
- Programmable test clock (TCK) generator with gated TCK mode
- Provides test reset (TRST*) optional TAP signal
- External pin control to 3-state test access port (TAP) signals (1215E)
- Conflict-free automatic test pattern generator (ATPG)
- 32-bit signature analysis register (SAR) with response masking for repeatable signatures
- TCK output frequency of 65 MHz
- Maskable processor interrupts; no lockup condition
- Built-in self-test for >95% fault coverage
- Supports protocols for multidrop backplane test configurations, such as *TI*'s[1] addressable scan port protocol
- Provides retiming (pipeline) delays of up to 13 TCK cycles to correct skewing
- One general-purpose input, two general-purpose outputs. Outputs can be programmed for use as DMA control signals (1215E device only)

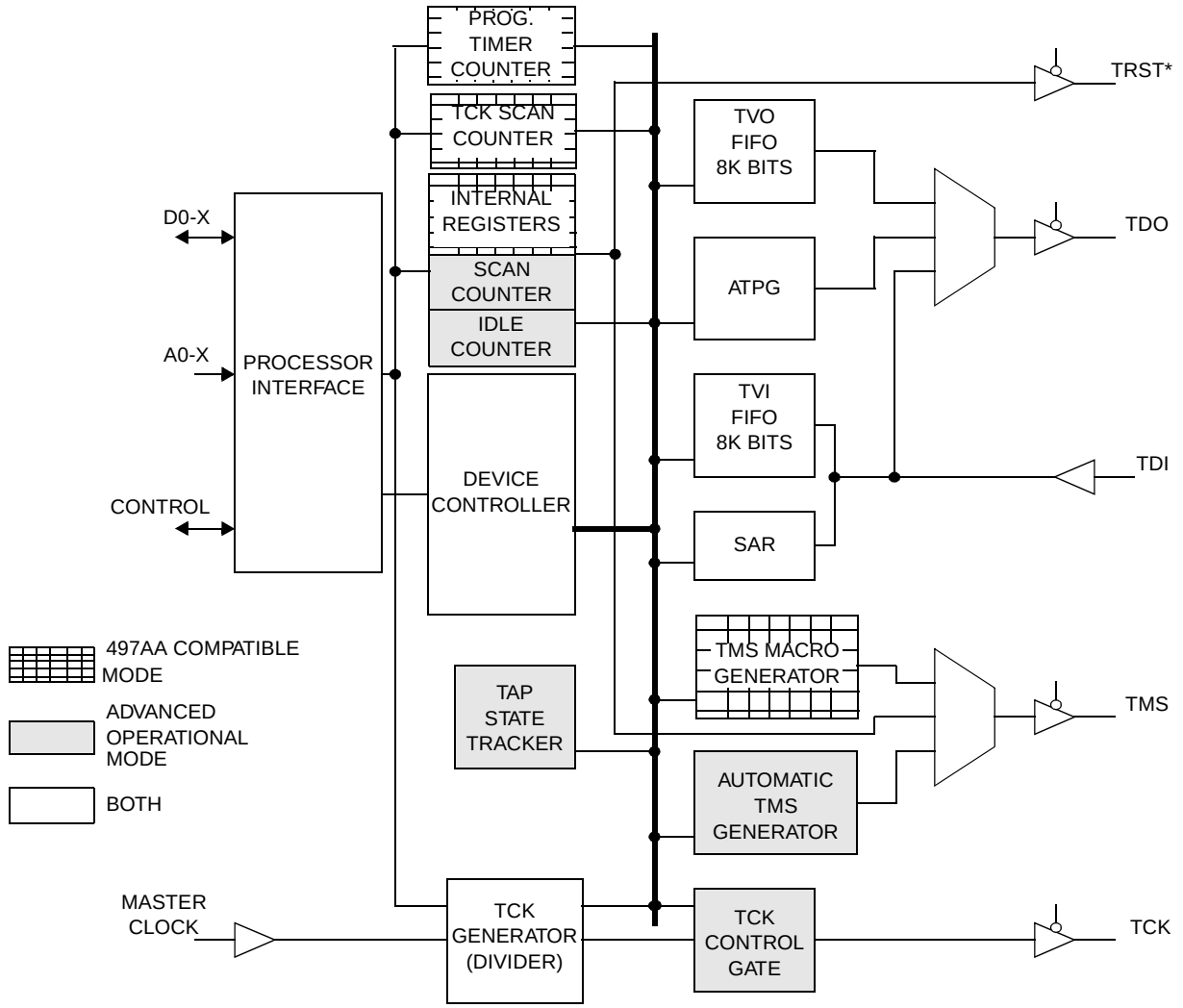
Description

The Lucent Technologies Microelectronics Group 497AE/1215E Boundary-Scan Master 2 (BSM2) communicates with a generic processor in parallel and controls the test and diagnosis (T&D) of a unit under test (UUT), which could be a device, board, or system, based on the ANSI/*IEEE*[2] standard 1149.1-1990 TAP and Boundary-Scan (B-S) Architecture. It serializes test vectors, delivers them to the UUT using the standard protocol, and stores the UUT response as raw data or as a signature. An ATPG generates four common test sequences for interconnect test, cluster test, etc. The device also solves the potential problems of bus conflict and nonrepeatable board-level signatures associated with the B/S architecture. Finally, the BSM2 provides support for edge-connector/backplane test and system test and diagnosis.

The BSM2 comes in two package sizes. The 497AE is a 3.3 V, 28-pin SOJ package that provides both software and hardware backward compatibility to the 497AA BSM. The 1215E is a 3.3 V, 48-pin TQFP package with a 16-bit data bus and direct register access.

* Asterisk on any pin name indicates active-low.
1. *TI* is a registered trademark of Texas Instruments Inc.
2. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Architecture



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