Product Brief
July 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

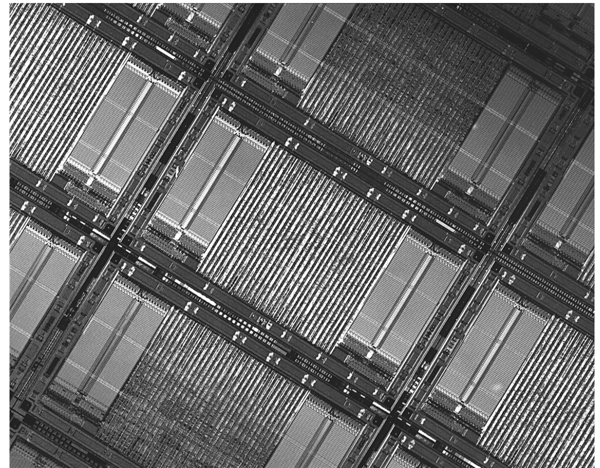
Lucent Boundary-Scan Master 497AA

Introduction

The Lucent Boundary-Scan Master (BSM), the 497AA, communicates with a generic processor in parallel and controls the test/diagnosis (T&D) of a unit under test (UUT), which could be a device, board, or system, based on the ANSI/*IEEE*[1] Std. 1149.1-1990 Test Access Port (TAP) and Boundary-Scan (B-S) Architecture. The Lucent BSM serializes test vectors, delivers them to the UUT using the standard protocol, and stores the UUT response as raw data or as a signature. An automatic test pattern generator (ATPG) generates four common test sequences for interconnect test, cluster test, etc. The device also solves the potential problems of bus conflict and nonrepeatable board-level signatures associated with the B-S architecture. Finally, the BSM provides support for edge-connector/backplane test and system test and diagnosis.

Features

- Small package size: 28-pin SOJ (300 mils x 710 mils)
- Parallel-to-serial protocol conversion
- Generic processor interface with programmable 1-bit or 8-bit data bus
- Dedicated 8K TDI and TDO buffers
- Conflict-free automatic test pattern generation
- 32-bit signature analysis register (SAR) with response masking for repeatable signatures
- Two independent programmable TMS macro generators
- Supports two scan chains in star configuration
- Supports *IEEE* 1149.1 sample operation through external trigger input, SP* (sample on event)
- Programmable counter/timer
- Maskable processor interrupts
- Reconfigurable system B-S ring for simplified backplane test and high T&D throughput
- Supports broadcast by processor to multiple BSMs



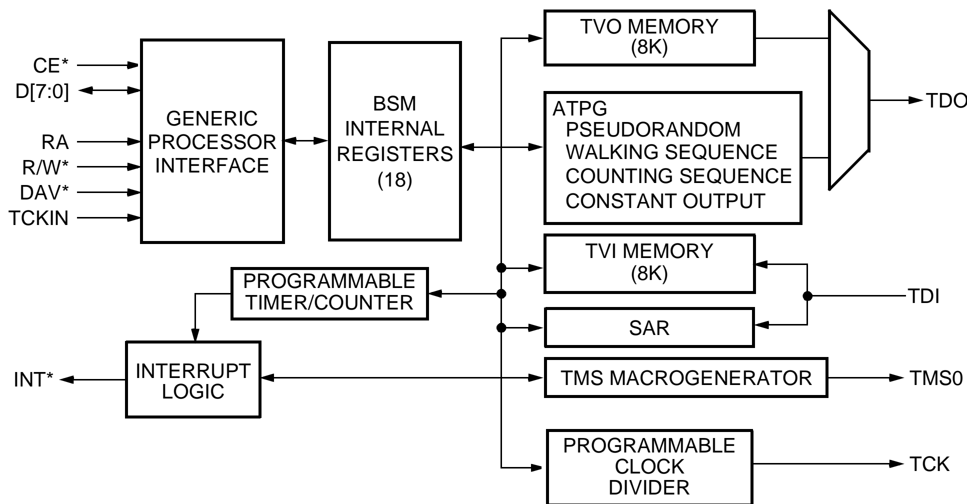
Description

The Boundary-Scan Master (BSM) minimizes the housekeeping required by a test and diagnosis host processor, and maximizes the test/diagnosis throughput. Figure 1 shows the architecture of the BSM. On the left, it has a generic 8-bit microprocessor interface with an address, data, and control bus. On the right, it communicates with the ANSI/*IEEE* Std. 1149.1-1990 TAP signals. Consequently, it can be thought of as a protocol converter. The main subsystems of this device are the generic processor interface (GPI), BSM internal registers (BIR), test data output (TDO) generator, test data input (TDI) receiver, test mode select (TMS) generator, test clock (TCK) generator, and system-level boundary-scan configuration logic. The BSM also provides support for the sampling feature of the Standard's SAMPLE/PRELOAD instruction. Other features included are interrupt control and a programmable timer/counter. An overview of these subsystems follows.

1. *IEEE* is a registered trademark of the Institute of Electrical and Electronics Engineers, Inc.

Note: A terminal * on an input lead name indicates that that input is active-low. This follows the convention used in the 1149.1 Standard.

Description (continued)



Note: A terminal * on an input lead name indicates that that input is active-low. This follows the convention used in the 1149.1 Standard.

Figure 1. The Architecture of the Boundary-Scan Master

Generic Processor Interface

The GPI communicates with a host processor that can be any generic processor or an ATE. Through the GPI, the processor can control the behavior of the BSM, monitor its status, and transfer/retrieve test vectors to, and test response from, the BSM.

To minimize the number of signals required to interface with the BSM, a bit-serial mode is supported. To achieve high throughput in a system with multiple BSMs, a broadcast mode is also supported.

Internal Registers

The BSM has 18 internal registers. One register is accessed directly, and the other 17 are accessed indirectly. There are 6 byte-wide control/status registers. The remaining 12 are data registers and are 2 bytes to 4 bytes wide.

The operation of the BSM is controlled by the processor via these registers. The mode of operation of the BSM, selection of the source of test stimuli, destination of the test response, etc., are all determined by read and write operations on these registers.

TDO Generator

The TDO generator is one of the most powerful subsystems in the BSM. It offers the user a choice to apply deterministic test vectors from its 8K TVO memory or to use the hardware ATPG which can be programmed to generate a serialized walking sequence, counting sequence, pseudorandom sequence, or constant output. The walking and counting sequence are useful in interconnect test while the pseudorandom sequence can be used for cluster testing. The constant output simplifies the scanning in of EXTEST and BYPASS instructions and can have other applications at system test.

Description (continued)

TDO Generator (continued)

The hardware ATPG has built-in intelligence that permits it to generate algorithmic and pseudorandom sequences and modify them so that no bus conflicts occur. This is achieved by a unit called the scan-sequence modifier (SSM) (Figure 2). The SSM helps in ensuring that only meaningful test data is compressed in the signature analysis register (SAR) so that repeatable board-level signatures are obtained. The SSM uses a scan path structure map stored in the TVO/TVI memories to identify every bit being shifted in or out of the B-S register as belonging to one of the following classes: a cell at which a test stimuli must be applied, a cell that will contain valid test response, a cell that must be held to a constant 1, and a cell that must be held to a constant 0. It can, therefore, modify the output stream to ensure safe operation as well as to identify data on the input stream that should be compressed by the SAR. This feature results in high test and diagnostic throughput since minimal intervention by the host processor is required.

TDI Receiver

The response received from the UUT can be stored in an 8K buffer memory for uploading by the processor. This is useful if the full response is required for diagnosis. The response can also be compressed to a 32-bit signature. This provides rapid pass/fail information.

TMS Generator

The BSM uses a novel technique for generating TMS. A 16-bit circular shift register is used to generate a sequence on the TMS output. This length is sufficient to generate arbitrary walk sequences through the TAP controller. To control the precise duration in the **Shift-IR/DR** controller state, a specific bit (bit 8) of the shift register is associated with this state. The register must be initialized correctly so that this mapping occurs. A scan duration counter (SDC) is initialized with the duration that the TAP controller should stay in the **Shift-IR/DR** controller state. This corresponds to the length of the scan path that is being accessed. The TAP controller starts in a stable controller state (either **Test-Logic-Reset**, **Run-Test/Idle**, or **Pause-DR/IR**). When the TMS generator is activated, it starts shifting the value in its register to the TMS output. At the eighth bit (corresponding to the TAP entering the **Shift-IR/DR** controller state), the shift register freezes, holding the TAP in the **Shift-IR/DR** controller state, and the SDC begins to count down. At this point, the BSM begins to shift out serialized test data from the TDO generator and to store test response via the TDI receiver. When the SDC counts down to zero, the TMS generator resumes shifting the remaining 8 bits, taking the UUT device TAP controllers from the **Shift-IR/DR** controller state to a stable controller state.

The TMS generator also directly supports the use of the SAMPLE instruction in a logic analyzer-like mode.

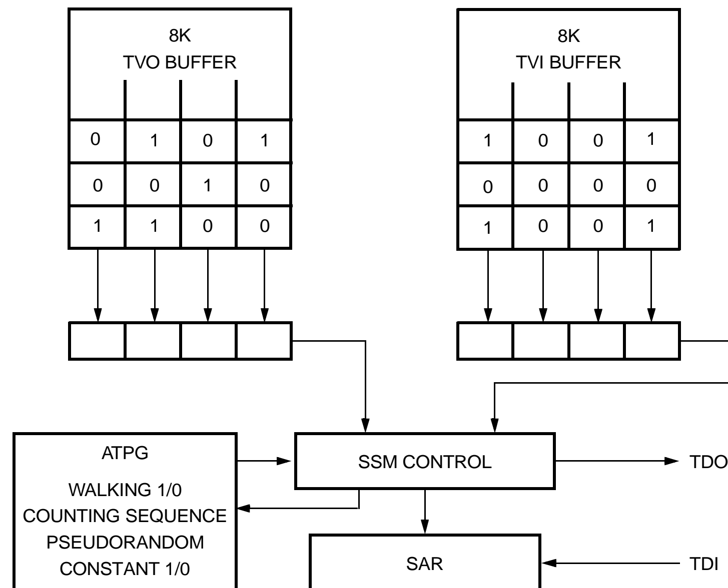


Figure 2. Scan-Sequence Modifier

Description (continued)

TCK Generator

This module generates the clock output TCK by dividing the input clock TCKIN by a programmable value ranging from 1 to 128, in power-of-two increments. This is required because the test clock may have to be slowed down to match the speed of the slowest device on the scan path.

System Scan Ring Configuration

The BSM provides support for simplifying backplane/ edge-connector test, implementing the uniring/multiring concept. It has two pins, TDIN and TDOUT, that are daisy-chained between BSMs on different boards, forming a system-level scan ring. During board testing, each BSM communicates with the T&D processor and independently tests its own local board (multiring configuration). For testing the backplane, the individual scan paths on different boards can be connected to form a system scan path (uniring configuration). A specific BSM can be designated as a system scan ring master. It will control the backplane test, which now can be performed as an ordinary interconnect test. Support is also provided for bypassing a board.

BSM Quality

Since the BSM is designed to enhance testability, the quality of the device itself must be exceedingly high. Extensive use has been made of built-in self-test. Approximately 96% of the BSM is covered by high-quality BIST that can be invoked in the system via the GPI interface.

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1189 324 299**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Bracknell),
FRANCE: **(33) 1 48 83 68 00** (Paris), SWEDEN: **(46) 8 600 7070** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 2 6606131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

Lucent Technologies Inc. reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information.

Copyright © 1998 Lucent Technologies Inc.
All Rights Reserved
Printed in U.S.A.

July 1998
PN98-167NTNB (Replaces PN92-008BSM)

microelectronics group

Lucent Technologies
Bell Labs Innovations