

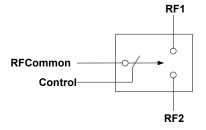
PE4220

Product Description

The PE4220 MOSFET RF Switch is designed to cover a broad range of uses in the 10 MHz through 2.5 GHz frequency range. This switch integrates on-board CMOS control logic with an internal charge pump, eliminating the need for a negative voltage supply. The control inputs are low voltage CMOS compatible.

The PE4220 MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi©) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram



SPDT Low Insertion Loss MOSFET RF Switch

Features

- Single 3.0 V Power Supply
- Low Insertion loss: 0.25 dB at 1.0 GHz, 0.65 dB at 2.0 GHz
- High isolation of 36 dB at 1.0 GHz, 26 dB at 2.0 GHz
- Typical 1 dB compression of +21 dBm
- Low voltage CMOS logic control
- Low Cost

Figure 2. Package Drawings

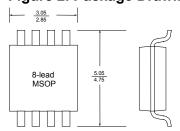


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Zs = ZL = 50 Ω)

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|--------------------------------|-----------------------------------|---------|--------------|---------|-----------|
| Operating Frequency | | 10 | | 2500 | MHz |
| Insertion Loss | 1000 MHz 2000 MHz | | 0.25 0.65 | | dB dB |
| Isolation | 1000 MHz 2000 MHz | | 36 26 | | dB dB |
| Return Loss | 1000 MHz 2000 MHz | | 20 14 | | dB dB |
| 'ON' Switching Time | CTRL to 0.1 dB final value, 2 GHz | | 200 | | ns |
| 'OFF' Switching Time | CTRL to 25 dB isolation, 2 GHz | | 90 | | ns |
| Full Cycle Switching Time | | | 5 | | μS |
| Video Feedthrough ¹ | | | 5.0 | | mV_{pp} |
| Input 1 dB Compression | 2000 MHz | | 21 | | dBm |
| Input IP3 | 2000 MHz, 8 dBm | | 39 | | dBm |



Figure 3. Pin Configuration

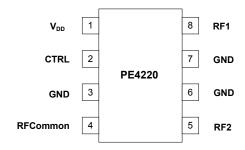


Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|-----------------|---|
| 1 | V _{DD} | Nominal 3 V supply connection. A bypass capacitor (100 pF) to the ground plane should be placed as close as possible to the pin |
| 2 | CTRL | CMOS or TTL logic level: High = RFCommon to RF1 signal path Low = RFCommon to RF2 signal path |
| 3 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 4 | RF Common | Common RF port for switch (Note 1) |
| 5 | RF2 | RF2 port (Note 1) |
| 6 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 7 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 8 | RF1 | RF1 port (Note 1) |

Note 1: All RF pins must be DC blocked with an external series capacitor.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|-----------------|-----------------------------------|------|--------------------------|-------|
| V_{DD} | Power supply voltage | -0.3 | 4.0 | V |
| Vı | Voltage on any input | -0.3 | V _{DD} + 0.3 | V |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| T _{OP} | Operating temperature range | -40 | 85 | °C |
| V_{ESD} | ESD voltage (Human Body Model) | 200 | | V |

Table 4. DC Electrical Specifications

| Parameter | Min | Тур | Max | Units |
|--------------------------------------|-------------------------|-----|-------------------------|-------|
| V _{DD} Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| Power Supply Current | | 29 | | μΑ |
| Control Voltage High | 0.7x V _{DD} | | | V |
| Control Voltage Low | | | 0.3x V _{DD} | V |

Table 5. Control Logic Truth Table

| Control Voltage | Signal Path | | |
|-----------------|-----------------|--|--|
| CTRL = High | RFCommon to RF1 | | |
| CTRL = Low | RFCommon to RF2 | | |

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.



Typical Performance Data @ +25 °C

Figure 4. Insertion Loss & Isolation

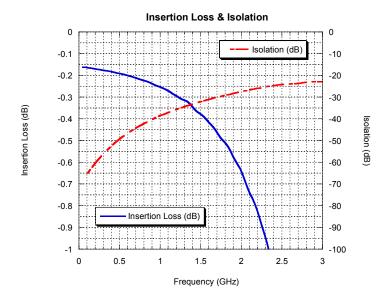


Figure 5. 1dB Compression Point & IP3

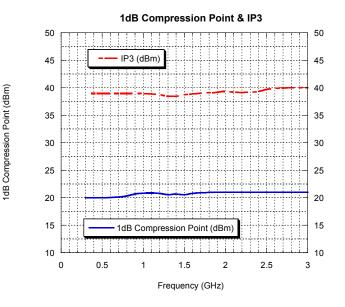


Figure 6. Switching Time

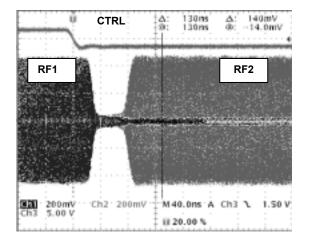
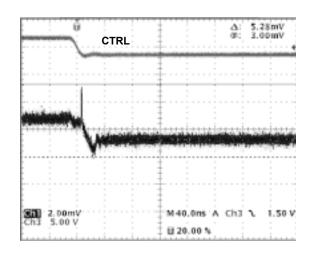


Figure 7. Video Feedthrough*

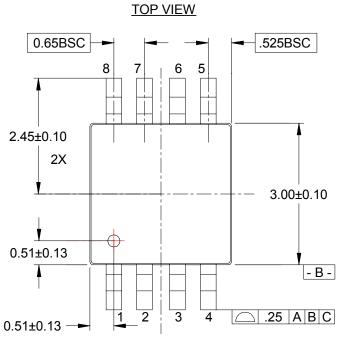


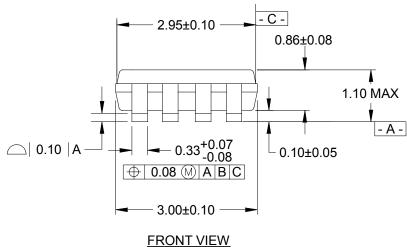
*The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 ohm test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

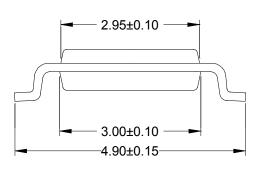


Figure 8. Package Drawing

8-lead MSOP







SIDE VIEW



Table 6. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---------------|--------------|-------------|----------------|--------------------|
| 4220-21 | 4220 | | 8-lead MSOP | 50 pcs. / Tube |
| 4220-22 | 4220 | | 8-lead MSOP | 2000 pcs. / T&R |
| 4220-00 | PE4220-EK | | Evaluation Kit | 1 / Box |

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Data Sheet Identification

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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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