Integrator Series FPGAs – 40MX and 42MX Families

Features

High Capacity

- 2,000 to 52,000 available logic gates
- Up to 3 Kbits configurable dual-port SRAM
- Fast wide-decode circuitry
- Up to 250 user-programmable I/O Pins

High Performance

- 250 MHz performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-bit Address Decode

Ease of Integration

- Mixed voltage operation (3.3 V or 5 V I/O)
- Synthesis-friendly architecture to support ASIC design methodologies
- 95–100% resource utilization, using automatic place-and-route tools with up to 100% pin fixing
- Deterministic, user-controllable timing via DirectTime software tools
- Supported by Actel Designer Series development system with interfaces to popular design environments such as Cadence, Exemplar, IST, Mentor Graphics, Synopsys, Synplicity, and Viewlogic
- Low power consumption (less than 100µA in stand-by mode)
- JTAG 1149.1 boundary scan testing
- 5.0V and 3.3V Programmable PCI-compliant I/O

General Description

Actel's new MX family of programmable logic devices provides system logic designers with a high-performance, cost-effective ASIC alternative in a single Actel FPGA.

The MX family architecture is based on Actel's patented antifuse technology, implemented in a 0.45µ triple-metal CMOS process. With capacities ranging from 2,000 to 52,000 gates, the synthesis-friendly MX family of devices provides data paths up to 250 MHz, are live on power-up, and deliver up to five times lower stand-by power consumption than any other FPGA device. With up to 250 I/O the MX FPGAs are available in a wide variety of packages.

Integrator Series Product Profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36	A42MX52
Capacity							
Gates	2,000	4,000	9,000	16,000	24,000	36,000	52,000
ASIC Equivalent Gates	1,200	2,000	4,000	8,000	14,000	20,000	30,000
SRAM Bits	N/A	N/A	N/A	N/A	N/A	2,560	3,072
Logic Modules							
Sequential	—	—	348	624	954	1230	1888
Combinatorial	295	547	336	608	912	1184	1833
Decode	—	—	N/A	N/A	24	24	28
SRAM Modules (64x4 or 32x8)	NA	NA	NA	NA	NA	10	12
Dedicated Flip-Flops	—	—	348	624	954	1,276	1,944
Clocks	1	1	2	2	2	6	6
User I/O (maximum)	57	69	104	140	176	202	250
JTAG	No	No	No	No	Yes	Yes	Yes
Packages	PL44 PL68 PQ100 VQ80	PL44 PL68 PL68 PQ100 VQ80	PL84 PQ100 PQ160 TQ176	PL84 PQ160 PQ208 TQ176	PL84 PQ160 PQ208 TQ176	PQ208 RQ208 RQ240	RQ208 RQ240

The MX Integrator family is comprised of the 40MX and the 42MX FPGAs. The 42MX devices also feature Actel's I/O which supports mixed voltage systems. I/Os can operate with either 0V to 5.0V swing, for 5.0V input tolerance, for 3.3V and mixed 5.0V/3.3V system operation. The logic core can be operated at 5.0V for maximum performance; or at 3.3V for minimum power consumption. The 42MX FPGA devices include system-level features such as JTAG, dual-port SRAM, fast wide-decode modules, and a programmable PCI interface. The 42MX FPGAs were designed to integrate system logic that is typically implemented in multiple CPLDs, PALs and FPGAs.

The 42MX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The large number of storage elements can efficiently address applications requiring wide data-path manipulation and can transformation functions such as telecommunications, networking, and DSP. Power consumption can be reduced to 100µA, providing an excellent solution for low-power systems. MultiPlex I/O includes selectable PCI output drives in certain 42MX devices, enabling 100% PCI compliance for both 5.0V and 3.3V systems.

Ordering Information

A42MX16 – PQ 100

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)

Package Lead Count

Package Type
- PL = Plastic Leaded Chip Carrier
- PQ = Plastic Quad Flatpack
- RQ = Plastic Power Quad Flatpack
- TQ = Thin (1.4 mm) Quad Flatpack
- VQ = Very Thin (1.0 mm) Quad Flatpack

Speed Grade
- Blank = Standard Speed
- 1 = Approximately 15% faster than Standard
- 2 = Approximately 25% faster than Standard
- 3 = Approximately 35% faster than Standard
- F = Approximately 40% slower than Standard

Part Number
- A40MX02 = 2,000 Gates
- A40MX04 = 4,000 Gates
- A42MX09 = 9,000 Gates
- A42MX16 = 16,000 Gates
- A42MX24 = 24,000 Gates
- A42MX36 = 36,000 Gates
- A42MX52 = 52,000 Gates

Product Plan

	Speed Grade					Application			
	Std	–1*	–2*	–3*	–F*	C	I	M	B
A40MX02 Device									
44-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
68-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
80-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
A40MX04 Device									
44-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
68-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
80-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
A42MX09 Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX16 Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX24 Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX36 Device									
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
208-pin Plastic Power Quad Flatpack (RQFP)	✔	✔	✔	—	✔	✔	✔	—	—
240-pin Plastic Power Quad Flatpack (RQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX52 Device									
208-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	—	P	P	P	—	—
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	—	P	P	P	—	—

Applications: *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883*

Availability: *✔ = Available* *P = Planned* *— = Not Planned*

** Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35% faster than Standard* *–F = Approx. 40% slower than Standard*

Integrator Series devices are supported by Actel's Designer Series development software, which provides a seamless integration into any ASIC design flow. The Designer Series development tools offer automatic placement and routing (even with preassigned pins), static timing analysis, user programming, and debug and diagnostic probe capabilities. In addition, the DirectTime tool provides deterministic as well as controllable timing. DirectTime allows the designer to specify the performance requirements of individual paths and system clocks. Using these specifications, the software will automatically optimize the placement and routing of the logic to meet the constraints. Included with the Designer Series tools is Actel's ACTgen™ Macro Builder. ACTgen allows the designer quickly to build fast, efficient logic functions such as counters, adders, FIFOs, and RAM.

The Designer Series tools provide designers with the capability to move up to high-level description languages, such as VHDL and Verilog, or to use schematic design entry with interfaces to most EDA tools. Designer Series is supported on 486 and Pentium PCs and on Sun® and HP® workstations. The software provides CAE interfaces to Cadence, Mentor Graphics®, Escalade, OrCAD™ and Viewlogic® design environments. Additional development tools are supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

Actel's FPGAs are an ideal solution for shortening the system design and development cycle, and they offer a cost-effective alternative for low-volume production runs. The 40MX and 42MX devices are an excellent choices for integrating logic that is currently implemented in multiple PALs, CPLDs, and FPGAs. Some example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and coprocessor functions.

Plastic Device Resources

Device	User I/Os									
	PLCC 44-pin	PLCC 68-pin	PLCC 84-pin	VQFP 80-pin	PQFP 100-pin	PQFP 160-pin	PQFP 208-pin	RQFP 208-pin	RQFP 240-pin	TQFP 176-pin
A40MX02	34	57	—	57	57	—	—	—	—	—
A40MX04	34	57	69	69	69	—	—	—	—	—
A42MX09	—	—	72	—	83	104	—	—	—	103
A42MX16	—	—	72	—	83	125	140	—	—	140
A42MX24	—	—	72	—	—	125	176	—	—	150
A42MX36	—	—	—	—	—	—	176	176	202	—
A42MX52	—	—	—	—	—	—	—	176	202	—

Package Definitions *(Consult your local Actel sales representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, RQFP = Plastic Power Quad Flat Pack

Pin Description

CLK, CLKA, CLKB
Clock Clock A and Clock B (input)
TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)
TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)
Input LOW supply voltage.

I/O Input/Output (Input, Output)
Input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

MODE Mode (Input)
Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). When the MODE pin is HIGH, the special functions are active. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required. To turn off input/output devices for low-power mode, MODE pin must be HIGH.

NC No Connection
Not connected to circuitry within the device.

PRA/I/O Probe A (Output)
Used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB/I/O Probe B (Output)
Used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B,C,D Quadrant Clock (Input/Output)
Quadrant clock inputs. When not used as a register control signal, these pins can function as general-purpose I/O.

SDI Serial Data Input (Input)
Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TCK Test Clock
Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In
Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out
Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

TMS Test Mode Select
Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

V_{CC} Supply Voltage (Input)
Input HIGH supply voltage.

V_{CCA} Supply Voltage (Input)
Input HIGH supply voltage, supplies array core only.

V_{CCI} Supply Voltage (Input)
Input HIGH supply voltage, supplies I/O cells only.

Note: *TCK, TDI, TDO, TMS are available only on devices containing JTAG circuitry.*

Connecting V_{CC} on MX Devices

40MX

The 40MX FPGAs will operate in 5.0V only systems, or 3.3V only systems.

V_{CC}	Input	Output
3.3V	3.3V	3.3V
5.0V	5.0V	5.0V

42MX

The 42MX FPGAs will operate in 5.0V only systems, 3.3V only systems, or mixed 5.0V/3.3V systems.

V_{CCA}	V_{CCI}	Input	Output
3.3V	3.3V	3.3V	3.3V
5.0V	3.3V	3.3V, 5.0V	3.3V
5.0V	5.0V	5.0V	5.0V

Integrator Series Architectural Overview

The 40MX and 42MX devices are composed of fine-grained building blocks that produce fast, efficient logic designs. All devices within the Integrator Series are composed of logic modules, routing resources, clock networks, and I/O modules, which are the building blocks for designing fast logic designs. In addition, a subset of devices contain embedded dual-port SRAM and wide decode modules. The dual-port SRAM modules are optimized for high-speed data-path functions such as FIFOs, LIFOs, and scratchpad memory. The “Integrator Series Product Profile” on page 1-91, lists the specific logic resources contained within each device.

Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 1).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array, since latches and flip-flops can be constructed from logic modules wherever needed in the application.

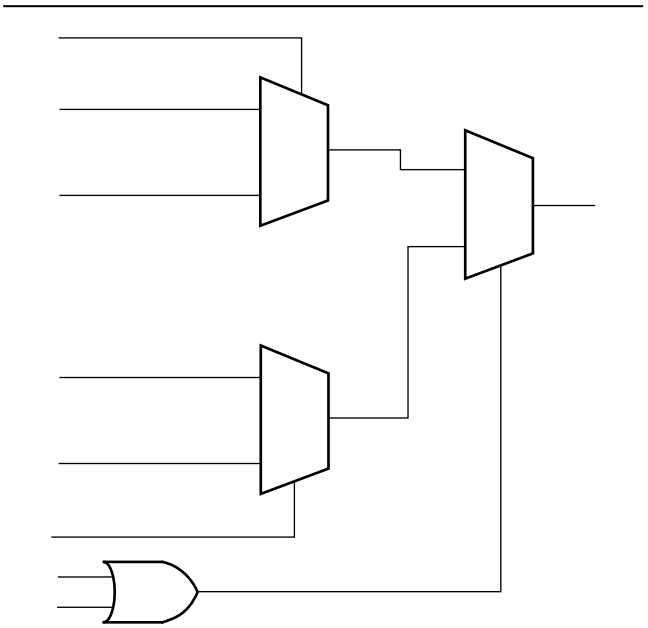


Figure 1 • *40MX Logic Module*

The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules).

The C-module is shown in Figure 2 and implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D01+S1*S0*D11

where

S0=A0*B0

S1=A1+B1

The S-module shown in Figure 3 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D flip-flop or a transparent latch. To increase flexibility, the S-module register can be by passed so that it implements purely combinatorial logic.

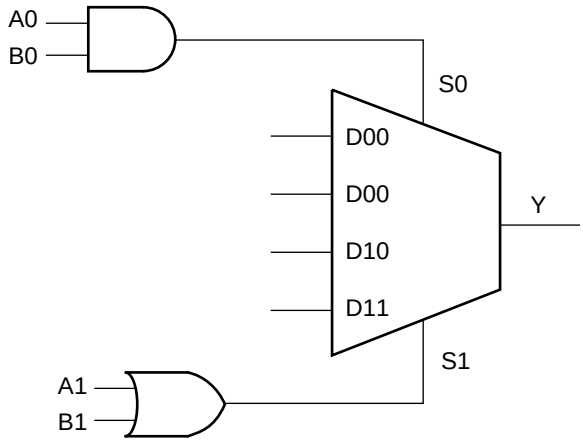
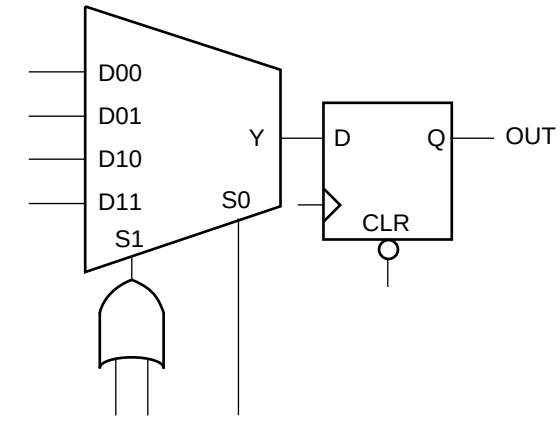
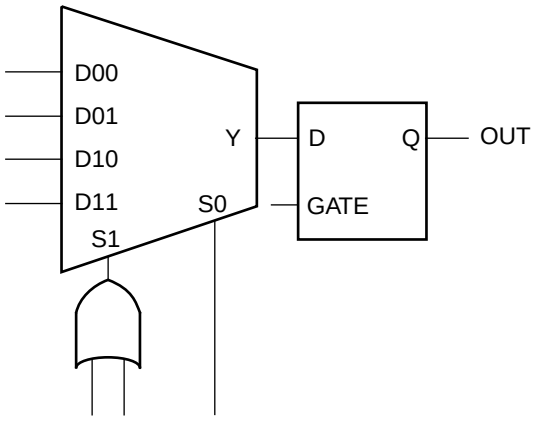


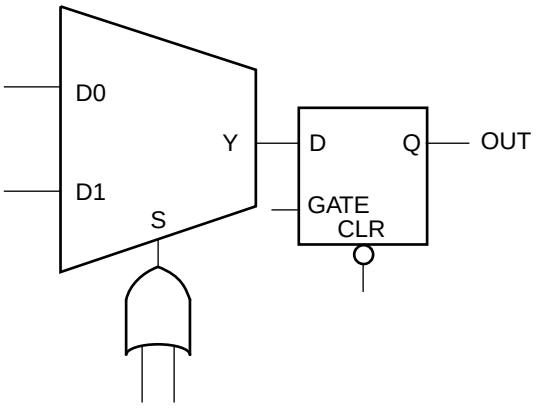
Figure 2 • *C-module Implementation*



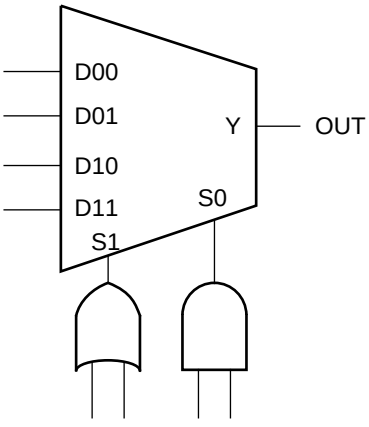
Up to 7-input function plus D-type flip-flop with clear



Up to 7-input function plus latch



Up to 4-input function plus latch with clear



Up to 8-input function (same as C-module)

Figure 3 • *S-module Implementation*

Some of the 42MX devices contain a third type of logic module, D-modules, which are arranged around the peripheries of the devices. D-modules contain wide-decode circuitry, which provides a fast, wide-input AND function similar to that found in product term architectures (Figure 4). The D-module allows 42MX devices to perform wide-decode functions at speeds comparable to CPLDs and PAL devices. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hard-wired to an output pin, or it can be fed back into the array to be incorporated into other logic.

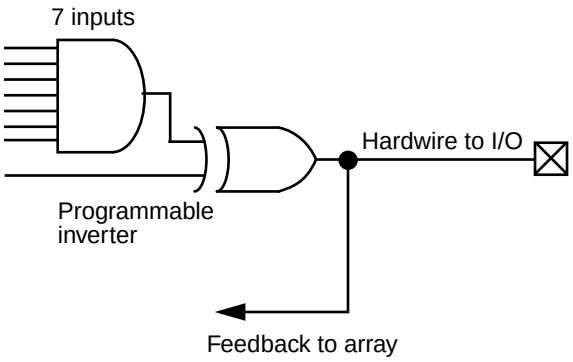


Figure 4 • *D-Module Implementation*

Dual-Port SRAM Modules

Several 42MX devices contain dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32 x 8 or 64 x 4. (Refer to the "Integrator Series Product Profile" table, on page 1-91, for the number of SRAM blocks within a particular device.) SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 42MX dual-port SRAM block is shown in Figure 5.

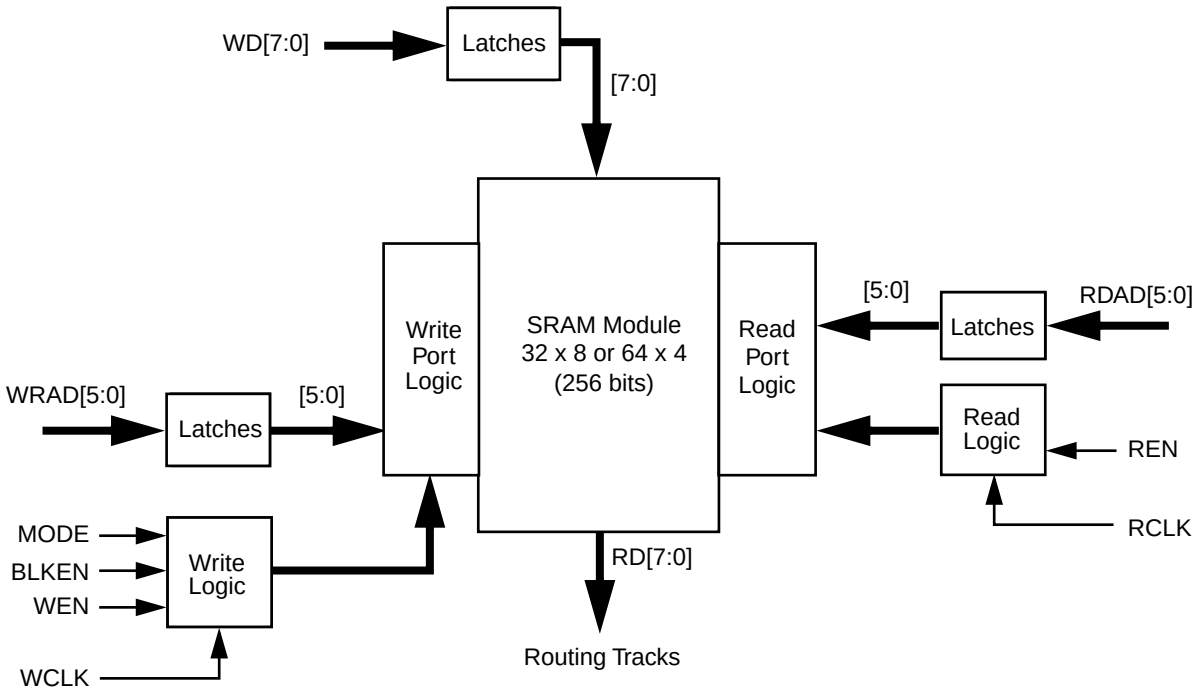


Figure 5 • *42MX Dual-Port SRAM Block*

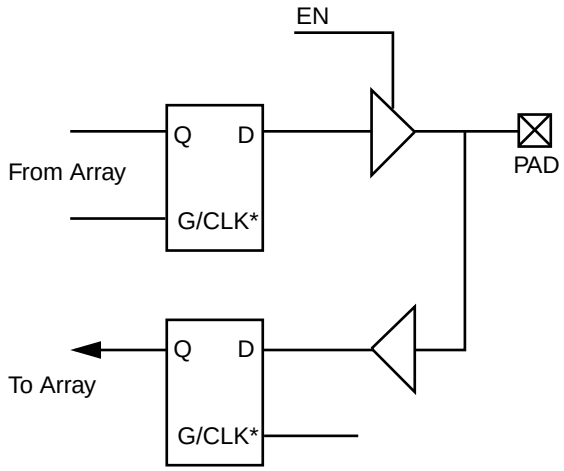
The 42MX SRAM modules are true dual-port structures containing independent Read and Write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64 x 4 bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 42MX dual-port SRAM blocks are ideal for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to design quickly memory functions, such as FIFOs, LIFOs, and

RAM arrays. In addition, unused SRAM blocks need not be wasted, since they can be used to implement registers for other logic within the design.

MultiPlex I/O Modules

The I/O modules provide the interface between the device pins and the logic array. The top of Figure 6 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (Refer to the Macro Library Guide for more information.) All 42MX I/O modules contain a tristate buffer, with input and output latches that can be configured for input, output, or bidirectional operation.



* Can be configured as a Latch or D Flip-Flop (using C-module)

Schematic

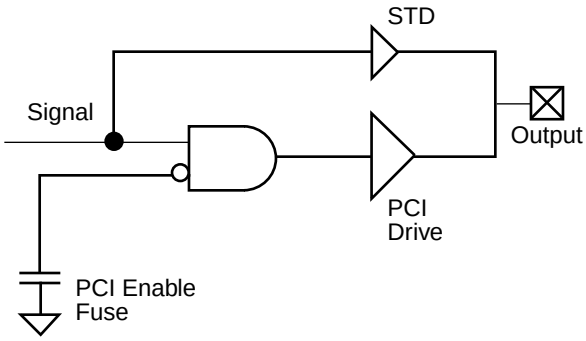


Figure 6 • *I/O Module*

The Integrator Series devices contain flexible I/O structures, in that each output pin has a dedicated output-enable control. The I/O module can be used to latch input or output data, or both, providing a fast setup time. In addition, the Actel Designer software tools can build a D flip-flop, using a C-module, to register input and output signals. To achieve 5.0V or 3.3V PCI-compliant output drives on A42MX24, A42MX36, and A42MX52, a chip-wide PCI fuse is programmed. When the PCI fuse is not programmed, output drive is standard. (See the bottom portion of Figure 6.)

Actel's Designer Series development tools provide a design library of I/O macros. The I/O macro library provides macrofunctions that can implement all I/O configurations supported by the MX FPGAs.

Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be either of continuous length or broken into pieces called *segments*. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends, using antifuses, to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Nondedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7.

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient

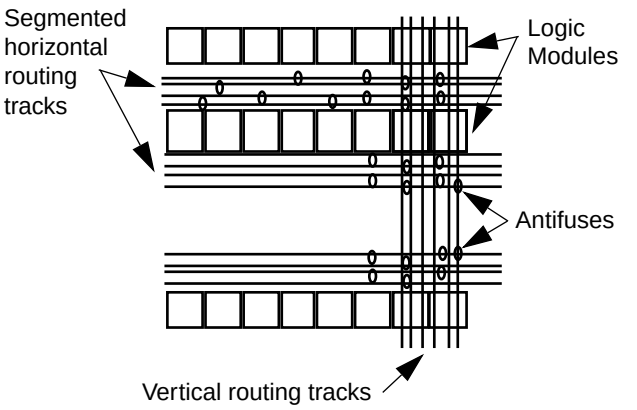


Figure 7 • *Routing Structure*

programming algorithms. The structure is highly testable because there are no preexisting connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Clock Networks

The 40MX devices have one global CLK distribution network. Two low-skew, high fanout clock distribution networks are provided in each 42MX device. These networks are referred to as *CLK0* and *CLK1*. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. The clock input pads can also be used as normal I/Os, bypassing the clock networks. (See Figure 8.)

The 42MX devices that contain SRAM modules have four additional register control resources, called quadrant clock

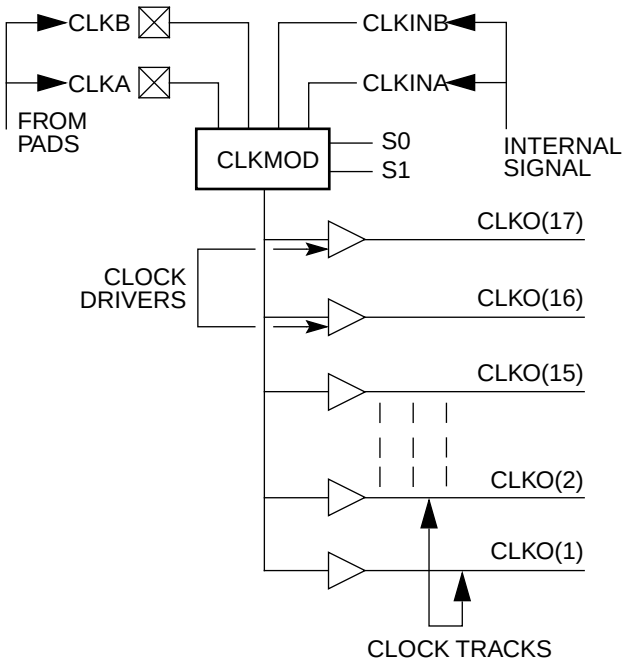


Figure 8 • *Clock Networks*

networks (Figure 9). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Test Circuitry

Both 40MX and 42MX devices provide the means to test and debug a design once it is programmed into a device. The 40MX and 42MX devices contain Actel's Actionprobe® test facility. Once a device has been programmed, the Actionprobe test facility allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, 42MX devices contain JTAG 1149.1 Boundary Scan Test.

JTAG Boundary Scan Testing (BST)

Device pin spacing is decreasing with the advent of fine-pitch packages such as TQFP and BGA, and manufacturers are routinely implementing surface-mount technology with multilayer PC boards. Boundary scan is becoming an attractive tool to help system manufacturers test their PC boards. The Joint Test Action Group (JTAG) developed the IEEE Boundary Scan standard 1149.1 to facilitate board-level testing during manufacturing.

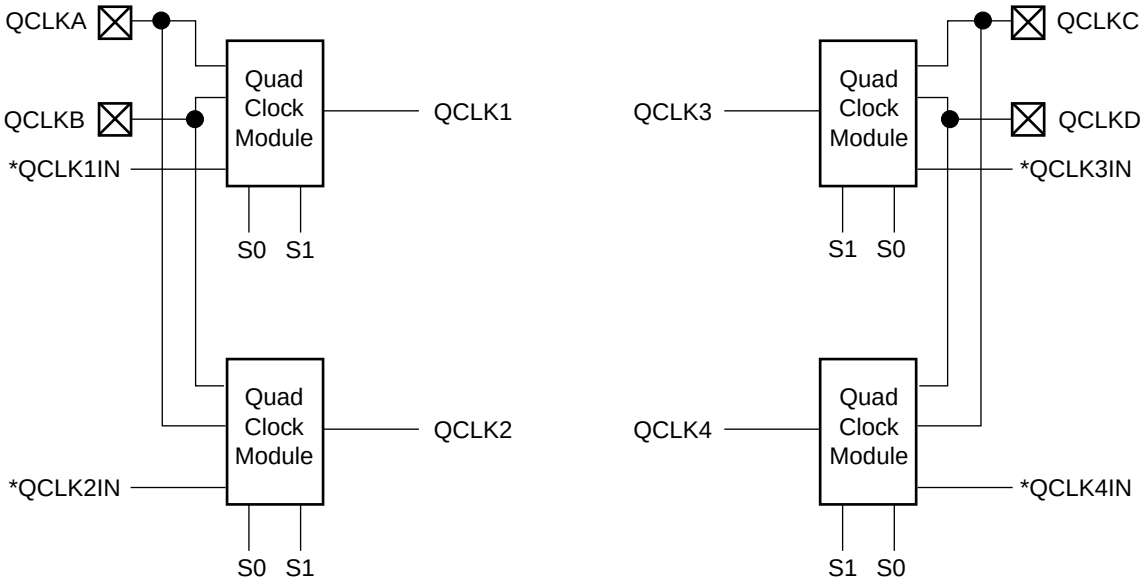
IEEE Standard 1149.1 defines a four-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 42MX family provides four JTAG BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCLK), and Test Mode Select (TMS). Devices are configured in a JTAG "chain"

where by BST data can be transmitted serially between devices via TDO-to-TDI interconnections. The TMS and TCLK signals are shared among all devices in the JTAG chain so that all components operate in the same state.

The 42MX family implements a subset of the IEEE 1149.1 BST instruction, in addition to a private instruction, to allow the use of Actel's Actionprobe facility with JTAG BST. Refer to the IEEE 1149.1 specification for detailed information regarding JTAG testing.

JTAG Architecture

The 42MX JTAG BST circuitry consist of a Test Access Port (TAP) controller, JTAG instruction register, a JPROBE register, a bypass register, and a boundary scan register. Figure 10 is a block diagram of the 42MX JTAG circuitry.



**QCLK1IN, QCLK2IN, QCLK3IN, and QCKL4IN are internally generated signals.*

Figure 9 • *Quadrant Clock Network*

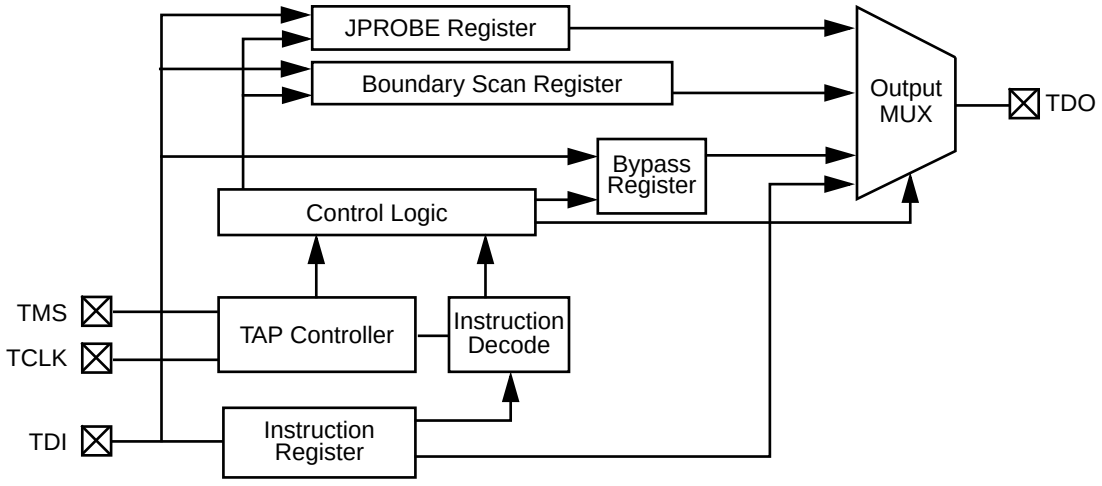


Figure 10 • *JTAG BST Circuitry*

When a device is operating in JTAG BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCLK signals. An active reset (nTRST) pin is not supported. However the 42MX contains power-on reset circuitry that resets the JTAG BST circuitry upon power-up. During normal device operation, the JTAG pins should be held LOW to disable the JTAG circuitry. The following table summarizes the functions of the JTAG BST signals.

JTAG Signal	Name	Function
TDI	Test Data In	Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK.
TDO	Test Data Out	Serial data output for JTAG instructions and test data.
TMS	Test Mode Select	Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK.
TCLK	Test Clock	Clock signal to shift the JTAG data into the device.

JTAG BST Instructions

JTAG BST testing within the 42MX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the JTAG testing of the device. The JTAG test mode is determined by the bit stream entered on the TMS pin. The table in the next column describes the JTAG instructions supported by the 42MX.

Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe diagnostic system provides the software and hardware required to perform real-time debugging. Refer to "Using the Actionprobe for System-Level Debug" application note for further information.

Test Mode	Code	Description
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/ PRELOAD	001	Allows a snapshot of the signals at the device pins to be captured and examined during device operation.
INTEST	010	Refer to the IEEE 1149.1 specification.
JPROBE	011	A private instruction allowing the user to connect Actel's Micro Probe registers to the JTAG chain.
USER INSTRUCTION	100	Allows the user to build application-specific instructions such as RAM READ and RAM WRITE.
HIGH Z	101	Refer to the IEEE 1149.1 specification.
CLAMP	110	Refer to the IEEE 1149.1 specification.
BYPASS	111	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the JTAG chain.

5.0V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source/Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial.*

Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –10 mA)[2]	2.4		2.4				V
	(I_{OH} = –6 mA)	3.84		3.84				V
	(I_{OH} = –4 mA)					3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5		0.5			V
	(I_{OL} = 6 mA)		0.33		0.33		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10	pF
Standby Current, I_{CC}[4] (typical = 1 mA)			1.0		20		10	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 1-21.						
Low Power Mode Standby Current, I_{CC}			0.1		20		10	mA
Power Current During Power-Up			1.0		20		10	mA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-pin CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = V_{CC} or GND; typical I_{CC} = 0.25 mA. I_{CC} limit includes I_{PP} and I_{SV} during normal operation.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
Power Supply Tolerance	±5	±10	%V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		3.7		V
	(I_{OH} = –3.2 mA)	2.4				V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4		0.48	V
V_{IL}		–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4] (typical = 0.3 mA)			0.75		0.75	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 1-21.				
Low Power Mode Standby Current, I_{CC}			0.1		10	mA
Power Current During Power-Up			1.0		10	mA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.*

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θjc, and the junction-to-ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{30°C/W} = 2.6W$$

Package Type	Pin Count	θja		Maximum Power Dissipation	
		Still Air	300 ft/min	Still Air	300 ft/min
Plastic Quad Flatpack	100	42 °C/W	33 °C/W	1.9 W	2.4 W
Plastic Quad Flatpack	160	34 °C/W	27 °C/W	2.4 W	3.0 W
Plastic Quad Flatpack	208	25 °C/W	16.2 °C/W	3.2 W	4.9 W
Plastic Leaded Chip Carrier	44	45 °C/W	35 °C/W	1.8 W	2.3 W
Plastic Leaded Chip Carrier	68	38 °C/W	29 °C/W	2.1 W	2.8 W
Plastic Leaded Chip Carrier	84	37 °C/W	28 °C/W	2.2 W	2.9 W
Thin Quad Flatpack	176	32 °C/W	25 °C/W	2.5 W	3.2 W
Power Quad Flatpack	208	16.8 °C/W	11.4 °C/W	4.8 W	7.0 W
Power Quad Flatpack	240	16.1 °C/W	10.6 °C/W	5.0 W	7.5 W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated for commercial, worst-case conditions:

I_{CC}	V_{CC}	Power
2 mA	5.25 V	10.5 mW

The static power dissipation by TTL loads depends on the number of outputs driving high or low and on the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low and 140 mW with all outputs driving high. The actual dissipation will average somewhere between, as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

F is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring $I_{CCactive}$ at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	5.2
Input Buffers (C_{EQI})	11.6
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.5

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

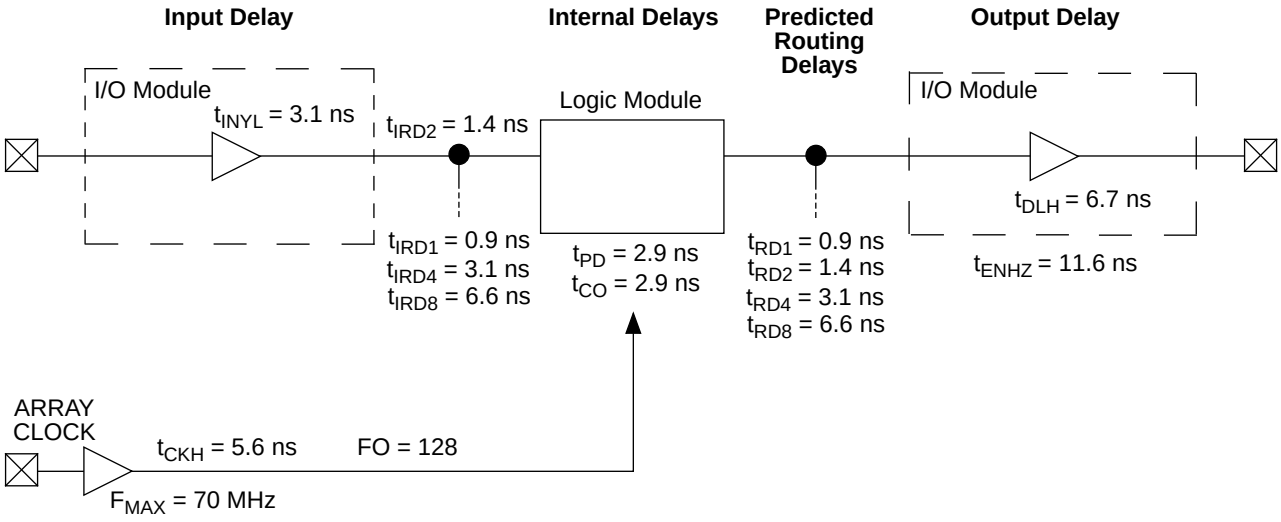
Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A40MX02	41.4	—
A40MX04	68.6	—
A40MX09	134	134
A42MX16	168	168
A42MX24	190	190
A42MX36	230	230
A42MX52	285	285

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

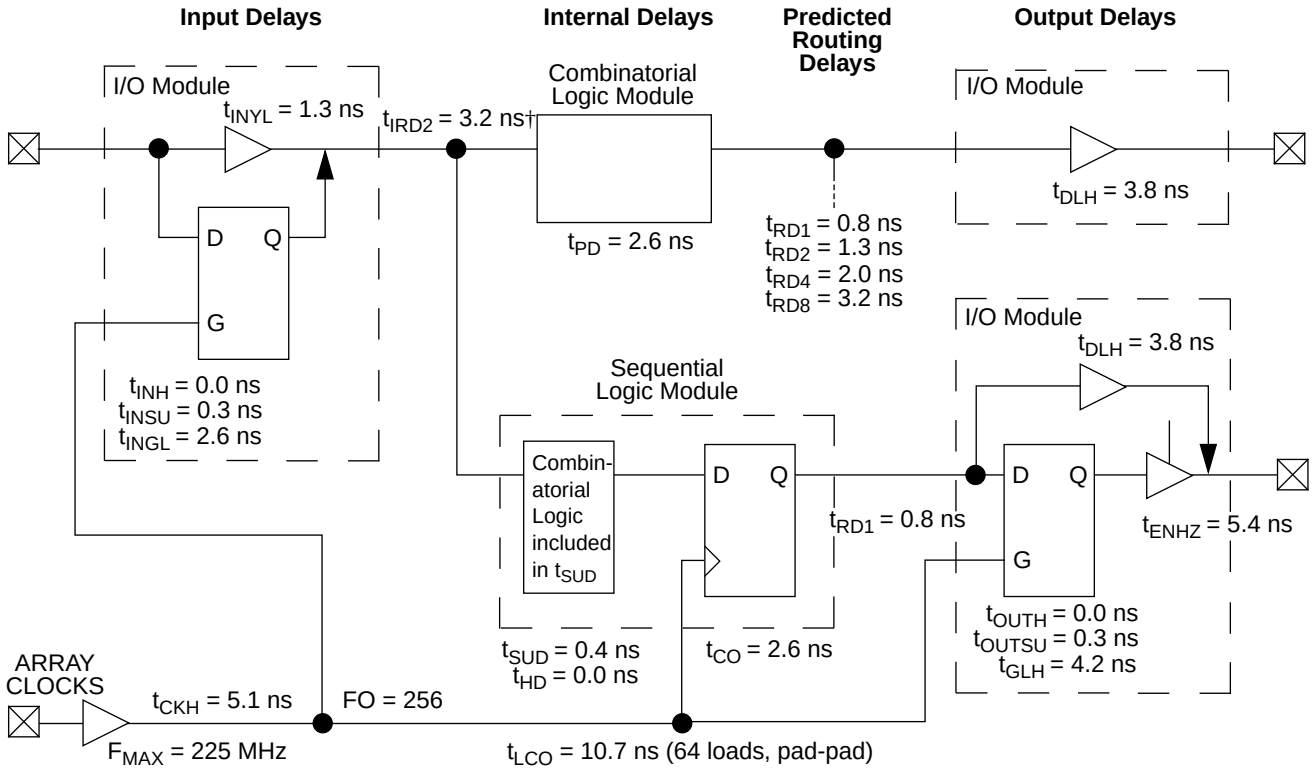
Logic Modules (m)	= 80% of combinatorial modules
Inputs switching (n)	= # of inputs/4
Outputs switching (p)	= # outputs/4
First routed array clock loads (q_1)	= 40% of sequential modules
Second routed array clock loads (q_2)	= 40% of sequential modules
Load capacitance (C_L)	= 35 pF
Average logic module switching rate (f_m)	= F/10
Average input switching rate (f_n)	= F/5
Average output switching rate (f_p)	= F/10
Average first routed array clock rate (f_{q1})	= F
Average second routed array clock rate (f_{q2})	= F/2

40MX Timing Model*



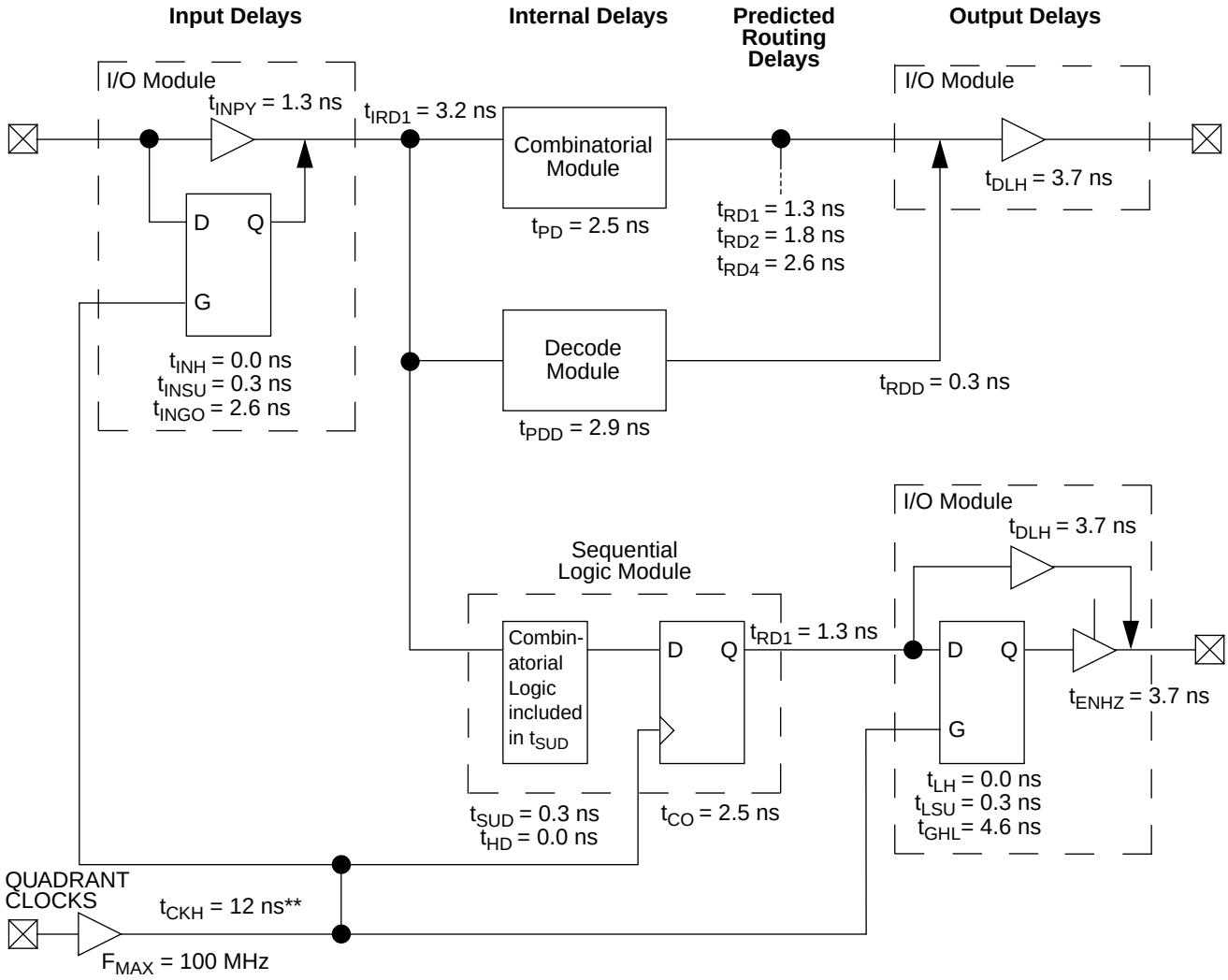
** Values are shown for 40MX '–3 speed' devices at worst-case commercial conditions.*

42MX Timing Model*



**Values are shown for A42MX09-2 at worst-case commercial conditions* *† Input module predicted routing delay*

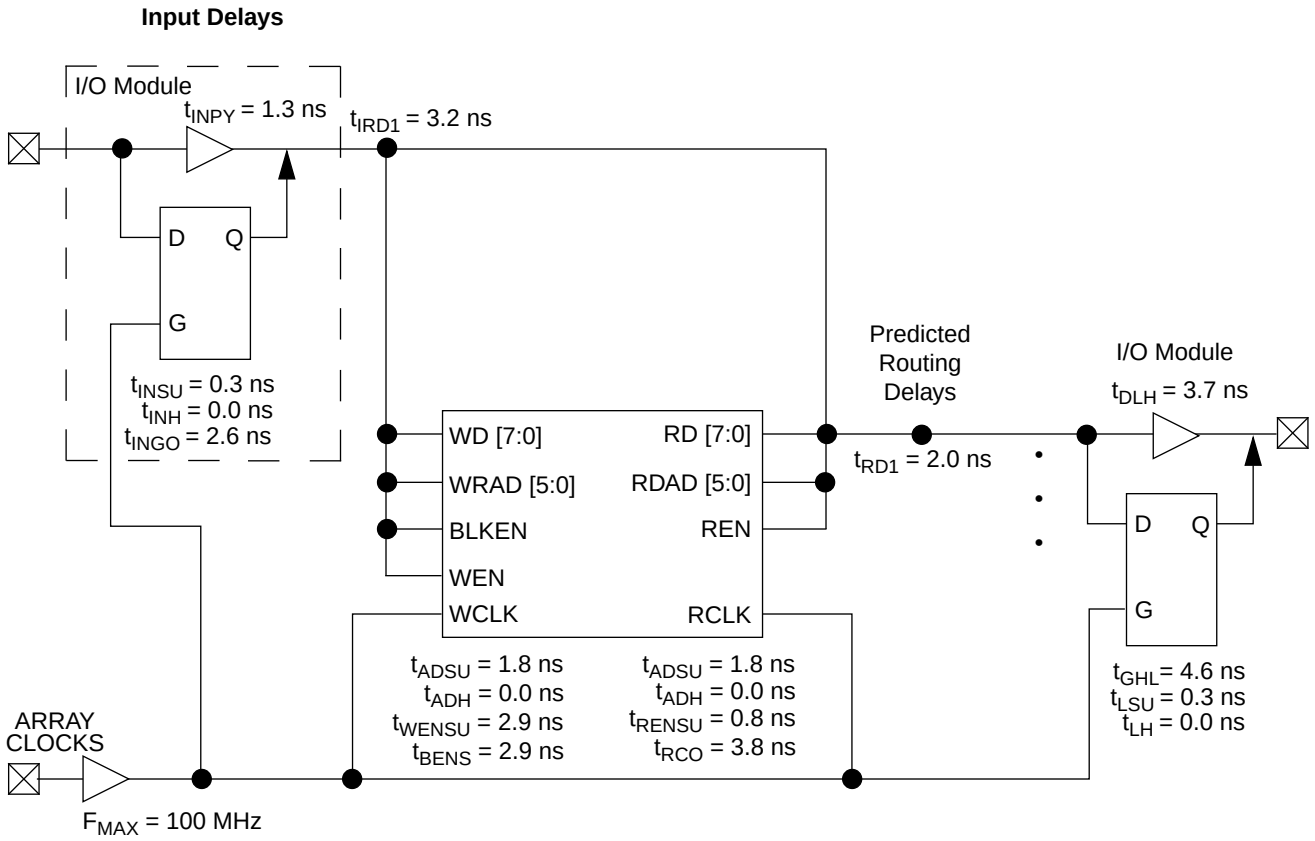
42MX Timing Model (Logic Functions using Quadrant Clocks)*



** Preliminary values are shown for A42MX36-2 at worst-case commercial conditions*

*** Load dependent*

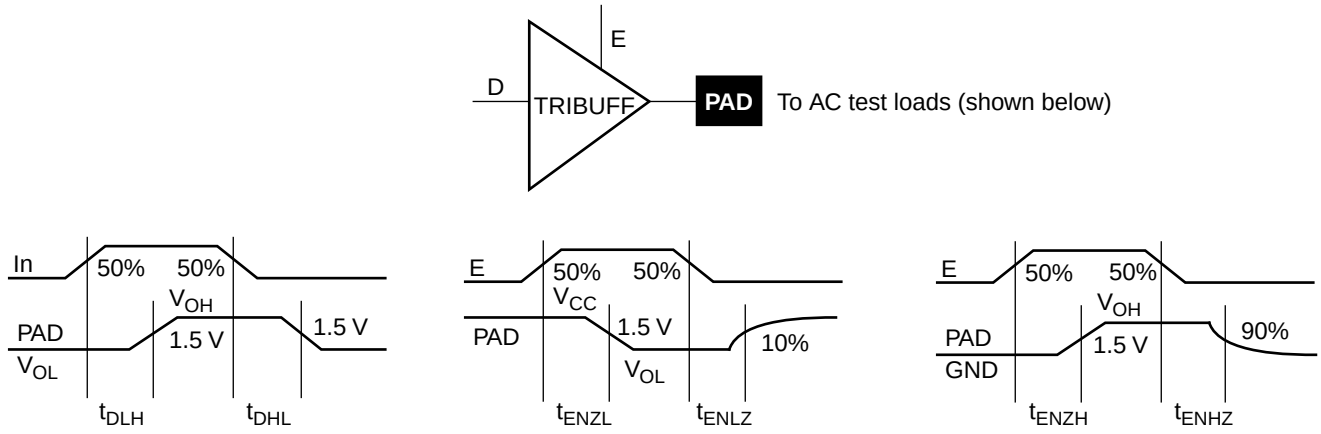
42MX Timing Model (SRAM Functions)*



**Values are shown for A42MX36-2 at worst-case commercial conditions.*

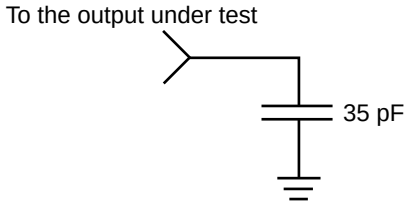
Parameter Measurement

Output Buffer Delays

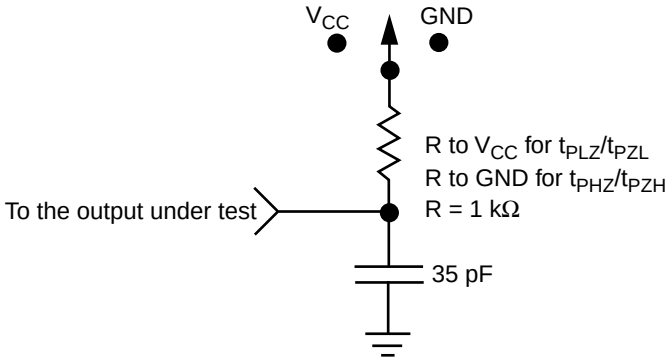


AC Test Loads

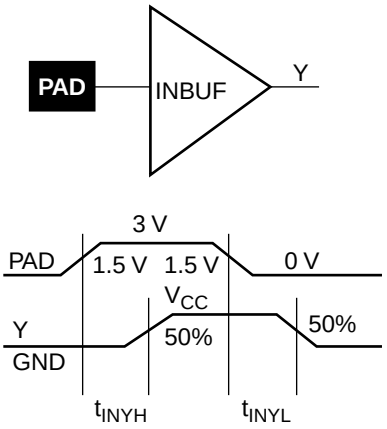
Load 1
(Used to measure propagation delay)



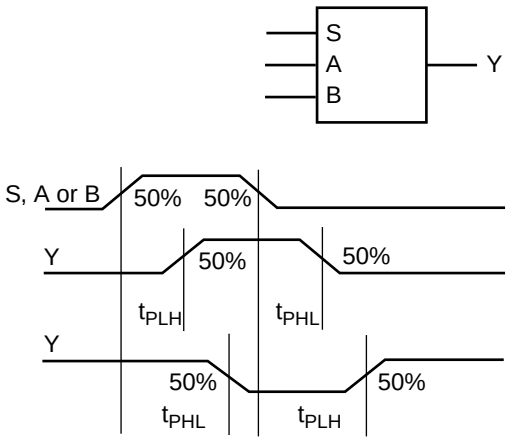
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

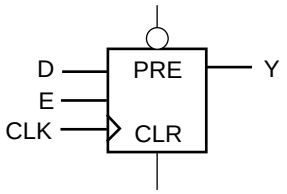


Module Delays

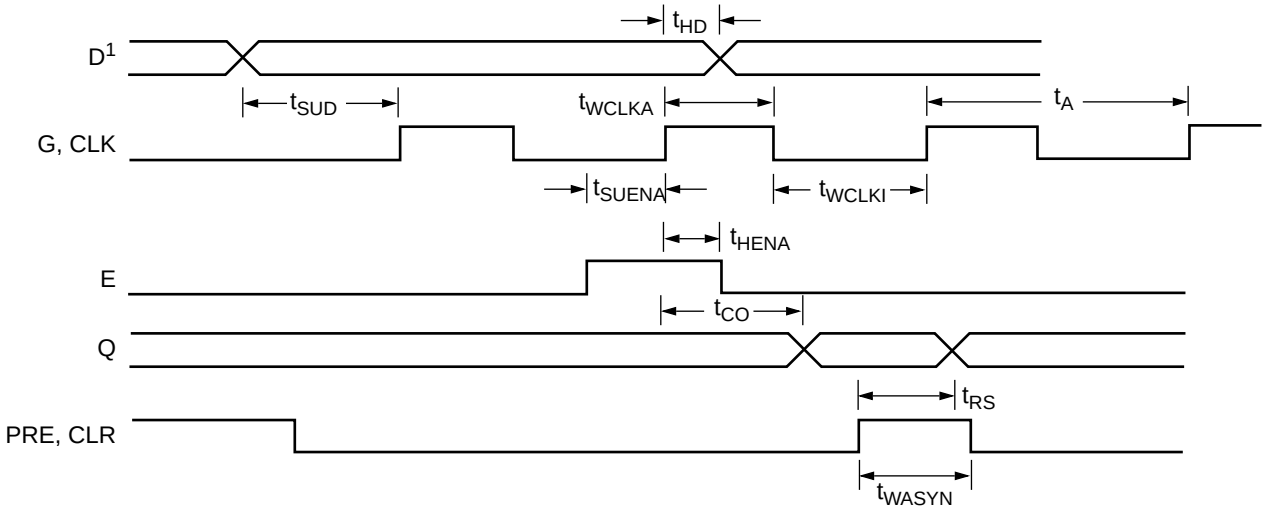


Sequential Module Timing Characteristics

Flip-Flops and Latches



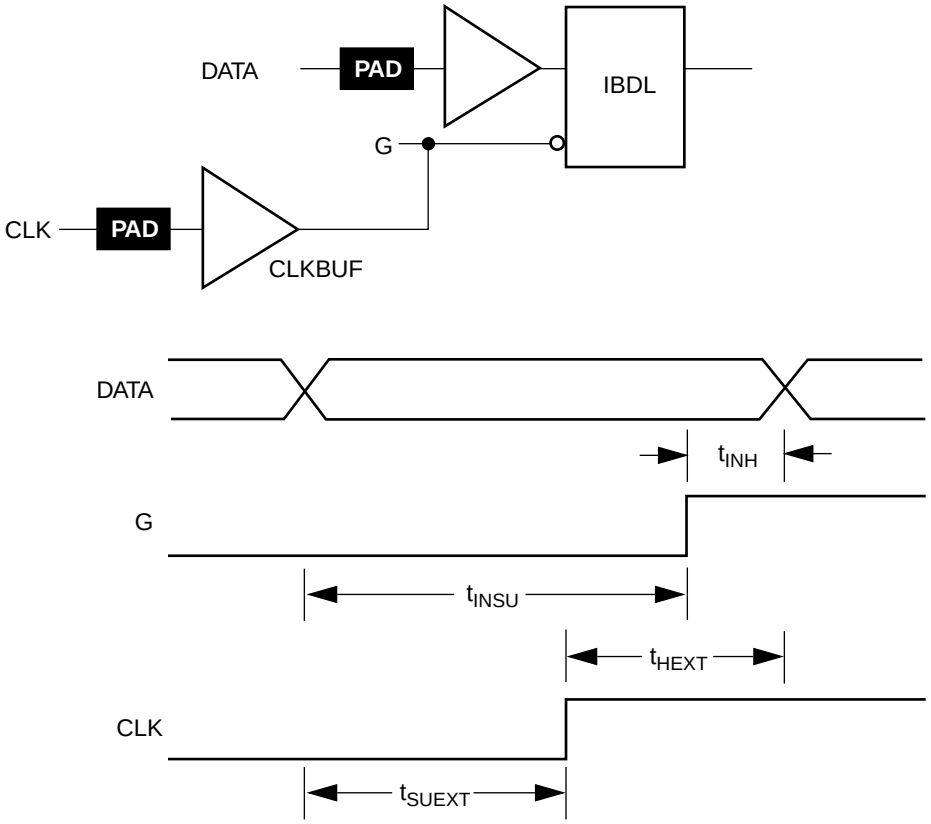
(Positive edge triggered)



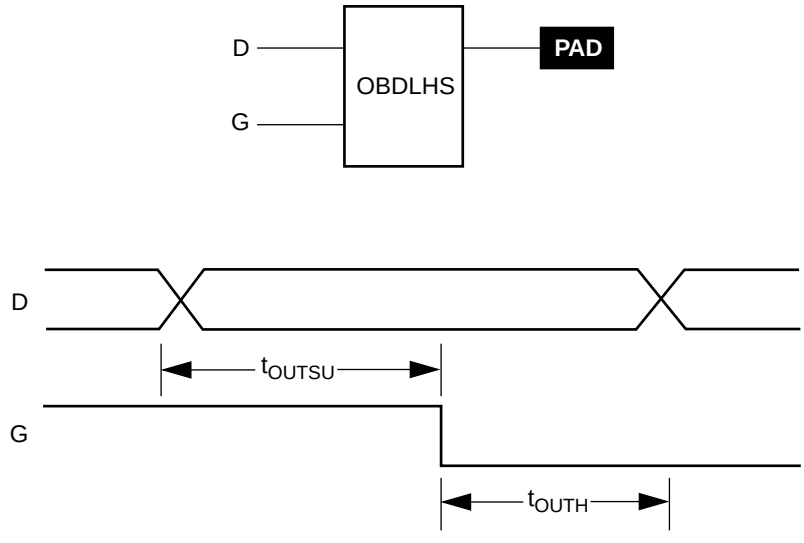
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

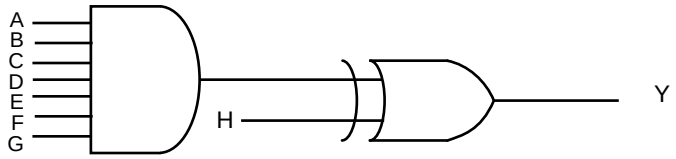
Input Buffer Latches

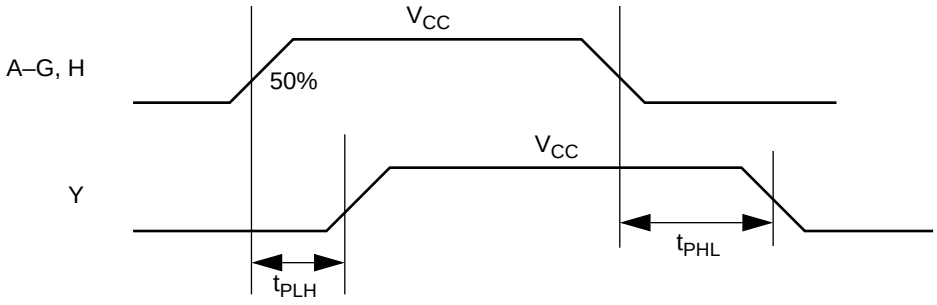


Output Buffer Latches

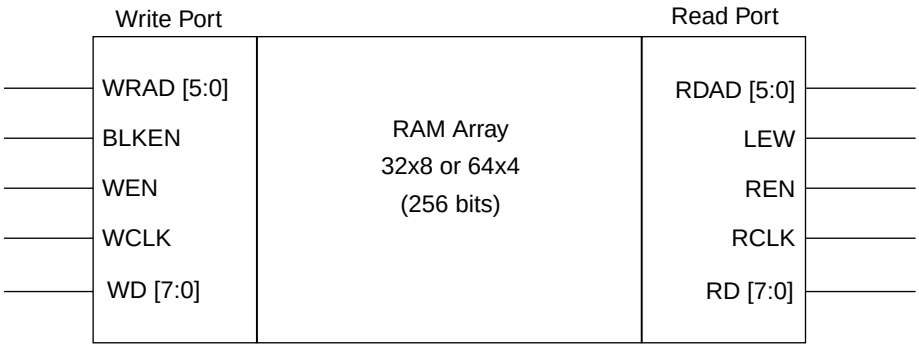


Decode Module Timing



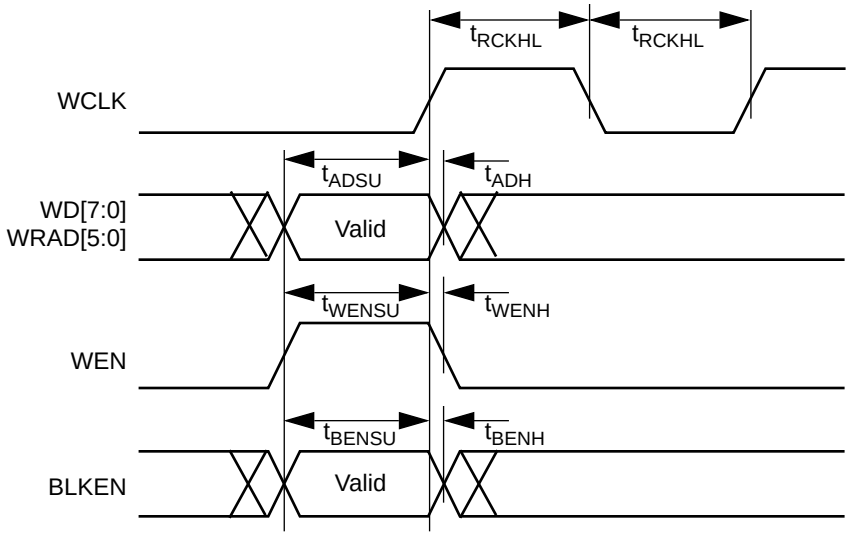


SRAM Timing Characteristics



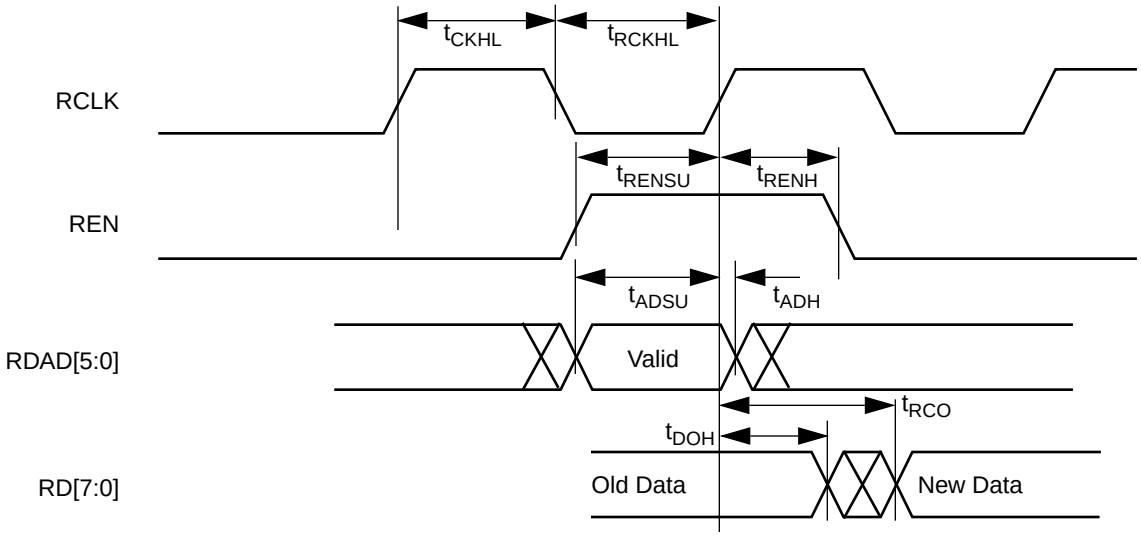
Dual-Port SRAM Timing Waveforms

42MX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

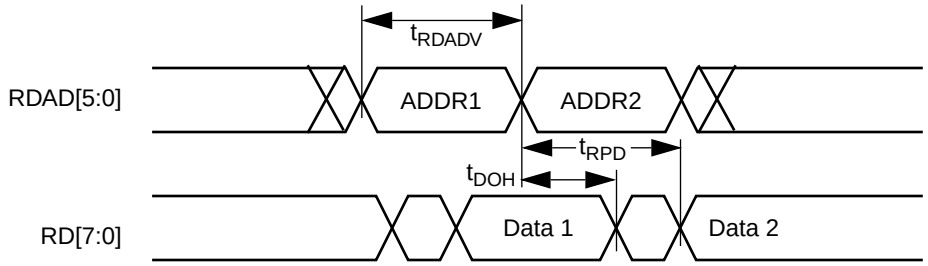
42MX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

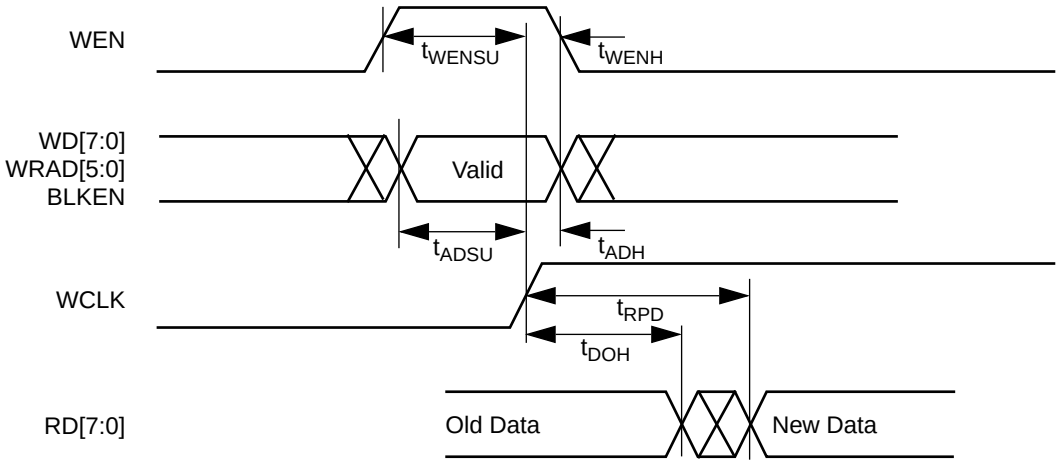
42MX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



42MX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers an extremely very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 micron lithography, offer nominal levels of 100 ohms resistance and 7.0 femtofarad (fF) capacitance per antifuse.

The Integrator Series fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all Integrator Series members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Designer Series utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Since the architecture provides deterministic timing and abundant routing resources, Actel's Designer Series development tools offers DirectTime, a timing-driven place-and-route tool. Using DirectTime, the designer can specify timing-critical nets and system clock frequency. Using these timing specifications, the place-and-route software optimizes the layout of the design to meet the user's specifications.

Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks add approximately 3 ns to 6 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A best-case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the standard-speed timing parameters and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial	
	Min.	**Max.**
(Commercial Specification) x	0.69	1.11

Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

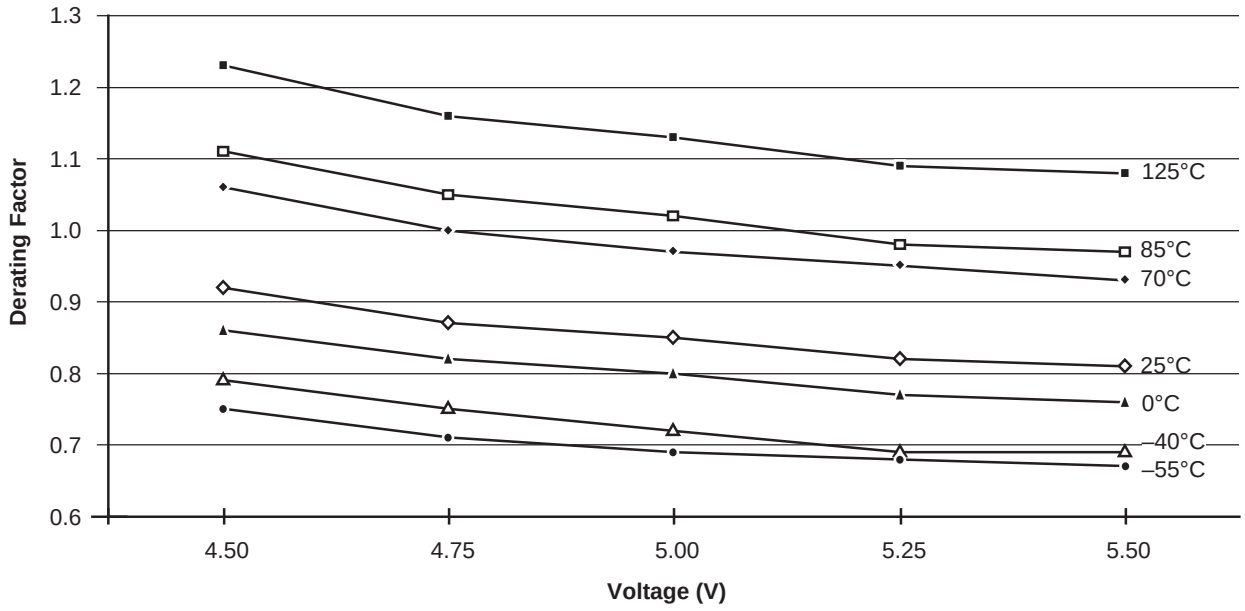
(Maximum Specification, Worst-Case Condition) x	0.85

Note: *This derating factor applies to all routing and propagation delays.*

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	–55	–40	0	25	70	85	125
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.16
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*

A40MX02 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.54		1.74		2.05		2.87	ns
t_{PD2}	Dual Module Macros		3.06		3.47		4.08		5.71	ns
t_{CO}	Sequential Clk to Q		1.54		1.74		2.05		2.87	ns
t_{GO}	Latch G to Q		1.54		1.74		2.05		2.87	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		1.54		1.74		2.05		2.87	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.48		1.67		1.97		2.76	ns
t_{RD2}	FO=2 Routing Delay		2.08		2.35		2.77		3.88	ns
t_{RD3}	FO=3 Routing Delay		2.69		3.04		3.58		5.01	ns
t_{RD4}	FO=4 Routing Delay		3.29		3.72		4.38		6.13	ns
t_{RD8}	FO=8 Routing Delay		5.69		6.45		7.59		10.63	ns
Sequential Timing Characteristics[3]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	3.38		3.83		4.50		6.30		ns
t_{HD}[4]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	3.38		3.83		4.50		6.30		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.13		4.68		5.50		7.70		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.13		4.68		5.50		7.70		ns
t_A	Flip-Flop Clock Input Period	5.59		6.33		7.45		10.43		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		167.50		154.10		134.00		80.40	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.*

A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.36		1.54		1.81		2.53	ns
t_{INYL}	Pad to Y Low			1.36		1.54		1.81		2.53	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.84		3.21		3.78		5.29	ns
t_{IRD2}	FO=2 Routing Delay			3.44		3.89		4.58		6.41	ns
t_{IRD3}	FO=3 Routing Delay			4.04		4.58		5.39		7.55	ns
t_{IRD4}	FO=4 Routing Delay			4.64		5.26		6.19		8.67	ns
t_{IRD8}	FO=8 Routing Delay			7.05		7.99		9.40		13.16	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 16		3.92		4.44		5.22		7.31	
		FO = 128		3.92		4.44		5.22		7.31	ns
t_{CKL}	Input High to Low	FO = 16		4.22		4.79		5.63		7.88	
		FO = 128		4.22		4.79		5.63		7.88	ns
t_{PWH}	Minimum Pulse Width High	FO = 16	2.58		2.92		3.44		4.82		
		FO = 128	2.71		3.07		3.61		5.05		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16	2.58		2.92		3.44		4.82		
		FO = 128	2.71		3.07		3.61		5.05		ns
t_{CKSW}	Maximum Skew	FO = 16		0.45		0.51		0.60		0.84	
		FO = 128		0.62		0.70		0.82		1.15	ns
t_P	Minimum Period	FO = 16	5.39		6.10		7.18		10.05		
		FO = 128	5.59		6.33		7.45		10.43		ns
f_{MAX}	Maximum Frequency	FO = 16		174.79		159.85		139.00		83.40	
		FO = 128		167.50		154.10		134.00		80.40	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.68		4.17		4.91		6.87	ns
t_{DHL}	Data to Pad Low		4.61		5.22		6.14		8.60	ns
t_{ENZH}	Enable Pad Z to High		4.38		4.96		5.84		8.18	ns
t_{ENZL}	Enable Pad Z to Low		5.44		6.16		7.25		10.15	ns
t_{ENHZ}	Enable Pad High to Z		7.40		8.39		9.87		13.82	ns
t_{ENLZ}	Enable Pad Low to Z		5.14		5.82		6.85		9.59	ns
d_{TLH}	Delta Low to High		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta High to Low		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.36		4.94		5.81		8.13	ns
t_{DHL}	Data to Pad Low		3.92		4.45		5.23		7.32	ns
t_{ENZH}	Enable Pad Z to High		4.03		4.56		5.37		7.52	ns
t_{ENZL}	Enable Pad Z to Low		5.66		6.41		7.54		10.56	ns
t_{ENHZ}	Enable Pad High to Z		7.40		8.39		9.87		13.82	ns
t_{ENLZ}	Enable Pad Low to Z		5.14		5.82		6.85		9.59	ns
d_{TLH}	Delta Low to High		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta High to Low		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneous Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A40MX02 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.15		2.44		2.87		4.02	ns
t_{PD2}	Dual Module Macros		4.28		4.86		5.71		8.00	ns
t_{CO}	Sequential Clk to Q		2.15		2.44		2.87		4.02	ns
t_{GO}	Latch G to Q		2.15		2.44		2.87		4.02	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.15		2.44		2.87		4.02	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		2.07		2.34		2.76		3.86	ns
t_{RD2}	FO=2 Routing Delay		2.91		3.30		3.88		5.43	ns
t_{RD3}	FO=3 Routing Delay		3.76		4.26		5.01		7.02	ns
t_{RD4}	FO=4 Routing Delay		4.60		5.21		6.13		8.58	ns
t_{RD8}	FO=8 Routing Delay		7.97		9.03		10.63		14.88	ns
Sequential Timing Characteristics[3]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	4.73		5.36		6.30		8.82		ns
t_{HD}[4]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	4.73		5.36		6.30		8.82		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.78		6.55		7.70		10.78		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.78		6.55		7.70		10.78		ns
t_A	Flip-Flop Clock Input Period	7.82		8.87		10.43		14.60		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		100.50		92.46		80.40		48.24	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
4. *The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.*

A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.90		2.15		2.53		3.55	ns
t_{INYL}	Pad to Y Low			1.90		2.15		2.53		3.55	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			3.97		4.50		5.29		7.41	ns
t_{IRD2}	FO=2 Routing Delay			4.81		5.45		6.41		8.89	ns
t_{IRD3}	FO=3 Routing Delay			5.66		6.41		7.55		10.56	ns
t_{IRD4}	FO=4 Routing Delay			6.50		7.37		8.67		12.13	ns
t_{IRD8}	FO=8 Routing Delay			9.87		11.19		13.16		18.42	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 16		5.48		6.21		7.31		10.23	
		FO = 128		5.48		6.21		7.31		10.23	ns
t_{CKL}	Input High to Low	FO = 16		5.91		6.70		7.88		11.03	
		FO = 128		5.91		6.70		7.88		11.03	ns
t_{PWH}	Minimum Pulse Width High	FO = 16	3.61		4.09		4.82		6.74		
		FO = 128	3.79		4.30		5.05		7.08		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16	3.61		4.09		4.82		6.74		
		FO = 128	3.79		4.30		5.05		7.08		ns
t_{CKSW}	Maximum Skew	FO = 16		0.63		0.71		0.84		1.18	
		FO = 128		0.86		0.98		1.15		1.61	ns
t_P	Minimum Period	FO = 16	7.54		8.54		10.05		14.07		
		FO = 128	7.82		8.87		10.43		14.60		ns
f_{MAX}	Maximum Frequency	FO = 16		104.88		95.91		83.40		50.04	
		FO = 128		100.50		92.46		80.40		48.24	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		5.16		5.84		6.87		9.62	ns
t_{DHL}	Data to Pad Low		6.45		7.31		8.60		12.03	ns
t_{ENZH}	Enable Pad Z to High		6.13		6.95		8.18		11.45	ns
t_{ENZL}	Enable Pad Z to Low		7.61		8.63		10.15		14.21	ns
t_{ENHZ}	Enable Pad High to Z		10.36		11.75		13.82		19.35	ns
t_{ENLZ}	Enable Pad Low to Z		7.19		8.15		9.59		13.43	ns
d_{TLH}	Delta Low to High		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta High to Low		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		6.10		6.91		8.13		11.39	ns
t_{DHL}	Data to Pad Low		5.49		6.22		7.32		10.25	ns
t_{ENZH}	Enable Pad Z to High		5.64		6.39		7.52		10.53	ns
t_{ENZL}	Enable Pad Z to Low		7.92		8.97		10.56		14.78	ns
t_{ENHZ}	Enable Pad High to Z		10.36		11.75		13.82		19.35	ns
t_{ENLZ}	Enable Pad Low to Z		7.19		8.15		9.59		13.43	ns
d_{TLH}	Delta Low to High		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta High to Low		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneous Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A40MX04 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.54		1.74		2.05		2.87	ns
t_{PD2}	Dual Module Macros		3.06		3.47		4.08		5.71	ns
t_{CO}	Sequential Clk to Q		1.54		1.74		2.05		2.87	ns
t_{GO}	Latch G to Q		1.54		1.74		2.05		2.87	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		1.54		1.74		2.05		2.87	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.48		1.67		1.97		2.76	ns
t_{RD2}	FO=2 Routing Delay		2.08		2.35		2.77		3.88	ns
t_{RD3}	FO=3 Routing Delay		2.69		3.04		3.58		5.01	ns
t_{RD4}	FO=4 Routing Delay		3.29		3.72		4.38		6.13	ns
t_{RD8}	FO=8 Routing Delay		5.69		6.45		7.59		10.63	ns
Sequential Timing Characteristics[3]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	3.38		3.83		4.50		6.30		ns
t_{HD}[4]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	3.38		3.83		4.50		6.30		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.13		4.68		5.50		7.70		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.13		4.68		5.50		7.70		ns
t_A	Flip-Flop Clock Input Period	5.59		6.33		7.45		10.43		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		167.50		154.10		134.00		80.40	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.*

A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.36		1.54		1.81		2.53	ns
t_{INYL}	Pad to Y Low			1.36		1.54		1.81		2.53	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.84		3.21		3.78		5.29	ns
t_{IRD2}	FO=2 Routing Delay			3.44		3.89		4.58		6.41	ns
t_{IRD3}	FO=3 Routing Delay			4.04		4.58		5.39		7.55	ns
t_{IRD4}	FO=4 Routing Delay			4.64		5.26		6.19		8.67	ns
t_{IRD8}	FO=8 Routing Delay			7.05		7.99		9.40		13.16	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 16		3.92		4.44		5.22		7.31	
		FO = 128		3.92		4.44		5.22		7.31	ns
t_{CKL}	Input High to Low	FO = 16		4.22		4.79		5.63		7.88	
		FO = 128		4.22		4.79		5.63		7.88	ns
t_{PWH}	Minimum Pulse Width High	FO = 16	2.58		2.92		3.44		4.82		
		FO = 128	2.71		3.07		3.61		5.05		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16	2.58		2.92		3.44		4.82		
		FO = 128	2.71		3.07		3.61		5.05		ns
t_{CKSW}	Maximum Skew	FO = 16		0.45		0.51		0.60		0.84	
		FO = 128		0.62		0.70		0.82		1.15	ns
t_P	Minimum Period	FO = 16	5.39		6.10		7.18		10.05		
		FO = 128	5.59		6.33		7.45		10.43		ns
f_{MAX}	Maximum Frequency	FO = 16		174.79		159.85		139.00		83.40	
		FO = 128		167.50		154.10		134.00		80.40	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.68		4.17		4.91		6.87	ns
t_{DHL}	Data to Pad Low		4.61		5.22		6.14		8.60	ns
t_{ENZH}	Enable Pad Z to High		4.38		4.96		5.84		8.18	ns
t_{ENZL}	Enable Pad Z to Low		5.44		6.16		7.25		10.15	ns
t_{ENHZ}	Enable Pad High to Z		7.40		8.39		9.87		13.82	ns
t_{ENLZ}	Enable Pad Low to Z		5.14		5.82		6.85		9.59	ns
d_{TLH}	Delta Low to High		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta High to Low		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.36		4.94		5.81		8.13	ns
t_{DHL}	Data to Pad Low		3.92		4.45		5.23		7.32	ns
t_{ENZH}	Enable Pad Z to High		4.03		4.56		5.37		7.52	ns
t_{ENZL}	Enable Pad Z to Low		5.66		6.41		7.54		10.56	ns
t_{ENHZ}	Enable Pad High to Z		7.40		8.39		9.87		13.82	ns
t_{ENLZ}	Enable Pad Low to Z		5.14		5.82		6.85		9.59	ns
d_{TLH}	Delta Low to High		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta High to Low		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneous Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A40MX04 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.15		2.44		2.87		4.02	ns
t_{PD2}	Dual Module Macros		4.28		4.86		5.71		8.00	ns
t_{CO}	Sequential Clk to Q		2.15		2.44		2.87		4.02	ns
t_{GO}	Latch G to Q		2.15		2.44		2.87		4.02	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.15		2.44		2.87		4.02	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		2.07		2.34		2.76		3.86	ns
t_{RD2}	FO=2 Routing Delay		2.91		3.30		3.88		5.43	ns
t_{RD3}	FO=3 Routing Delay		3.76		4.26		5.01		7.02	ns
t_{RD4}	FO=4 Routing Delay		4.60		5.21		6.13		8.58	ns
t_{RD8}	FO=8 Routing Delay		7.97		9.03		10.63		14.88	ns
Sequential Timing Characteristics[3]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	4.73		5.36		6.30		8.82		ns
t_{HD}[4]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	4.73		5.36		6.30		8.82		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.78		6.55		7.70		10.78		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.78		6.55		7.70		10.78		ns
t_A	Flip-Flop Clock Input Period	7.82		8.87		10.43		14.60		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		100.50		92.46		80.40		48.24	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
4. *The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.*

A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.90		2.15		2.53		3.55	ns
t_{INYL}	Pad to Y Low			1.90		2.15		2.53		3.55	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			3.97		4.50		5.29		7.41	ns
t_{IRD2}	FO=2 Routing Delay			4.81		5.45		6.41		8.89	ns
t_{IRD3}	FO=3 Routing Delay			5.66		6.41		7.55		10.56	ns
t_{IRD4}	FO=4 Routing Delay			6.50		7.37		8.67		12.13	ns
t_{IRD8}	FO=8 Routing Delay			9.87		11.19		13.16		18.42	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 16		5.48		6.21		7.31		10.23	
		FO = 128		5.48		6.21		7.31		10.23	ns
t_{CKL}	Input High to Low	FO = 16		5.91		6.70		7.88		11.03	
		FO = 128		5.91		6.70		7.88		11.03	ns
t_{PWH}	Minimum Pulse Width High	FO = 16	3.61		4.09		4.82		6.74		
		FO = 128	3.79		4.30		5.05		7.08		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16	3.61		4.09		4.82		6.74		
		FO = 128	3.79		4.30		5.05		7.08		ns
t_{CKSW}	Maximum Skew	FO = 16		0.63		0.71		0.84		1.18	
		FO = 128		0.86		0.98		1.15		1.61	ns
t_P	Minimum Period	FO = 16	7.54		8.54		10.05		14.07		
		FO = 128	7.82		8.87		10.43		14.60		ns
f_{MAX}	Maximum Frequency	FO = 16		104.88		95.91		83.40		50.04	
		FO = 128		100.50		92.46		80.40		48.24	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		5.16		5.84		6.87		9.62	ns
t_{DHL}	Data to Pad Low		6.45		7.31		8.60		12.03	ns
t_{ENZH}	Enable Pad Z to High		6.13		6.95		8.18		11.45	ns
t_{ENZL}	Enable Pad Z to Low		7.61		8.63		10.15		14.21	ns
t_{ENHZ}	Enable Pad High to Z		10.36		11.75		13.82		19.35	ns
t_{ENLZ}	Enable Pad Low to Z		7.19		8.15		9.59		13.43	ns
d_{TLH}	Delta Low to High		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta High to Low		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		6.10		6.91		8.13		11.39	ns
t_{DHL}	Data to Pad Low		5.49		6.22		7.32		10.25	ns
t_{ENZH}	Enable Pad Z to High		5.64		6.39		7.52		10.53	ns
t_{ENZL}	Enable Pad Z to Low		7.92		8.97		10.56		14.78	ns
t_{ENHZ}	Enable Pad High to Z		10.36		11.75		13.82		19.35	ns
t_{ENLZ}	Enable Pad Low to Z		7.19		8.15		9.59		13.43	ns
d_{TLH}	Delta Low to High		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta High to Low		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneous Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A42MX09 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.55		1.76		2.07		2.90	ns
t_{CO}	Sequential Clk to Q		1.37		1.56		1.83		2.56	ns
t_{GO}	Latch G to Q		1.33		1.50		1.77		2.48	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		1.37		1.56		1.83		2.56	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		0.70		0.79		0.93		1.30	ns
t_{RD2}	FO=2 Routing Delay		0.97		1.10		1.29		1.81	ns
t_{RD3}	FO=3 Routing Delay		1.24		1.40		1.65		2.31	ns
t_{RD4}	FO=4 Routing Delay		1.51		1.71		2.01		2.81	ns
t_{RD8}	FO=8 Routing Delay		2.59		2.93		3.45		4.83	ns
Sequential Timing Characteristics[3, 4]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.36		0.41		0.48		0.67		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.45		0.51		0.60		0.84		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.77		4.27		5.02		7.03		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.94		5.59		6.58		9.21		ns
t_A	Flip-Flop Clock Input Period	4.50		5.10		6.00		8.40		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.30		0.4		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.30		0.4		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		225		207		180		108	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.16		1.32		1.55		2.17	ns
t_{INYL}	Pad to Y Low			1.43		1.62		1.91		2.67	ns
t_{INGH}	G to Y High			0.54		0.61		0.72		1.01	ns
t_{INGL}	G to Y Low			5.30		6.00		7.06		9.88	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.05		2.32		2.73		3.82	ns
t_{IRD2}	FO=2 Routing Delay			2.34		2.65		3.12		4.37	ns
t_{IRD3}	FO=3 Routing Delay			2.64		2.99		3.52		4.93	ns
t_{IRD4}	FO=4 Routing Delay			2.94		3.33		3.92		5.49	ns
t_{IRD8}	FO=8 Routing Delay			4.13		4.68		5.50		7.70	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 32 FO = 256		2.75 3.15		3.11 3.57		3.66 4.20		5.12 5.88	ns ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		2.54 2.93		2.88 3.32		3.39 3.90		4.75 5.46	ns ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	1.35 1.46		1.53 1.66		1.80 1.95		2.52 2.73		ns ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	1.35 1.46		1.53 1.66		1.80 1.95		2.52 2.73		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.34 0.34		0.38 0.38		0.45 0.45		0.63 0.63	ns ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 256	0.54 0.54		0.61 0.61		0.72 0.72		1.01 1.01		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	0.00 0.00		0.00 0.00		0.00 0.00		0.00 0.00		ns ns
t_P	Minimum Period	FO = 32 FO = 256	4.20 4.50		4.76 5.10		5.60 6.00		7.84 8.40		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		250 225		230 207		200 180		120 108	MHz MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		2.71		3.07		3.61		5.05	ns
t_{DHL}	Data to Pad Low		3.19		3.61		4.25		5.95	ns
t_{ENZH}	Enable Pad Z to High		2.93		3.32		3.90		5.46	ns
t_{ENZL}	Enable Pad Z to Low		3.24		3.67		4.32		6.05	ns
t_{ENHZ}	Enable Pad High to Z		5.44		6.16		7.25		10.15	ns
t_{ENLZ}	Enable Pad Low to Z		5.93		6.72		7.90		11.06	ns
t_{GLH}	G to Pad High		4.61		5.22		6.14		8.60	ns
t_{GHL}	G to Pad Low		4.61		5.22		6.14		8.60	ns
t_{LSU}	I/O Latch Setup	0.54		0.61		0.72		1.01		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		6.90		7.82		9.20		12.88	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		9.68		10.97		12.90		18.06	ns
d_{TLH}	Capacity Loading, Low to High		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, High to Low		0.04		0.04		0.07		0.07	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.44		3.89		4.58		6.41	ns
t_{DHL}	Data to Pad Low		2.66		3.02		3.55		4.97	ns
t_{ENZH}	Enable Pad Z to High		2.93		3.32		3.90		5.46	ns
t_{ENZL}	Enable Pad Z to Low		3.24		3.67		4.32		6.05	ns
t_{ENHZ}	Enable Pad High to Z		5.44		6.16		7.25		10.15	ns
t_{ENLZ}	Enable Pad Low to Z		5.93		6.72		7.90		11.06	ns
t_{GLH}	G to Pad High		4.61		5.22		6.14		8.60	ns
t_{GHL}	G to Pad Low		4.61		5.22		6.14		8.60	ns
t_{LSU}	I/O Latch Setup	0.54		0.61		0.72		1.01		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		6.90		7.82		9.20		12.88	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		9.68		10.97		12.90		18.06	ns
d_{TLH}	Capacity Loading, Low to High		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, High to Low		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX09 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.17		2.46		2.90		4.06	ns
t_{CO}	Sequential Clk to Q		1.92		2.18		2.56		3.59	ns
t_{GO}	Latch G to Q		1.86		2.11		2.48		3.47	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		1.92		2.18		2.56		3.59	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		0.98		1.11		1.30		1.82	ns
t_{RD2}	FO=2 Routing Delay		1.35		1.54		1.81		2.53	ns
t_{RD3}	FO=3 Routing Delay		1.73		1.96		2.31		3.23	ns
t_{RD4}	FO=4 Routing Delay		2.11		2.39		2.81		3.94	ns
t_{RD8}	FO=8 Routing Delay		3.62		4.11		4.83		6.76	ns
Sequential Timing Characteristics[3, 4]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.50		0.57		0.67		0.94		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.63		0.71		0.84		1.18		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.27		5.97		7.03		9.84		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.91		7.83		9.21		12.90		ns
t_A	Flip-Flop Clock Input Period	6.30		7.14		8.40		11.76		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.30		0.4		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.30		0.4		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		135		125		108		65	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.63		1.84		2.17		3.04	ns
t_{INYL}	Pad to Y Low			2.01		2.27		2.67		3.74	ns
t_{INGH}	G to Y High			0.76		0.86		1.01		1.41	ns
t_{INGL}	G to Y Low			7.41		8.40		9.88		13.84	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.87		3.25		3.82		5.35	ns
t_{IRD2}	FO=2 Routing Delay			3.28		3.71		4.37		6.12	ns
t_{IRD3}	FO=3 Routing Delay			3.70		4.19		4.93		6.90	ns
t_{IRD4}	FO=4 Routing Delay			4.12		4.66		5.49		7.68	ns
t_{IRD8}	FO=8 Routing Delay			5.78		6.55		7.70		10.78	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 32		3.84		4.36		5.12		7.17	ns
		FO = 256		4.41		5.00		5.88		8.23	ns
t_{CKL}	Input High to Low	FO = 32		3.56		4.03		4.75		6.64	ns
		FO = 256		4.10		4.64		5.46		7.64	ns
t_{PWH}	Minimum Pulse Width High	FO = 32	1.89		2.14		2.52		3.53		ns
		FO = 256	2.05		2.32		2.73		3.82		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32	1.89		2.14		2.52		3.53		ns
		FO = 256	2.05		2.32		2.73		3.82		ns
t_{CKSW}	Maximum Skew	FO = 32		0.47		0.54		0.63		0.88	ns
		FO = 256		0.47		0.54		0.63		0.88	ns
t_{SUEXT}	Input Latch External Setup	FO = 32	0.76		0.86		1.01		1.41		ns
		FO = 256	0.76		0.86		1.01		1.41		ns
t_{HEXT}	Input Latch External Hold	FO = 32	0.00		0.00		0.00		0.00		ns
		FO = 256	0.00		0.00		0.00		0.00		ns
t_P	Minimum Period	FO = 32	5.88		6.66		7.84		10.98		ns
		FO = 256	6.30		7.14		8.40		11.76		ns
f_{MAX}	Maximum Frequency	FO = 32		150		140		120		72	MHz
		FO = 256		135		125		108		65	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.79		4.30		5.05		7.08	ns
t_{DHL}	Data to Pad Low		4.46		5.06		5.95		8.33	ns
t_{ENZH}	Enable Pad Z to High		4.10		4.64		5.46		7.64	ns
t_{ENZL}	Enable Pad Z to Low		4.54		5.14		6.05		8.47	ns
t_{ENHZ}	Enable Pad High to Z		7.61		8.63		10.15		14.21	ns
t_{ENLZ}	Enable Pad Low to Z		8.30		9.40		11.06		15.48	ns
t_{GLH}	G to Pad High		6.45		7.31		8.60		12.03	ns
t_{GHL}	G to Pad Low		6.45		7.31		8.60		12.03	ns
t_{LSU}	I/O Latch Setup	0.76		0.86		1.01		1.41		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.66		10.95		12.88		18.03	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		13.55		15.35		18.06		25.28	ns
d_{TLH}	Capacity Loading, Low to High		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.81		5.45		6.41		8.98	ns
t_{DHL}	Data to Pad Low		3.73		4.22		4.97		6.96	ns
t_{ENZH}	Enable Pad Z to High		4.10		4.64		5.46		7.64	ns
t_{ENZL}	Enable Pad Z to Low		4.54		5.14		6.05		8.47	ns
t_{ENHZ}	Enable Pad High to Z		7.61		8.63		10.15		14.21	ns
t_{ENLZ}	Enable Pad Low to Z		8.30		9.40		11.06		15.48	ns
t_{GLH}	G to Pad High		6.45		7.31		8.60		12.03	ns
t_{GHL}	G to Pad Low		6.45		7.31		8.60		12.03	ns
t_{LSU}	I/O Latch Setup	0.76		0.86		1.01		1.41		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.66		10.95		12.88		18.03	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		13.55		15.35		18.06		25.28	ns
d_{TLH}	Capacity Loading, Low to High		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.0		2.3		2.7		3.8	ns
t_{CO}	Sequential Clk to Q		1.9		2.2		2.6		3.6	ns
t_{GO}	Latch G to Q		2.0		2.3		2.7		3.8	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		1.8		2.0		2.4		3.3	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.0		1.1		1.3		1.8	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{RD3}	FO=3 Routing Delay		1.7		1.9		2.2		3.1	ns
t_{RD4}	FO=4 Routing Delay		2.0		2.2		2.6		3.6	ns
t_{RD8}	FO=8 Routing Delay		3.8		4.3		5.0		7.0	ns
Sequential Timing Characteristics[3,4]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.8		4.3		5.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.9		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period	7.5		8.5		10.0		14.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.5		0.6		0.7		1.0		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.6		0.7		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		216		180		156		94	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.3		1.4		1.7		2.4	ns
t_{INYL}	Pad to Y Low			1.0		1.1		1.3		1.8	ns
t_{INGH}	G to Y High			2.1		2.3		2.7		3.8	ns
t_{INGL}	G to Y Low			2.5		2.8		3.4		4.7	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			3.2		3.7		4.3		6.0	ns
t_{IRD2}	FO=2 Routing Delay			3.7		4.2		4.9		6.9	ns
t_{IRD3}	FO=3 Routing Delay			4.0		4.5		5.3		7.4	ns
t_{IRD4}	FO=4 Routing Delay			4.6		5.2		6.1		8.5	ns
t_{IRD8}	FO=8 Routing Delay			6.6		7.5		8.8		12.3	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 32		2.6		3.0		3.5		4.9	ns
		FO = 384		3.0		3.4		4.0		5.6	ns
t_{CKL}	Input High to Low	FO = 32		2.5		2.8		3.3		4.6	ns
		FO = 384		2.9		3.2		3.8		5.3	ns
t_{PWH}	Minimum Pulse Width High	FO = 32	3.5		4.0		4.7		6.5		ns
		FO = 384	4.1		4.6		5.4		7.6		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.5		4.0		4.7		6.6		ns
		FO = 384	4.1		4.6		5.4		7.6		ns
t_{CKSW}	Maximum Skew	FO = 32		0.4		0.4		0.5		0.7	ns
		FO = 384		1.7		2.0		2.3		3.2	ns
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	4.9		5.5		6.5		9.1		ns
		FO = 384	7.4		8.3		9.8		13.7		ns
t_P	Minimum Period	FO = 32	6.7		7.6		8.9		12.5		ns
		FO = 384	7.4		8.4		9.9		13.9		ns
f_{MAX}	Maximum Frequency	FO = 32		215		200		172		103	MHz
		FO = 384		195		180		156		94	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		2.7		3.1		3.6		5.1	ns
t_{DHL}	Data to Pad Low		3.3		3.7		4.4		6.2	ns
t_{ENZH}	Enable Pad Z to High		3.0		3.4		4.0		5.6	ns
t_{ENZL}	Enable Pad Z to Low		3.3		3.8		4.5		6.2	ns
t_{ENHZ}	Enable Pad High to Z		6.3		7.1		8.4		11.7	ns
t_{ENLZ}	Enable Pad Low to Z		5.8		6.5		7.7		10.8	ns
t_{GLH}	G to Pad High		5.9		6.6		7.8		10.9	ns
t_{GHL}	G to Pad Low		6.4		7.3		8.6		12.0	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		6.9		7.8		9.2		12.9	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		9.7		11.0		12.9		18.1	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.04		0.05		0.07	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.1		3.5		4.2		5.8	ns
t_{DHL}	Data to Pad Low		3.8		4.3		5.1		7.1	ns
t_{ENZH}	Enable Pad Z to High		4.0		4.5		5.3		7.5	ns
t_{ENZL}	Enable Pad Z to Low		4.3		4.9		5.8		8.1	ns
t_{ENHZ}	Enable Pad High to Z		7.0		7.9		9.3		13.0	ns
t_{ENLZ}	Enable Pad Low to Z		6.9		7.9		9.2		12.9	ns
t_{GLH}	G to Pad High		6.9		7.9		9.3		13.0	ns
t_{GHL}	G to Pad Low		7.5		8.5		10.0		14.0	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		6.9		7.8		9.2		12.9	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		9.7		11.0		12.9		18.1	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the “Simultaneously Switching Output Limits for Actel FPGAs” application note.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.8		3.2		3.8		5.3	ns
t_{CO}	Sequential Clk to Q		2.7		3.1		3.6		5.0	ns
t_{GO}	Latch G to Q		2.8		3.2		3.8		5.3	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.5		2.8		3.3		4.7	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1		2.5		3.5	ns
t_{RD3}	FO=3 Routing Delay		2.3		2.6		3.1		4.3	ns
t_{RD4}	FO=4 Routing Delay		2.7		3.1		3.6		5.1	ns
t_{RD8}	FO=8 Routing Delay		5.3		6.0		7.0		9.8	ns
Sequential Timing Characteristics[3,4]										
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.3		6.0		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.9		7.8		9.2		12.9		ns
t_A	Flip-Flop Clock Input Period	10.5		11.9		14.0		19.6		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.8		0.9		1.0		1.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.8		0.9		1.0		1.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		130		108		94		57	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.8		2.0		2.4		3.3	ns
t_{INYL}	Pad to Y Low			1.4		1.5		1.8		2.5	ns
t_{INGH}	G to Y High			2.9		3.3		3.8		5.4	ns
t_{INGL}	G to Y Low			3.5		4.0		4.7		6.6	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			4.5		5.1		6.0		8.4	ns
t_{IRD2}	FO=2 Routing Delay			5.1		5.8		6.9		9.6	ns
t_{IRD3}	FO=3 Routing Delay			5.6		6.3		7.4		10.4	ns
t_{IRD4}	FO=4 Routing Delay			6.4		7.3		8.5		12.0	ns
t_{IRD8}	FO=8 Routing Delay			9.2		10.5		12.3		17.2	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO = 32		3.7		4.2		4.9		6.9	ns
		FO = 384		4.2		4.8		5.6		7.9	ns
t_{CKL}	Input High to Low	FO = 32		3.5		3.9		4.6		6.5	ns
		FO = 384		4.0		4.5		5.3		7.4	ns
t_{PWH}	Minimum Pulse Width High	FO = 32	4.9		5.5		6.5		9.1		ns
		FO = 384	5.7		6.4		7.6		10.6		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32	4.9		5.6		6.6		9.2		ns
		FO = 384	5.7		6.4		7.6		10.6		ns
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.6		0.7		0.9	ns
		FO = 384		2.4		2.8		3.2		4.5	ns
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	6.8		7.7		9.1		12.7		ns
		FO = 384	10.3		11.7		13.7		19.2		ns
t_P	Minimum Period	FO = 32	9.3		10.6		12.5		17.4		ns
		FO = 384	10.4		11.8		13.9		19.4		ns
f_{MAX}	Maximum Frequency	FO = 32		144		120		104		62	MHz
		FO = 384		130		108		94		57	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.8		4.3		5.1		7.1	ns
t_{DHL}	Data to Pad Low		4.6		5.2		6.2		8.6	ns
t_{ENZH}	Enable Pad Z to High		4.2		4.8		5.6		7.9	ns
t_{ENZL}	Enable Pad Z to Low		4.7		5.3		6.2		8.7	ns
t_{ENHZ}	Enable Pad High to Z		8.8		10.0		11.7		16.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.1		9.1		10.8		15.1	ns
t_{GLH}	G to Pad High		8.2		9.3		10.9		15.3	ns
t_{GHL}	G to Pad Low		9.0		10.2		12.0		16.8	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.4		4.9		5.8		8.1	ns
t_{DHL}	Data to Pad Low		5.3		6.0		7.1		9.9	ns
t_{ENZH}	Enable Pad Z to High		5.6		6.4		7.5		10.5	ns
t_{ENZL}	Enable Pad Z to Low		6.1		6.9		8.1		11.3	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.1		13.0		18.2	ns
t_{ENLZ}	Enable Pad Low to Z		9.7		11.0		12.9		18.1	ns
t_{GLH}	G to Pad High		9.7		11.0		13.0		18.1	ns
t_{GHL}	G to Pad Low		10.5		11.9		14.0		19.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays[1]		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.55		1.75		2.06		2.88	ns
t_{PDD}	Internal Decode Module Delay		1.64		1.86		2.19		3.07	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.25		1.41		1.66		2.32	ns
t_{RD2}	FO=2 Routing Delay		1.52		1.72		2.02		2.83	ns
t_{RD3}	FO=3 Routing Delay		1.79		2.02		2.38		3.33	ns
t_{RD4}	FO=4 Routing Delay		2.06		2.33		2.74		3.84	ns
t_{RD5}	FO=8 Routing Delay		3.14		3.55		4.18		5.85	ns
Sequential Timing Characteristics[3, 4]										
t_{CO}	Flip-Flop Clock-to-Output		1.36		1.54		1.81		2.53	ns
t_{GO}	Latch Gate-to-Output		1.32		1.50		1.76		2.46	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.35		0.40		0.47		0.66		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		1.36		1.54		1.81		2.53	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.45		0.51		0.60		0.84		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.70		4.19		4.93		6.90		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.85		5.49		6.46		9.04		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.16		1.31		1.54		2.16	ns
t_{INGO}	Input Latch Gate-to-Output			1.43		1.62		1.91		2.67	ns
t_{INH}	Input Latch Hold		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Setup		0.53		0.60		0.70		0.98		ns
t_{ILA}	Latch Active Pulse Width		5.20		5.89		6.93		9.70		ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.64		2.99		3.52		4.93	ns
t_{IRD2}	FO=2 Routing Delay			2.94		3.33		3.92		5.49	ns
t_{IRD3}	FO=3 Routing Delay			3.23		3.66		4.31		6.03	ns
t_{IRD4}	FO=4 Routing Delay			3.53		4.00		4.71		6.59	ns
t_{IRD8}	FO=8 Routing Delay			4.72		5.35		6.29		8.81	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		2.87		3.25		3.82		5.35	ns
		FO=486		3.64		4.12		4.85		6.79	ns
t_{CKL}	Input High to Low	FO=32		2.36		2.67		3.14		4.40	ns
		FO=486		3.08		3.50		4.12		5.77	ns
t_{PWH}	Minimum Pulse Width High	FO=32	2.40		2.72		3.20		4.48		ns
		FO=486	2.63		2.98		3.50		4.90		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	2.40		2.72		3.20		4.48		ns
		FO=486	2.63		2.98		3.50		4.90		ns
t_{CKSW}	Maximum Skew	FO=32		0.60		0.68		0.80		1.12	ns
		FO=486		0.60		0.68		0.80		1.12	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.53		0.60		0.70		0.98		ns
		FO=486	0.53		0.60		0.70		0.98		ns
t_{HEXT}	Input Latch External Hold	FO=32	0.00		0.00		0.00		0.00		ns
		FO=486	0.00		0.00		0.00		0.00		ns
t_P	Minimum Period ($1/f_{max}$)	FO=32	4.88		5.53		6.50		9.10		ns
		FO=486	5.40		6.12		7.20		10.08		ns
f_{MAX}	Maximum Data-Path Frequency	FO=32		191.25		175.95		153.00		91.80	MHz
		FO=486		175.00		161.00		140.00		84.00	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Output Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		2.97		3.37		3.96		5.54	ns
t_{DHL}	Data to Pad Low		3.35		3.80		4.47		6.26	ns
t_{ENZH}	Enable Pad Z to High		2.25		2.55		3.00		4.20	ns
t_{ENZL}	Enable Pad Z to Low		2.68		3.03		3.57		5.00	ns
t_{ENHZ}	Enable Pad High to Z		5.83		6.60		7.77		10.88	ns
t_{ENLZ}	Enable Pad Low to Z		5.39		6.10		7.18		10.05	ns
t_{GLH}	G to Pad High		4.58		5.19		6.10		8.54	ns
t_{GHL}	G to Pad Low		4.58		5.19		6.10		8.54	ns
t_{LSU}	I/O Latch Output Setup	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.33		9.44		11.10		15.54	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.78		13.35		15.70		21.98	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.80		4.31		5.07		7.10	ns
t_{DHL}	Data to Pad Low		2.78		3.15		3.71		5.19	ns
t_{ENZH}	Enable Pad Z to High		2.25		2.55		3.00		4.20	ns
t_{ENZL}	Enable Pad Z to Low		2.68		3.03		3.57		5.00	ns
t_{ENHZ}	Enable Pad High to Z		5.83		6.60		7.77		10.88	ns
t_{ENLZ}	Enable Pad Low to Z		5.39		6.10		7.18		10.05	ns
t_{GLH}	G to Pad High		4.58		5.19		6.10		8.54	ns
t_{GHL}	G to Pad Low		4.58		5.19		6.10		8.54	ns
t_{LSU}	I/O Latch Setup	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.33		9.44		11.10		15.54	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.78		13.35		15.70		21.98	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays[1]		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.16		2.45		2.88		4.04	ns
t_{PDD}	Internal Decode Module Delay		2.30		2.61		3.07		4.29	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.74		1.98		2.32		3.25	ns
t_{RD2}	FO=2 Routing Delay		2.12		2.40		2.83		3.96	ns
t_{RD3}	FO=3 Routing Delay		2.50		2.83		3.33		4.66	ns
t_{RD4}	FO=4 Routing Delay		2.88		3.26		3.84		5.37	ns
t_{RD5}	FO=8 Routing Delay		4.39		4.97		5.85		8.19	ns
Sequential Timing Characteristics[3, 4]										
t_{CO}	Flip-Flop Clock-to-Output		1.90		2.15		2.53		3.55	ns
t_{GO}	Latch Gate-to-Output		1.85		2.09		2.46		3.45	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.49		0.56		0.66		0.92		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		1.90		2.15		2.53		3.55	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.63		0.71		0.84		1.18		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.18		5.87		6.90		9.66		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.78		7.69		9.04		12.66		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.62		1.83		2.16		3.02	ns
t_{INGO}	Input Latch Gate-to-Output			2.01		2.27		2.67		3.74	ns
t_{INH}	Input Latch Hold		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Setup		0.74		0.83		0.98		1.37		ns
t_{ILA}	Latch Active Pulse Width		7.28		8.25		9.70		13.58		ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			3.70		4.19		4.93		6.90	ns
t_{IRD2}	FO=2 Routing Delay			4.12		4.66		5.49		7.68	ns
t_{IRD3}	FO=3 Routing Delay			4.53		5.13		6.03		8.45	ns
t_{IRD4}	FO=4 Routing Delay			4.95		5.60		6.59		9.23	ns
t_{IRD8}	FO=8 Routing Delay			6.60		7.49		8.81		12.33	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		4.01		4.55		5.35		7.49	ns
		FO=486		5.09		5.77		6.79		9.51	ns
t_{CKL}	Input High to Low	FO=32		3.30		3.74		4.40		6.15	ns
		FO=486		4.33		4.90		5.77		8.08	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.36		3.81		4.48		6.27		ns
		FO=486	3.68		4.17		4.90		6.86		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.36		3.81		4.48		6.27		ns
		FO=486	3.68		4.17		4.90		6.86		ns
t_{CKSW}	Maximum Skew	FO=32		0.84		0.95		1.12		1.57	ns
		FO=486		0.84		0.95		1.12		1.57	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.74		0.83		0.98		1.37		ns
		FO=486	0.74		0.83		0.98		1.37		ns
t_{HEXT}	Input Latch External Hold	FO=32	0.00		0.00		0.00		0.00		ns
		FO=486	0.00		0.00		0.00		0.00		ns
t_P	Minimum Period ($1/f_{max}$)	FO=32	6.83		7.74		9.10		12.74		ns
		FO=486	7.56		8.57		10.08		14.11		ns
f_{MAX}	Maximum Data-Path Frequency	FO=32		114.75		105.57		91.80		55.08	MHz
		FO=486		105.00		96.60		84.00		50.40	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Output Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.16		4.71		5.54		7.76	ns
t_{DHL}	Data to Pad Low		4.69		5.32		6.26		8.76	ns
t_{ENZH}	Enable Pad Z to High		3.15		3.57		4.20		5.88	ns
t_{ENZL}	Enable Pad Z to Low		3.75		4.25		5.00		7.00	ns
t_{ENHZ}	Enable Pad High to Z		8.16		9.25		10.88		15.23	ns
t_{ENLZ}	Enable Pad Low to Z		7.54		8.54		10.05		14.07	ns
t_{GLH}	G to Pad High		6.41		7.26		8.54		11.96	ns
t_{GHL}	G to Pad Low		6.41		7.26		8.54		11.96	ns
t_{LSU}	I/O Latch Output Setup	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.66		13.21		15.54		21.76	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.49		18.68		21.98		30.77	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		5.32		6.03		7.10		9.94	ns
t_{DHL}	Data to Pad Low		3.90		4.41		5.19		7.27	ns
t_{ENZH}	Enable Pad Z to High		3.15		3.57		4.20		5.88	ns
t_{ENZL}	Enable Pad Z to Low		3.75		4.25		5.00		7.00	ns
t_{ENHZ}	Enable Pad High to Z		8.16		9.25		10.88		15.23	ns
t_{ENLZ}	Enable Pad Low to Z		7.54		8.54		10.05		14.07	ns
t_{GLH}	G to Pad High		6.41		7.26		8.54		11.96	ns
t_{GHL}	G to Pad Low		6.41		7.26		8.54		11.96	ns
t_{LSU}	I/O Latch Setup	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.66		13.21		15.54		21.76	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.49		18.68		21.98		30.77	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.08	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX36 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.5		1.7		2.0		2.7	ns
t_{PDD}	Internal Decode Module Delay		1.9		2.1		2.5		3.5	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.0		1.1		1.3		1.9	ns
t_{RD2}	FO=2 Routing Delay		1.1		1.3		1.5		2.1	ns
t_{RD3}	FO=3 Routing Delay		1.3		1.5		1.7		2.4	ns
t_{RD4}	FO=4 Routing Delay		1.4		1.6		1.9		2.7	ns
t_{RD5}	FO=8 Routing Delay		2.1		2.3		2.8		3.9	ns
t_{RDD}	Decode-to-Output Routing Delay		0.4		0.4		0.5		0.7	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		1.5		1.7		2.0		2.8	ns
t_{GO}	Latch Gate-to-Output		1.5		1.7		2.0		2.7	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.4		0.4		0.5		0.7		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		1.5		1.7		2.0		2.8	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.8		5.5		6.5		9.0		ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	7.5		8.5		10.0		14.0		ns
t_{WC}	Write Cycle Time	7.5		8.5		10.0		14.0		ns
t_{RCKHL}	Clock High/Low Time	3.8		4.3		5.0		7.0		ns
t_{RCO}	Data Valid After Clock High/Low		3.8		4.3		5.0		7.0	ns
t_{ADSU}	Address/Data Setup Time	1.8		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.7		0.8		0.9		1.3		ns
t_{RENH}	Read Enable Hold	3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Setup	3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.1		3.5		4.1		5.7		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		9.0		10.2		12.0		16.8	ns
t_{RDADV}	Read Address Valid	9.8		11.1		13.0		18.2		ns
t_{ADSU}	Address/Data Setup Time	1.8		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.7		0.8		0.9		1.3		ns
t_{RENHA}	Read Enable Hold	3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Setup	3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.4		1.5		1.8		2.5	ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Advanced Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.3		1.5		1.7		2.4	ns
t_{INGO}	Input Latch Gate-to-Output[1]			1.6		1.8		2.1		3.0	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup[1]		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width[1]		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			3.2		3.7		4.3		6.0	ns
t_{IRD2}	FO=2 Routing Delay			3.7		4.2		4.9		6.9	ns
t_{IRD3}	FO=3 Routing Delay			4.0		4.5		5.3		7.4	ns
t_{IRD4}	FO=4 Routing Delay			4.6		5.2		6.1		8.5	ns
t_{IRD8}	FO=8 Routing Delay			6.6		7.5		8.8		12.3	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		6.7		7.6		8.9		12.5	ns
		FO=635		8.6		9.8		11.5		16.1	ns
t_{CKL}	Input High to Low	FO=32		6.2		7.0		8.2		11.5	ns
		FO=635		8.0		9.1		10.7		15.0	ns
t_{PWH}	Minimum Pulse Width High	FO=32	2.0		2.2		2.6		3.6		ns
		FO=635	2.2		2.5		2.9		4.1		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	2.0		2.2		2.6		3.6		ns
		FO=635	2.2		2.5		2.9		4.1		ns
t_{CKSW}	Maximum Skew	FO=32		0.8		0.9		1.0		1.4	ns
		FO=635		0.8		0.9		1.0		1.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=635	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.6		2.9		3.4		4.8		ns
		FO=635	3.2		3.7		4.3		6.0		ns
t_P	Minimum Period ($1/f_{max}$)	FO=32	6.5		7.4		8.7		12.2		ns
		FO=635	7.2		8.2		9.6		13.4		ns
f_{HMAX}	Maximum Data-Path Frequency	FO=32		164		151		131		79	MHz
		FO=635		152		140		121		73	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.1		3.5		4.2		5.8	ns
t_{DHL}	Data to Pad Low		3.6		4.1		4.8		6.7	ns
t_{ENZH}	Enable Pad Z to High		3.3		3.7		4.4		6.1	ns
t_{ENZL}	Enable Pad Z to Low		3.6		4.0		4.8		6.7	ns
t_{ENHZ}	Enable Pad High to Z		6.6		7.4		8.7		12.2	ns
t_{ENLZ}	Enable Pad Low to Z		6.1		6.9		8.1		11.3	ns
t_{GLH}	G to Pad High		5.1		5.8		6.8		9.6	ns
t_{GHL}	G to Pad Low		5.1		5.8		6.8		9.6	ns
t_{LSU}	I/O Latch Output Setup	0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.8		11.1		13.1		18.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		15.7		18.5		25.9	ns
d_{TLH}	Capacitive Loading, Low to High		0.0		0.0		0.1		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.1		0.1		0.1		0.1	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.4		4.9		5.8		8.1	ns
t_{DHL}	Data to Pad Low		5.3		6.0		7.1		9.9	ns
t_{ENZH}	Enable Pad Z to High		5.6		6.4		7.5		10.5	ns
t_{ENZL}	Enable Pad Z to Low		6.1		6.9		8.1		11.3	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.1		13.0		18.2	ns
t_{ENLZ}	Enable Pad Low to Z		9.8		11.1		13.0		18.2	ns
t_{GLH}	G to Pad High		9.8		11.1		13.0		18.2	ns
t_{GHL}	G to Pad Low		10.5		11.9		14.0		19.6	ns
t_{LSU}	I/O Latch Setup	0.3		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.6		13.2		15.5		21.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.4		18.5		21.8		30.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.1		0.1		0.1		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.0		0.1		0.1		0.1	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.1		2.3		2.7		3.8	ns
t_{PDD}	Internal Decode Module Delay		2.6		2.9		3.5		4.8	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.4		1.6		1.9		2.6	ns
t_{RD2}	FO=2 Routing Delay		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.0		2.4		3.4	ns
t_{RD4}	FO=4 Routing Delay		2.0		2.3		2.7		3.8	ns
t_{RD5}	FO=8 Routing Delay		2.9		3.3		3.9		5.4	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.6		0.7		1.0	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.4		2.8		4.0	ns
t_{GO}	Latch Gate-to-Output		2.1		2.3		2.7		3.8	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		0.7		0.9		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.1		2.4		2.8		4.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.2		5.9		6.9		9.7		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.8		7.7		9.0		12.7		ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	10.5		11.9		14.0		19.6		ns
t_{WC}	Write Cycle Time	10.5		11.9		14.0		19.6		ns
t_{RCKHL}	Clock High/Low Time	5.3		6.0		7.0		9.8		ns
t_{RCO}	Data Valid After Clock High/Low		5.3		6.0		7.0		9.8	ns
t_{ADSU}	Address/Data Setup Time	2.5		2.8		3.4		4.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Setup	12.0		1.1		1.3		1.8		ns
t_{RENH}	Read Enable Hold	5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Setup	4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Setup	4.3		4.9		5.7		8.0		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		12.6		14.3		16.8		23.5	ns
t_{RDADV}	Read Address Valid	13.7		15.5		18.2		25.5		ns
t_{ADSU}	Address/Data Setup Time	2.5		2.8		3.4		9.5		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	1.0		1.1		1.3		1.8		ns
t_{RENHA}	Read Enable Hold	5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Setup	4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		2.0		2.1		2.5		3.5	ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.8		2.1		2.4		3.4	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.2		2.5		3.0		4.2	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup[1]		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width[1]		7.3		8.2		9.7		13.6		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			4.5		5.1		6.0		8.4	ns
t_{IRD2}	FO=2 Routing Delay			5.1		5.8		6.9		9.6	ns
t_{IRD3}	FO=3 Routing Delay			5.6		6.3		7.4		10.4	ns
t_{IRD4}	FO=4 Routing Delay			6.4		7.3		8.5		12.0	ns
t_{IRD8}	FO=8 Routing Delay			9.2		10.5		12.3		17.2	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		9.3		10.6		12.5		17.4	ns
		FO=635		12.1		13.7		16.1		22.5	ns
t_{CKL}	Input High to Low	FO=32		8.6		9.8		11.5		16.1	ns
		FO=635		11.2		12.7		15.0		21.0	ns
t_{PWH}	Minimum Pulse Width High	FO=32	2.7		3.1		3.6		5.1		ns
		FO=635	3.0		3.5		4.1		5.7		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	2.7		3.1		3.6		5.1		ns
		FO=635	3.0		3.5		4.1		5.7		ns
t_{CKSW}	Maximum Skew	FO=32		1.1		1.2		1.4		2.0	ns
		FO=635		1.1		1.2		1.4		2.0	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=635	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.6		4.0		4.8		6.7		ns
		FO=635	4.5		5.1		6.0		8.4		ns
t_P	Minimum Period ($1/f_{max}$)	FO=32	9.1		10.4		12.2		17.1		ns
		FO=635	10.1		11.4		13.4		18.8		ns
f_{HMAX}	Maximum Data-Path Frequency	FO=32		99		91		79		48	MHz
		FO=635		93		84		73		44	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

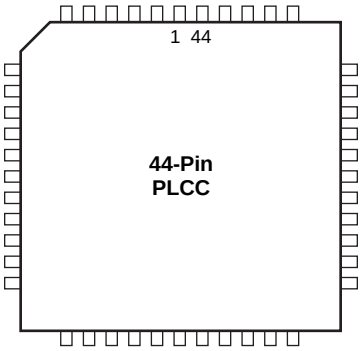
		Preliminary Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.4		5.0		5.8		8.2	ns
t_{DHL}	Data to Pad Low		5.1		5.7		6.7		9.4	ns
t_{ENZH}	Enable Pad Z to High		4.6		5.2		6.1		8.5	ns
t_{ENZL}	Enable Pad Z to Low		5.0		5.7		6.7		9.3	ns
t_{ENHZ}	Enable Pad High to Z		9.2		10.4		12.2		17.1	ns
t_{ENLZ}	Enable Pad Low to Z		8.5		9.6		11.3		15.8	ns
t_{GLH}	G to Pad High		7.2		8.1		9.6		13.4	ns
t_{GHL}	G to Pad Low		7.2		8.1		9.6		13.4	ns
t_{LSU}	I/O Latch Output Setup	0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.8		15.6		18.3		25.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.4		22.0		25.9		36.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.1		0.1		0.1		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.1		0.1		0.1		0.1	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		6.1		6.9		8.1		11.4	ns
t_{DHL}	Data to Pad Low		7.5		8.4		9.9		13.9	ns
t_{ENZH}	Enable Pad Z to High		7.9		8.9		10.5		14.7	ns
t_{ENZL}	Enable Pad Z to Low		8.5		9.6		11.3		15.9	ns
t_{ENHZ}	Enable Pad High to Z		13.7		15.5		18.2		25.5	ns
t_{ENLZ}	Enable Pad Low to Z		13.7		15.5		18.2		25.5	ns
t_{GLH}	G to Pad High		13.7		15.5		18.2		25.5	ns
t_{GHL}	G to Pad Low		14.7		16.7		19.6		27.4	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		0.6		0.8		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		18.4		21.7		30.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		22.9		25.9		30.5		42.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.1		0.1		0.1		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.1		0.1		0.1		0.1	ns/pF

Notes:

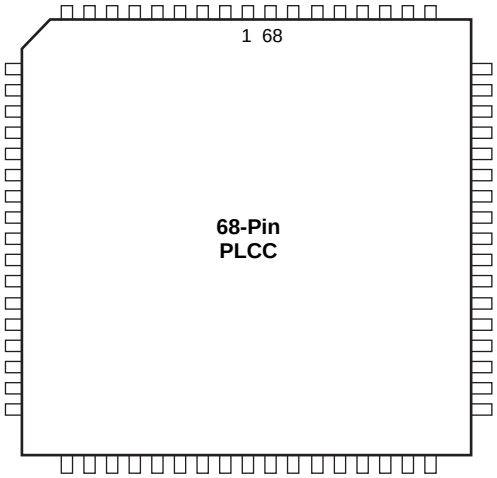
1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

Package Pin Assignments

44-Pin PLCC



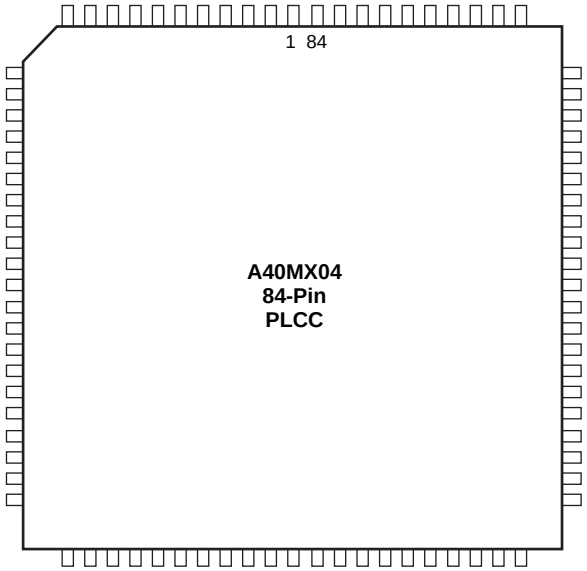
68-Pin PLCC



Signal	A40MX02 Function	A40MX04 Function	Signal	A40MX02 Function	A40MX04 Functions
3	VCC	VCC	4	VCC	VCC
10	GND	GND	14	GND	GND
14	VCC	VCC	15	GND	GND
16	VCC	VCC	21	VCC	VCC
21	GND	GND	25	VCC	VCC
25	VCC	VCC	32	GND	GND
32	GND	GND	38	VCC	VCC
33	CLK, I/O	CLK, I/O	49	GND	GND
34	MODE	MODE	52	CLK, I/O	CLK, I/O
35	VCC	VCC	54	MODE	MODE
36	SDI, I/O	SDI, I/O	55	VCC	VCC
37	DCLK, I/O	DCLK, I/O	56	SDI, I/O	SDI, I/O
38	PRA, I/O	PRA, I/O	57	DCLK, I/O	DCLK, I/O
39	PRB, I/O	PRB, I/O	58	PRA, I/O	PRA, I/O
43	GND	GND	59	PRB, I/O	PRB, I/O

Package Pin Assignments (continued)

84-Pin PLCC



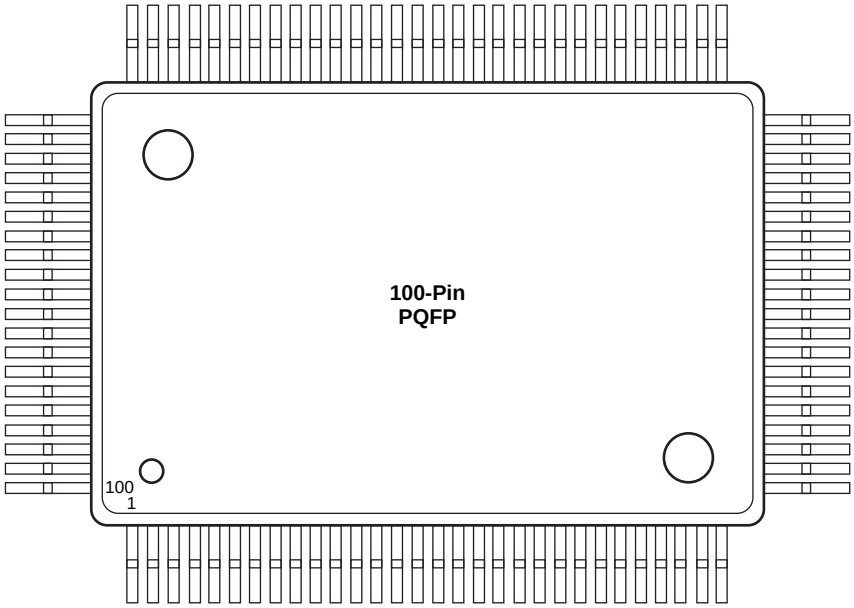
Signal	A40MX04 Function
4	VCC
12	NC
18	GND
19	GND
25	VCC
26	VCC
33	VCC
40	GND
46	VCC
60	GND
61	GND
64	CLK, I/O
66	MODE
67	VCC
68	VCC
72	SDI, I/O
73	DCLK, I/O
74	PRA, I/O
75	PRB, I/O
82	GND

Notes:

1. *NC: Denotes No Connection.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP



Pin	A40MX02 Function	A40MX04 Function
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
6	PRB, I/O	PRB, I/O
13	GND	GND
19	VCC	VCC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	I/O
32	NC	I/O
33	NC	I/O
36	GND	GND
37	GND	GND
43	VCC	VCC
44	VCC	VCC
48	NC	I/O
49	NC	I/O
50	NC	I/O
51	NC	NC
52	NC	NC

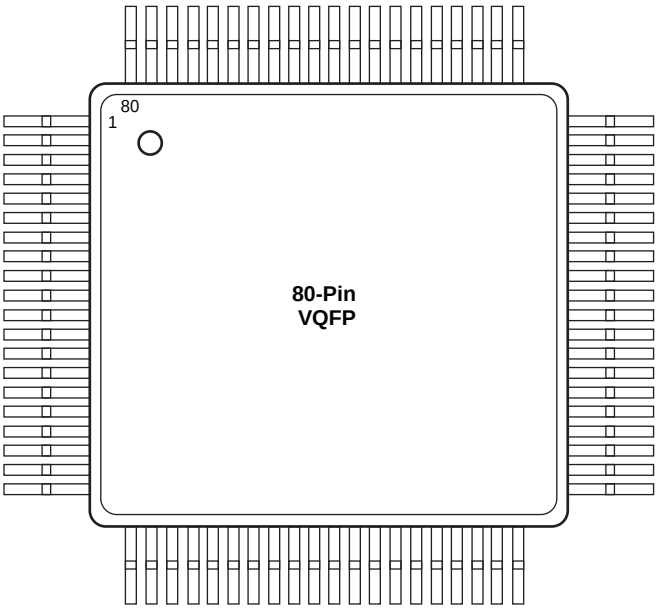
Pin	A40MX02 Function	A40MX04 Function
53	NC	NC
54	NC	NC
55	NC	NC
56	VCC	VCC
63	GND	GND
69	VCC	VCC
77	NC	NC
78	NC	NC
79	NC	NC
80	NC	I/O
81	NC	I/O
82	NC	I/O
86	GND	GND
87	GND	GND
90	CLK, I/O	CLK, I/O
92	MODE	MODE
93	VCC	VCC
94	VCC	VCC
95	NC	I/O
96	NC	I/O
97	NC	I/O
98	SDI, I/O	SDI, I/O
99	DCLK, I/O	DCLK, I/O
100	PRA, I/O	PRA, I/O

Notes:

1. *NC: Denotes No Connection.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

80-Pin VQFP



Pin	A40MX02 Function	A40MX04 Function
2	NC	I/O
3	NC	I/O
4	NC	I/O
7	GND	GND
13	VCC	VCC
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
27	GND	GND
33	VCC	VCC
41	NC	I/O
42	NC	I/O
43	NC	I/O

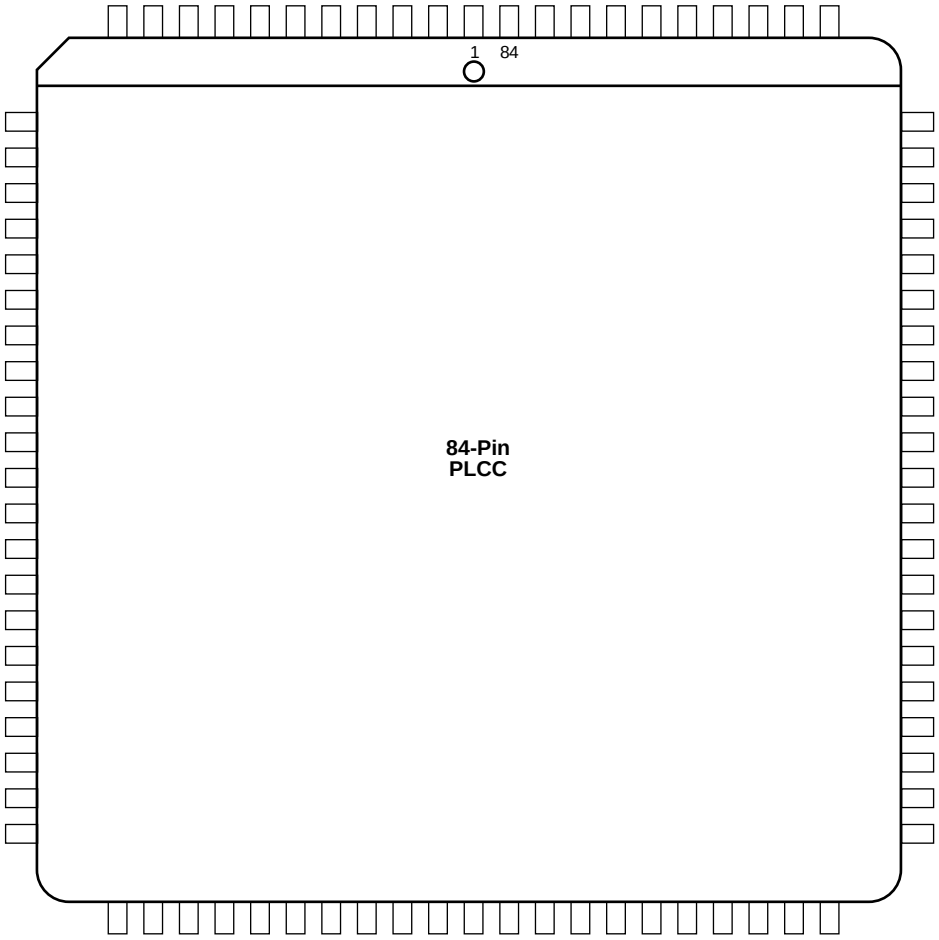
Pin	A40MX02 Function	A40MX04 Function
47	GND	GND
50	CLK, I/O	CLK, I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
68	GND	GND
74	VCC	VCC

Notes:

1. *NC: Denotes No Connection.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin PLCC Package (Top View)



84-Pin PLCC Package

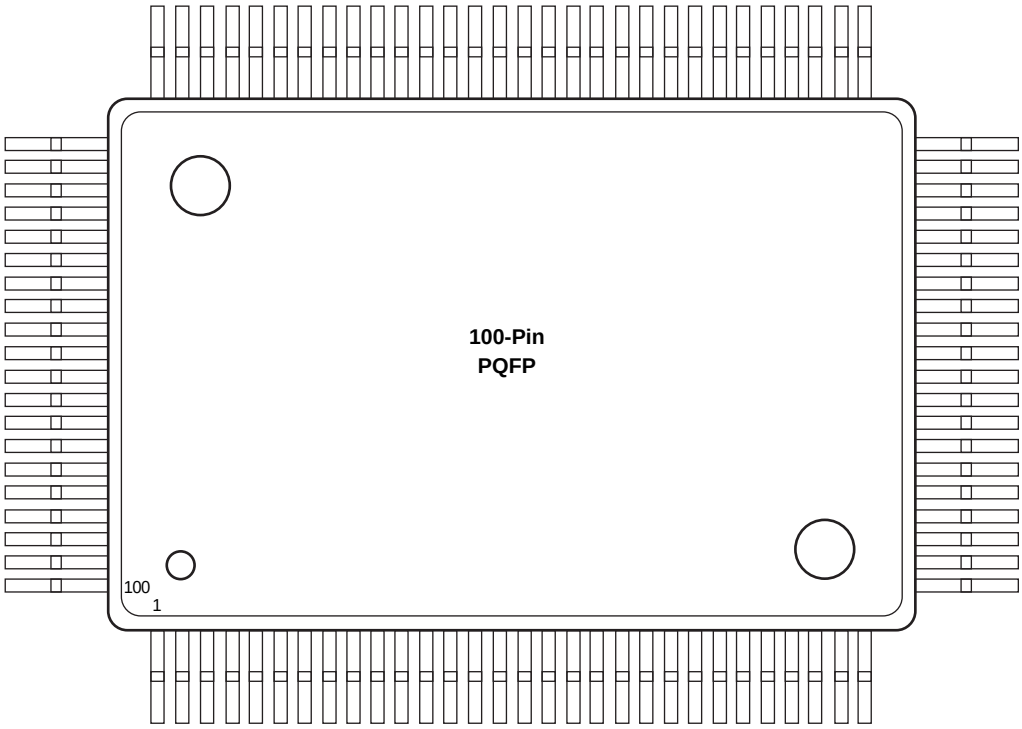
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
2	CLKB,I/O	CLKB,I/O	CLKB,I/O
4	PRB,I/O	PRB,I/O	PRB,I/O
5	I/O	I/O	I/O (WD)
6	GND	GND	GND
8	I/O	I/O	I/O (WD)
9	I/O	I/O	I/O (WD)
10	DCLK,I/O	DCLK,I/O	DCLK,I/O
12	MODE	MODE	MODE
22	VCCI	VCCI	VCCI
23	VCCA	VCCA	VCCA
28	GND	GND	GND
34	I/O	I/O	TMS, I/O
35	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O (WD)
38	I/O	I/O	I/O (WD)
39	I/O	I/O	I/O (WD)
43	VCCA	VCCA	VCCA
44	I/O	I/O	I/O (WD)
45	I/O	I/O	I/O (WD)
46	I/O	I/O	I/O (WD)
47	I/O	I/O	I/O (WD)
49	GND	GND	GND
50	I/O	I/O	I/O (WD)
51	I/O	I/O	I/O (WD)
52	I/O	I/O	TDO (WD)
62	I/O	I/O	TCK, I/O
63	GND	GND	GND
64	VCCA	VCCA	VCCA
65	VCCI	VCCI	VCCI
70	GND	GND	GND
76	SDI,I/O	SDI,I/O	SDI,I/O
78	I/O	I/O	I/O (WD)
79	I/O	I/O	I/O (WD)
80	I/O	I/O	I/O (WD)
81	PRA,I/O	PRA,I/O	PRA,I/O
83	CLKA,I/O	CLKA,I/O	CLKA,I/O
84	VCCA	VCCA	VCCA

Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes No Connection.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-pin PQFP Package (Top View)



100-pin PQFP Package

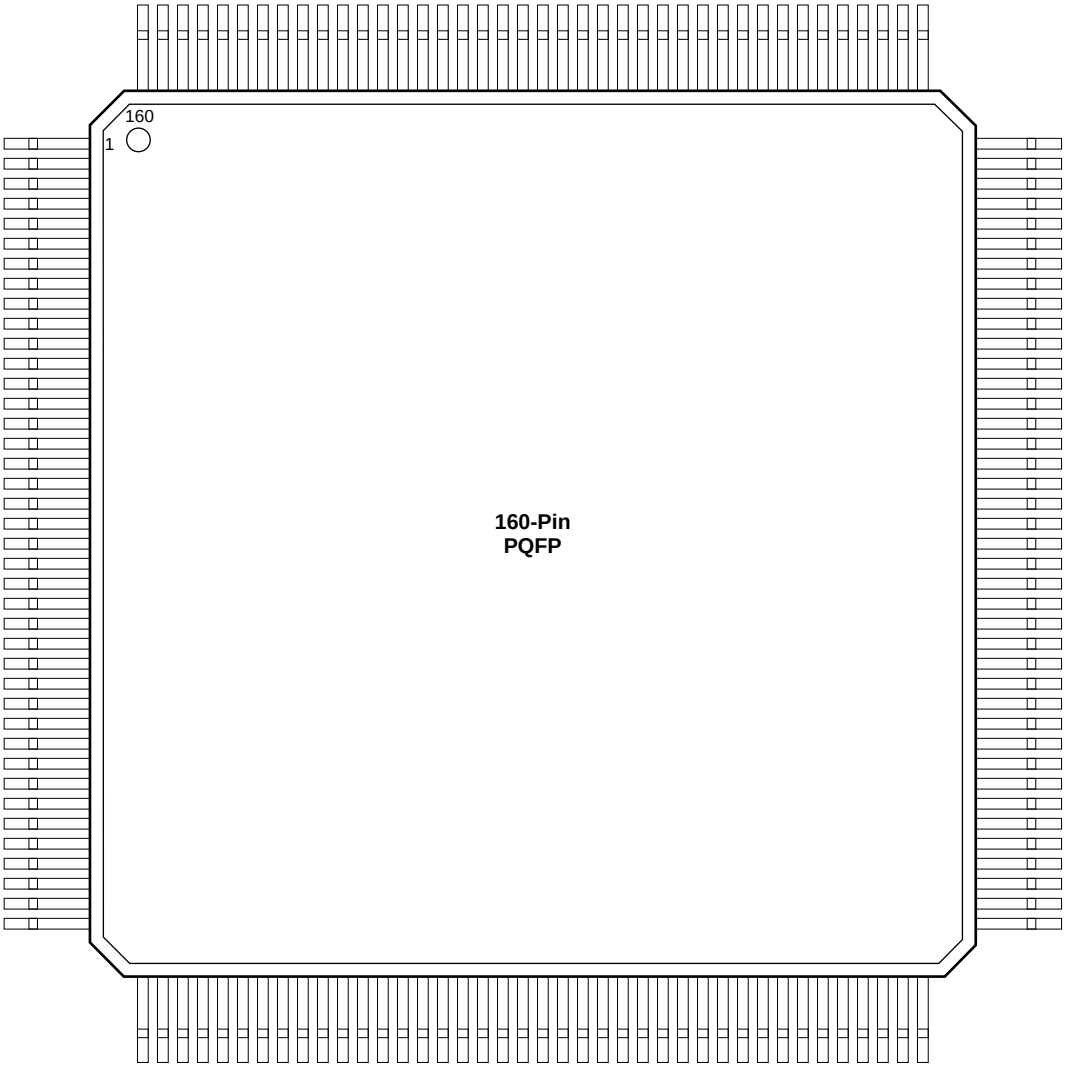
Pin Number	A42MX09 PQ100 Function	A42MX16 PQ100 Function
2	DCLK, I/O	DCLK, I/O
4	MODE	MODE
7	I/O	I/O
9	GND	GND
14	I/O	I/O
15	I/O	I/O
16	VCCA	VCCA
17	VCC	VCC
20	I/O	I/O
22	GND	GND
32	I/O	I/O
34	GND	GND
38	I/O	I/O
40	VCCA	VCCA
44	I/O	I/O
46	GND	GND
55	I/O	I/O
57	GND	GND
62	I/O	I/O
63	I/O	I/O
64	GND	GND
65	VCCA	VCCA
66	VCCI	VCCI
67	VCCA	VCCA
70	I/O	I/O
72	GND	GND
77	I/O	I/O
79	SDI, I/O	SDI, I/O
82	I/O	I/O
84	GND	GND
85	I/O	I/O
87	PRA, I/O	PRA, I/O
88	I/O	I/O
89	CLKA, I/O	CLKA, I/O
90	VCCA	VCCA
92	CLKB, I/O	CLKB, I/O
94	PRB, I/O	PRB, I/O
96	GND	GND
100	I/O	I/O

Notes:

1. *NC: Denotes No Connection.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

160-pin PQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes No Connection.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

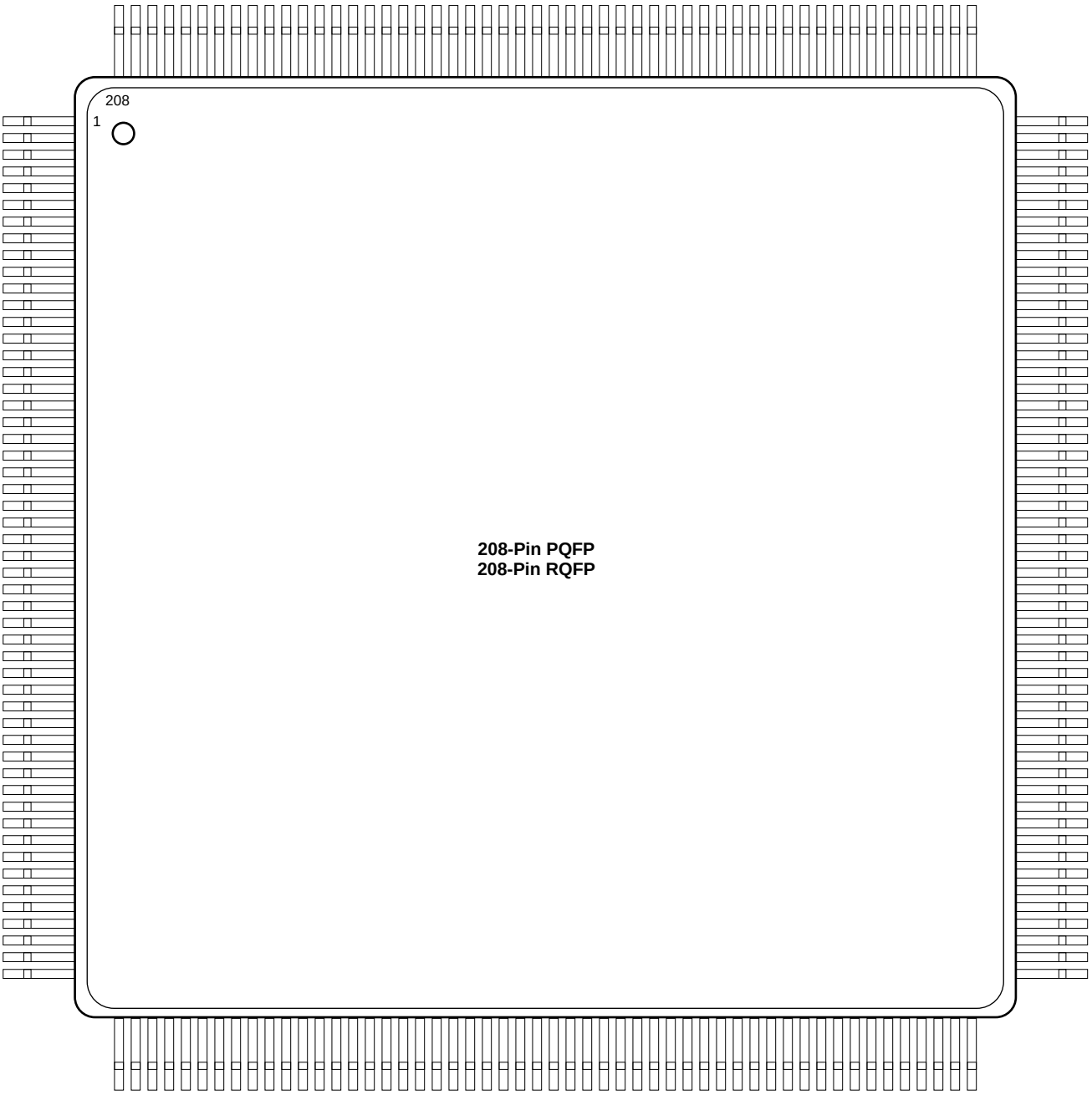
160-Pin PQFP Package

Pin Number	A42MX16 Function	A42MX24 Function
2	DCLK,I/O	DCLK,I/O
4	I/O	I/O (WD)
5	I/O	I/O (WD)
6	VCCI	VCCI
7	I/O	I/O
11	GND	GND
13	I/O	I/O (WD)
14	I/O	I/O (WD)
16	PRB,I/O	PRB,I/O
18	CLKB,I/O	CLKB,I/O
20	VCCA	VCCA
21	CLKA,I/O	CLKA,I/O
23	PRA,I/O	PRA,I/O
24	I/O	I/O (WD)
25	I/O	I/O (WD)
26	I/O	I/O
29	I/O	I/O (WD)
30	GND	GND
31	I/O	I/O (WD)
34	I/O	I/O
35	VCCI	VCCI
36	I/O	I/O (WD)
37	I/O	I/O (WD)
38	SDI,I/O	SDI,I/O
40	GND	GND
44	GND	GND
49	GND	GND
54	VCCA	VCCA
57	VCCA	VCCA
58	VCCI	VCCI
59	GND	GND
60	VCCA	VCCA
61	GND	GND
62	I/O	TCK, I/O
64	GND	GND
69	GND	GND

Pin Number	A42MX16 Function	A42MX24 Function
80	GND	GND
82	I/O	TDO, I/O
83	I/O	I/O (WD)
84	I/O	I/O (WD)
86	VCCI	VCCI
87	I/O	I/O
88	I/O	I/O (WD)
89	GND	GND
92	I/O	I/O
93	I/O	I/O
96	I/O	I/O (WD)
97	I/O	I/O
98	VCCA	VCCA
99	GND	GND
106	I/O	I/O (WD)
107	I/O	I/O (WD)
109	GND	GND
111	I/O	I/O (WD)
112	I/O	I/O (WD)
114	VCCI	VCCI
115	I/O	I/O (WD)
116	I/O	I/O (WD)
118	I/O	TDI, I/O
119	I/O	TMS, I/O
120	GND	GND
125	GND	GND
130	GND	GND
135	VCCA	VCCA
138	VCCA	VCCA
139	VCCI	VCCI
140	GND	GND
145	GND	GND
150	VCCA	VCCA
155	GND	GND
159	MODE	MODE
160	GND	GND

Package Pin Assignments (continued)

208-Pin PQFP Package, 208-pin RQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes No Connection.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heat sink on the top surface.*

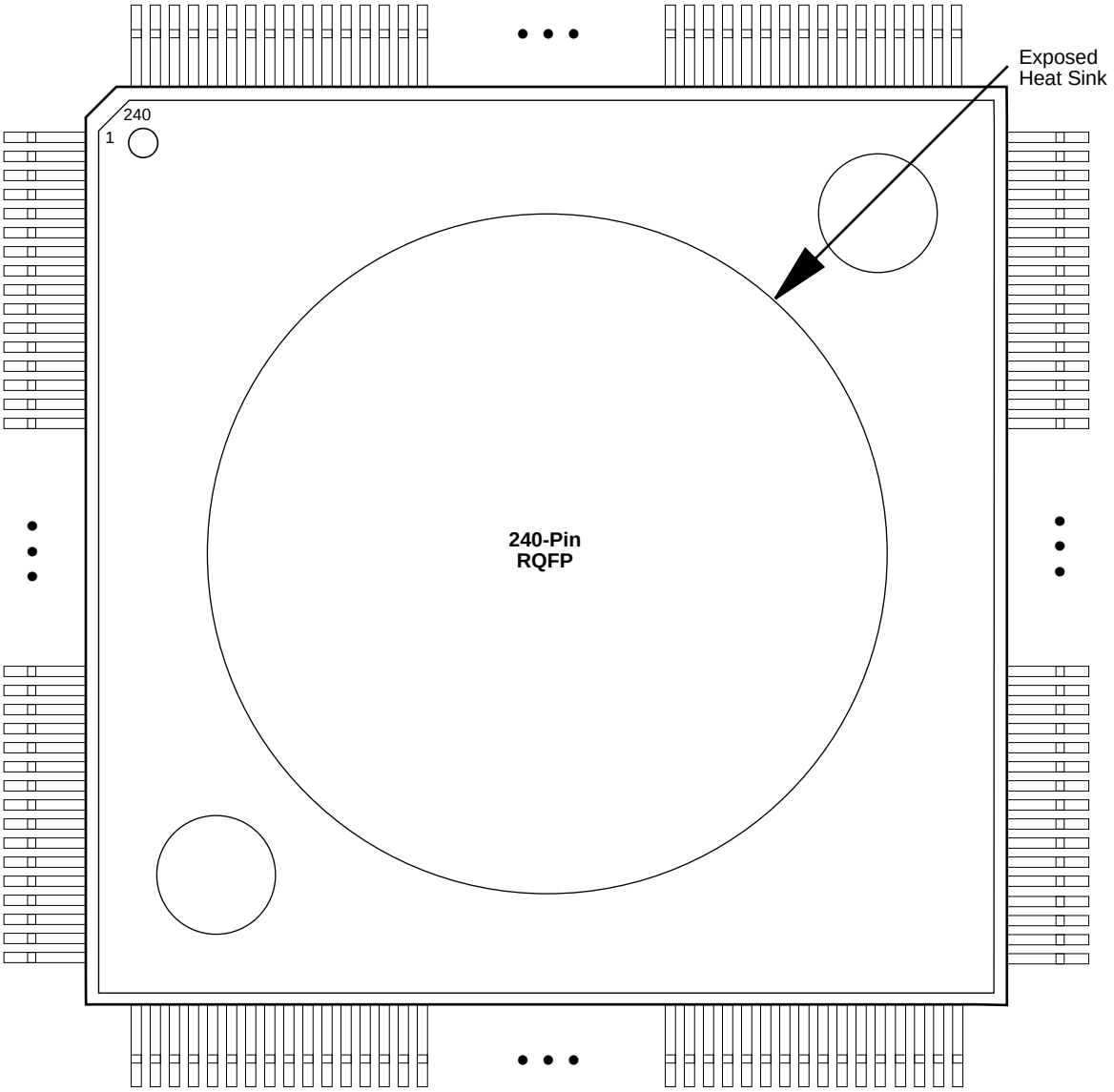
208-Pin PQFP Package, 208-pin RQFP Package

Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 PQ208 Function	42MX36 RQ208 Function
1	GND	GND	GND	I/O
2	NC	VCCA	VCCA	DCLK, I/O
3	MODE	MODE	MODE	I/O
5	I/O	I/O	I/O	I/O (WD)
6	I/O	I/O	I/O	I/O (WD)
7	I/O	I/O	I/O	VCC
9	NC	I/O	I/O	I/O
10	NC	I/O	I/O	I/O
11	NC	I/O	I/O	I/O
13	I/O	I/O	I/O	QCLKC, I/O
15	I/O	I/O	I/O	I/O (WD)
16	NC	I/O	I/O	I/O (WD)
17	VCCA	VCCA	VCCA	I/O
19	I/O	I/O	I/O	I/O (WD)
20	I/O	I/O	I/O	I/O (WD)
22	GND	GND	GND	PRB, I/O
24	I/O	I/O	I/O	CLKB, I/O
26	I/O	I/O	I/O	GND
27	GND	GND	GND	VCCA
28	VCCI	VCCI	VCCI	I/O
29	VCCA	VCCA	VCCA	CLKA, I/O
30	I/O	I/O	I/O	PRA, I/O
32	VCCA	VCCA	VCCA	I/O (WD)
33	I/O	I/O	I/O	I/O (WD)
38	I/O	I/O	I/O	QCLKD, I/O
40	I/O	I/O	I/O	I/O (WD)
41	NC	I/O	I/O	I/O (WD)
42	NC	I/O	I/O	I/O
43	NC	I/O	I/O	I/O
45	I/O	I/O	I/O	VCCI
47	I/O	I/O	I/O	I/O (WD)
48	I/O	I/O	I/O	I/O (WD)
50	NC	I/O	I/O	SDI, I/O
51	NC	I/O	I/O	I/O
52	GND	GND	GND	GND
53	GND	GND	GND	I/O
54	I/O	TMS, I/O	TMS, I/O	I/O
55	I/O	TDI, I/O	TDI, I/O	I/O
57	I/O	I/O (WD)	I/O (WD)	I/O
58	I/O	I/O (WD)	I/O (WD)	I/O
59	I/O	I/O	I/O	GND
60	VCCI	VCCI	VCCI	I/O
61	NC	I/O	I/O	I/O
62	NC	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O	I/O
66	I/O	I/O (WD)	I/O (WD)	I/O
67	NC	I/O (WD)	I/O (WD)	I/O
68	NC	I/O	I/O	I/O
70	I/O	I/O (WD)	I/O (WD)	I/O
71	I/O	I/O (WD)	I/O (WD)	I/O
74	I/O	I/O	I/O	VCCA
77	I/O	I/O	I/O	VCCA
78	GND	GND	GND	VCCI
79	VCCA	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI	GND
81	I/O	I/O	I/O	TCK, I/O
83	I/O	I/O	I/O	GND
85	I/O	I/O (WD)	I/O (WD)	I/O
86	I/O	I/O (WD)	I/O (WD)	I/O
89	NC	I/O	I/O	I/O
90	NC	I/O	I/O	I/O
91	I/O	I/O	QCLKB, I/O	I/O
93	I/O	I/O (WD)	I/O (WD)	I/O
94	I/O	I/O (WD)	I/O (WD)	I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	VCCI	VCCI	VCCI	I/O
100	I/O	I/O (WD)	I/O (WD)	I/O
101	I/O	I/O (WD)	I/O (WD)	I/O
103	I/O	TDO, I/O	TDO, I/O	VCCA

Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 PQ208 Function	42MX36 RQ208 Function
104	I/O	I/O	I/O	GND
105	GND	GND	GND	I/O
106	NC	VCC	VCC	TDO, I/O
107	I/O	I/O	I/O	I/O (WD)
108	I/O	I/O	I/O	I/O (WD)
110	I/O	I/O	I/O	VCC
112	NC	I/O	I/O	I/O
113	NC	I/O	I/O	I/O
114	NC	I/O	I/O	I/O (WD)
115	NC	I/O	I/O	I/O (WD)
117	I/O	I/O	I/O	QCLKB, I/O
121	I/O	I/O	I/O	I/O (WD)
122	I/O	I/O	I/O	I/O (WD)
126	GND	GND	GND	I/O
128	I/O	TCK, I/O	TCK, I/O	I/O
129	GND	GND	GND	VCCA
130	VCCA	VCCA	VCCA	GND
131	GND	GND	GND	I/O
132	VCCI	VCCI	VCCI	I/O
133	VCCA	VCCA	VCCA	I/O
136	VCCA	VCCA	VCCA	I/O
137	I/O	I/O	I/O	I/O (WD)
138	I/O	I/O	I/O	I/O (WD)
141	NC	I/O	I/O	I/O (WD)
142	I/O	I/O	I/O	I/O (WD)
144	I/O	I/O	I/O	QCLKA, I/O
146	NC	I/O	I/O	I/O
147	NC	I/O	I/O	I/O
148	NC	I/O	I/O	I/O
149	NC	I/O	I/O	VCCI
150	GND	GND	GND	I/O
151	I/O	I/O	I/O	I/O (WD)
152	I/O	I/O	I/O	I/O (WD)
154	I/O	I/O	I/O	TDI, I/O
155	I/O	I/O	I/O	TMS, I/O
156	I/O	I/O	I/O	GND
157	GND	GND	GND	VCCA
159	SDI,I/O	SDI,I/O	SDI,I/O	I/O
161	I/O	I/O (WD)	I/O (WD)	I/O
162	I/O	I/O (WD)	I/O (WD)	I/O
164	VCCI	VCCI	VCCI	I/O
165	NC	I/O	I/O	I/O
166	NC	I/O	I/O	I/O
168	I/O	I/O (WD)	I/O (WD)	I/O
169	I/O	I/O (WD)	I/O (WD)	I/O
171	NC	I/O	QCLKD, I/O	I/O
176	I/O	I/O (WD)	I/O (WD)	I/O
177	I/O	I/O (WD)	I/O (WD)	I/O
178	PRA,I/O	PRA,I/O	PRA,I/O	VCCA
180	CLKA,I/O	CLKA,I/O	CLKA,I/O	I/O
181	NC	I/O	I/O	VCCA
182	NC	VCCI	VCCI	VCCI
183	VCCA	VCCA	VCCA	I/O
184	GND	GND	GND	I/O
186	CLKB,I/O	CLKB,I/O	CLKB,I/O	I/O
187	I/O	I/O	I/O	GND
188	PRB,I/O	PRB,I/O	PRB,I/O	I/O
190	I/O	I/O (WD)	I/O (WD)	I/O
191	I/O	I/O (WD)	I/O (WD)	I/O
193	NC	I/O	I/O	I/O
194	NC	I/O (WD)	I/O (WD)	I/O
195	NC	I/O (WD)	I/O (WD)	I/O
196	I/O	I/O	QCLKC, I/O	I/O
197	NC	I/O	I/O	I/O
201	NC	I/O	I/O	I/O
202	VCCI	VCCI	VCCI	I/O
203	I/O	I/O (WD)	I/O (WD)	I/O
204	I/O	I/O (WD)	I/O (WD)	I/O
206	I/O	I/O	I/O	MODE
207	DCLK,I/O	DCLK,I/O	DCLK,I/O	VCCA
208	I/O	I/O	I/O	GND

Package Pin Assignments (continued)

240-Pin RQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes No Connection.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heat sink on the top surface.*

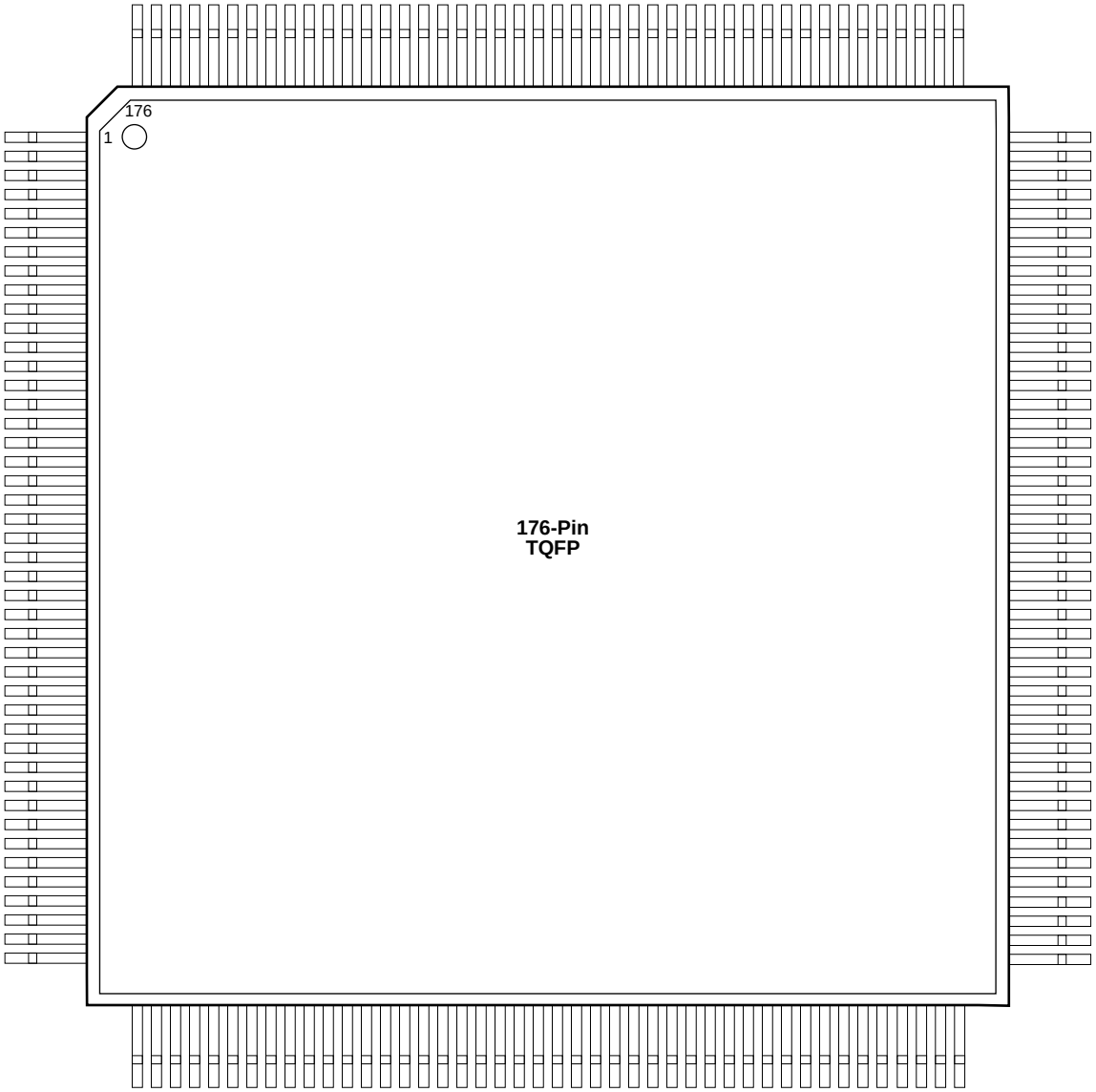
240-Pin RQFP Package

Pin Number	A42MX36 Function
2	DCLK, I/O
6	I/O (WD)
7	I/O (WD)
8	VCCI
15	QCLKC, I/O
17	I/O (WD)
18	I/O (WD)
21	I/O (WD)
22	I/O (WD)
24	PRB, I/O
26	CLKB, I/O
28	GND
29	VCCA
30	VCCI
32	CLKA, I/O
34	PRA, I/O
37	I/O (WD)
38	I/O (WD)
45	QCLKD, I/O
47	I/O (WD)
48	I/O (WD)
52	VCCI
54	I/O (WD)
55	I/O (WD)
57	SDI, I/O
59	VCCA
60	GND
61	GND
71	VCCI
85	VCCA
88	VCCA
89	VCCI
90	VCCA
91	GND
92	TCK, I/O
94	GND
108	VCCI
118	VCCA

Pin Number	A42MX36 Function
119	GND
120	GND
121	GND
123	TDO, I/O
125	I/O (WD)
126	I/O (WD)
128	VCCI
132	I/O (WD)
133	I/O (WD)
135	QCLKB, I/O
142	I/O (WD)
143	I/O (WD)
150	VCCI
151	VCCA
152	GND
159	I/O (WD)
160	I/O (WD)
163	I/O (WD)
164	I/O (WD)
166	QCLKA, I/O
172	VCCI
174	I/O (WD)
175	I/O (WD)
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCC
182	GND
192	VCCI
206	VCCA
209	VCCA
210	VCCI
219	VCCA
227	VCCI
237	GND
238	MODE
239	VCCA
240	GND

Package Pin Assignments (continued)

176-Pin TQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes No Connection.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

176-pin TQFP Package

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
8	NC	NC	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
13	NC	VCCA	VCCA
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	VCCI	VCCI
25	VCCA	VCCA	VCCA
26	NC	I/O	I/O
27	NC	I/O	I/O
28	VCCA	VCCA	VCCA
29	NC	I/O	I/O
33	NC	NC	I/O
37	NC	I/O	I/O
38	NC	NC	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O (WD)
50	I/O	I/O	I/O (WD)
52	NC	VCCI	VCCI
54	NC	I/O	I/O
55	NC	I/O	I/O (WD)
56	I/O	I/O	I/O (WD)
57	NC	NC	I/O
59	I/O	I/O	I/O (WD)
60	I/O	I/O	I/O (WD)
61	NC	I/O	I/O
64	NC	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	I/O (WD)
70	I/O	I/O	I/O (WD)
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
77	NC	NC	I/O (WD)
78	NC	I/O	I/O (WD)
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
84	I/O	I/O	I/O (WD)
85	I/O	I/O	I/O (WD)
86	NC	I/O	I/O
87	I/O	I/O	TDO, I/O
89	GND	GND	GND
96	NC	I/O	I/O
97	NC	I/O	I/O
101	NC	NC	I/O
103	NC	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	GND	GND	GND
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCCI	VCCI	VCCI
113	VCCA	VCCA	VCCA
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	VCC	VCC
117	I/O	I/O	I/O
121	NC	NC	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
133	GND	GND	GND
135	SDI,I/O	SDI,I/O	SDI,I/O
136	NC	I/O	I/O
137	I/O	I/O	I/O (WD)
138	I/O	I/O	I/O (WD)
139	I/O	I/O	I/O
140	NC	VCCI	VCCI
141	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	I/O (WD)
145	NC	NC	I/O (WD)
146	I/O	I/O	I/O
147	NC	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O (WD)
151	NC	I/O	I/O (WD)
152	PRA,I/O	PRA,I/O	PRA,I/O
154	CLKA,I/O	CLKA,I/O	CLKA,I/O
155	VCCA	VCCA	VCCA
156	GND	GND	GND
158	CLKB,I/O	CLKB,I/O	CLKB,I/O
160	PRB,I/O	PRB,I/O	PRB,I/O
161	NC	I/O	I/O (WD)
162	I/O	I/O	I/O (WD)
163	I/O	I/O	I/O
165	NC	NC	I/O (WD)
166	NC	I/O	I/O (WD)
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	I/O (WD)
172	I/O	I/O	I/O (WD)
173	NC	I/O	I/O
175	DCLK,I/O	DCLK,I/O	DCLK,I/O