





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

T <sub>J</sub>	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 125°C	Adjustable Down to 0.9 V	QFN (RHF) <sup>(1)(2)</sup>	TPS54377RHF

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The RHF package is available in two different tape and reel quantities. Add an R suffix to the device type (i.e. TPS54377RHFR) for a 3000 piece reel and add a T suffix (TPS54377RHFT) for a 250 piece reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
V <sub>I</sub> Input voltage range	VIN, SS/ENA, SYNC	–0.3 to 7	V
	RT	–0.3 to 6	V
	VSENSE	–0.3 to 4	V
	BOOT	–0.3 to 17	V
V <sub>O</sub> Output voltage range	VBIAS, PWRGD, COMP	–0.3 to 7	V
	PH (steady state)	–0.6 to 10	V
	PH (transient < 20 ns)	–2 to 10	V
I <sub>O</sub> Output current range	PH	Internally Limited	
	COMP, VBIAS	6	mA
Sink current	PH	6	A
	COMP	6	mA
	SS/ENA, PWRGD	10	mA
Voltage differential	AGND to PGND	±0.3	V
Continuous power dissipation		See Power Dissipation Rating Table	
T <sub>J</sub> Operating virtual junction temperature range		–40 to 150	°C
T <sub>stg</sub> Storage temperature		–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V <sub>I</sub> Input voltage range	3		6	V
T <sub>J</sub> Operating junction temperature	–40		125	°C

**PACKAGE DISSIPATION RATINGS<sup>(1) (2)</sup>**

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	THERMAL IMPEDANCE JUNCTION-TO-CASE
24-Pin RHF with solder	19.7°C/W	1.7°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.

(2) Test board conditions:

- 3 inch x 3 inch, 4 layers, thickness: 0.062 inch
- 2 oz. copper traces located on the top of the PCB
- 2 oz. copper ground plane on the bottom of the PCB
- 2 oz. copper ground planes on the 2 internal layers
- 6 thermal vias (see the Recommended land pattern, [Figure 12](#))

**ELECTRICAL CHARACTERISTICS**

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_I = 3\text{ V}$  to  $6\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
VI	Input voltage range, VIN		3		6	V
	Quiescent current	f <sub>s</sub> = 350 kHz, SYNC = 0.8 V, RT open		6.2	9.6	mA
		f <sub>s</sub> = 550 kHz, SYNC ≥ 2.5 V, RT open, phase pin open		8.4	12.8	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDERVOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3	V
	Stop threshold voltage, UVLO		2.7	2.8		
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO <sup>(1)</sup>			2.5		μs
BIAS VOLTAGE						
VO	Output voltage, VBIAS	I(VBIAS) = 0	2.7	2.8	2.9	V
	Output current, VBIAS <sup>(2)</sup>				100	μA
CUMULATIVE REFERENCE						
Vref	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation <sup>(1) (3)</sup>	IL = 1.5 A, fs = 1.1 MHz, TJ = 25°C		0.04		%/V
	Load regulation <sup>(1) (3)</sup>	IL = 0 A to 3 A, fs = 1.1 MHz, TJ = 25°C		0.09		%/A
OSCILLATOR						
	Internally set free-running frequency range	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set free-running frequency range	RT = 100 kΩ (1% resistor to AGND)	460	500	540	kHz
		RT = 43 kΩ (1% resistor to AGND)	995	1075	1155	
	High-level threshold voltage, SYNC		2.5			V
	Low-level threshold voltage, SYNC				0.8	V
	Pulse duration, SYNC <sup>(1)</sup>		50			ns
	Frequency range, SYNC		330		1600	kHz
	Ramp valley <sup>(1)</sup>			0.75		V
	Ramp amplitude (peak-to-peak) <sup>(1)</sup>			1		V
	Minimum controllable on time				150	ns
	Maximum duty cycle		90%			

(1) Specified by design

(2) Static resistive loads only

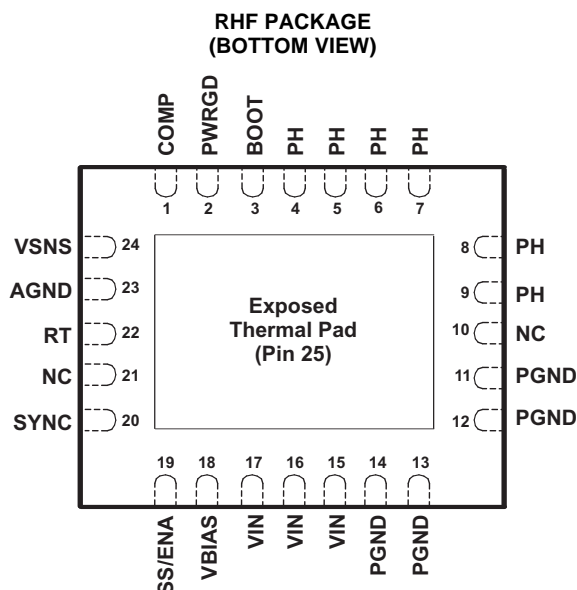
(3) Specified by the circuit used in [Figure 10](#).

**ELECTRICAL CHARACTERISTICS (continued)**T<sub>J</sub> = –40°C to 125°C, V<sub>I</sub> = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ERROR AMPLIFIER</b>						
Error amplifier open loop voltage gain		1 kΩ COMP to AGND <sup>(4)</sup>	90	110		dB
Error amplifier unity gain bandwidth		Parallel 10 kΩ, 160 pF COMP to AGND <sup>(4)</sup>	3	5		MHz
Error amplifier common-mode input voltage range		Powered by internal LDO <sup>(4)</sup>	0	VBIAS		V
I <sub>IB</sub>	Input bias current, VSENSE	VSENSE = V <sub>ref</sub>		60	250	nA
V <sub>O</sub>	Output voltage slew rate (symmetric), COMP		1	1.4		V/μs
<b>PWM COMPARATOR</b>						
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)		10 mV overdrive <sup>(4)</sup>		70	85	ns
<b>SLOW-START/ENABLE</b>						
Enable threshold voltage, SS/ENA			0.82	1.2	1.4	V
Enable hysteresis voltage, SS/ENA <sup>(4)</sup>				0.03		V
Falling edge deglitch, SS/ENA <sup>(4)</sup>				2.5		μs
Internal slow-start time			2.6	3.35	4.1	ms
Charge current, SS/ENA		SS/ENA = 0 V	3	5	8	μA
Discharge current, SS/ENA		SS/ENA = 0.2 V, V <sub>I</sub> = 2.7 V	1.3	2.3	4	mA
<b>POWER GOOD</b>						
Power good threshold voltage		VSENSE falling		90		%V <sub>ref</sub>
Power good hysteresis voltage <sup>(4)</sup>				3		%V <sub>ref</sub>
Power good falling edge deglitch <sup>(4)</sup>				35		μs
Output saturation voltage, PWRGD		I <sub>(sink)</sub> = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD		V <sub>I</sub> = 5.5 V			1	μA
<b>CURRENT LIMIT</b>						
Current limit trip point		V <sub>I</sub> = 3 V, output shorted <sup>(4)</sup>	4	6.5		A
		V <sub>I</sub> = 6 V, output shorted <sup>(4)</sup>	4.5	7.5		
Current limit leading edge blanking time <sup>(4)</sup>				100		ns
Current limit total response time <sup>(4)</sup>				200		ns
<b>THERMAL SHUTDOWN</b>						
Thermal shutdown trip point <sup>(4)</sup>			135	150	165	°C
Thermal shutdown hysteresis <sup>(4)</sup>				10		°C
<b>OUTPUT POWER MOSFETS</b>						
r <sub>DS(on)</sub>	Power MOSFET switches	V <sub>I</sub> = 6 V		59	88	mΩ
		V <sub>I</sub> = 3 V		85	136	

(4) Specified by design

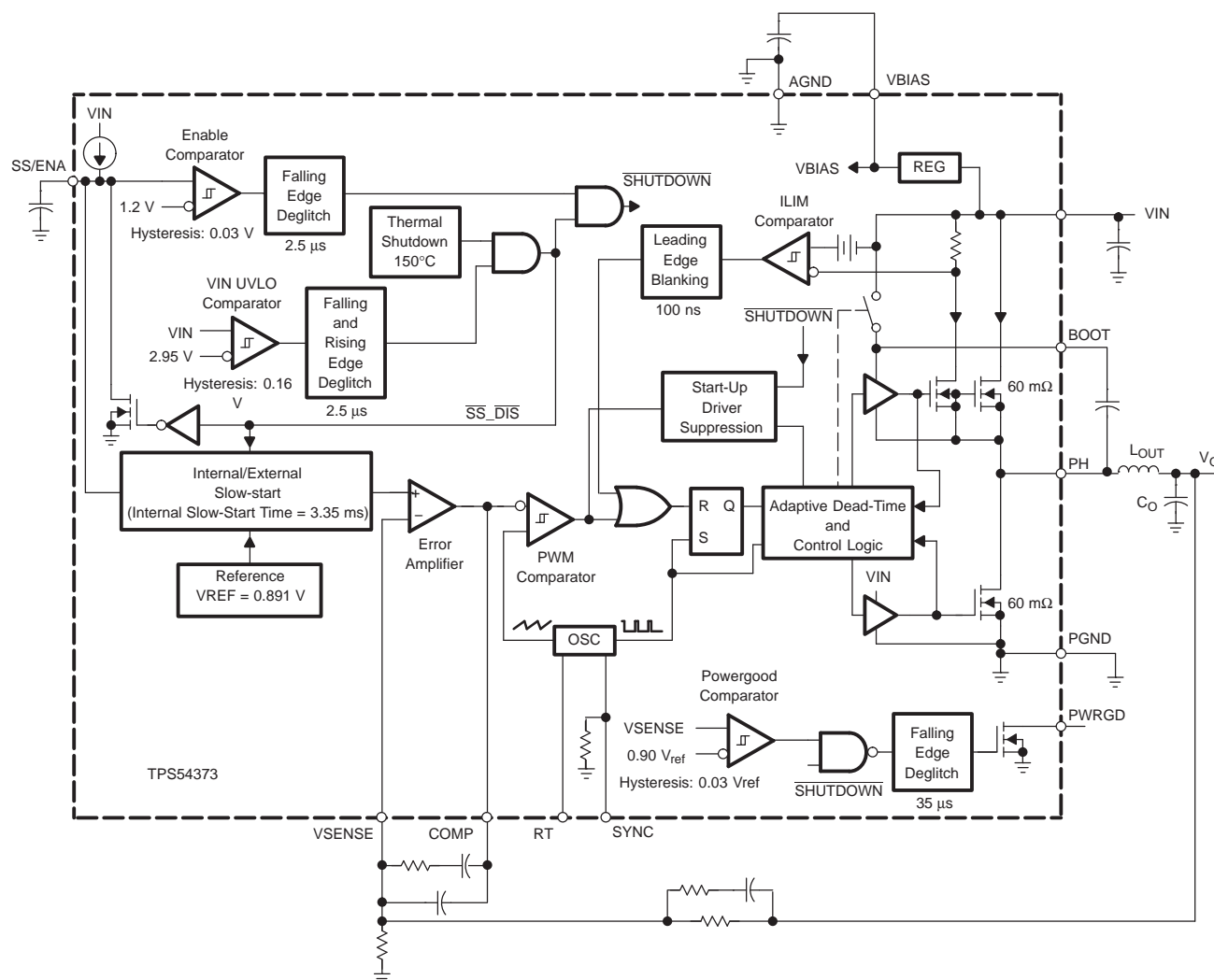
## PIN ASSIGNMENTS



## TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
COMP	1	Error amplifier output. Connect compensation network from COMP to VSENSE.
PWRGD	2	Power good open drain output. High when VSENSE $\geq$ 90% $V_{ref}$ , otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
BOOT	3	Bootstrap input. 0.022- $\mu$ F to 0.1- $\mu$ F low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
PH	4-9	Phase input/output. Junction of the internal high and low-side power MOSFETs, and output inductor.
PGND	11-14	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
VIN	15-17	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1- $\mu$ F to 10- $\mu$ F ceramic capacitor.
VBIAS	18	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1- $\mu$ F to 1.0- $\mu$ F ceramic capacitor.
SS/ENA	19	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	20	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
RT	22	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, $f_s$ .
AGND	23, 25	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Make PowerPAD connection to AGND.
VSNS	24	Error amplifier inverting input.
NC	10, 21	Not connected internally.

## FUNCTIONAL BLOCK DIAGRAM



### ADDITIONAL 3-A SWIFT DEVICES

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS5430/1	Wide Vin/Adjustable	TPS54350	Low Side Gate Drive/Adjustable
TPS54310 & TPS54317	Adjustable	TPS54372	DDR/Adjustable
TPS54380	Sequencing/Adjustable	TPS54373	Prebias/Adjustable

## TYPICAL CHARACTERISTICS

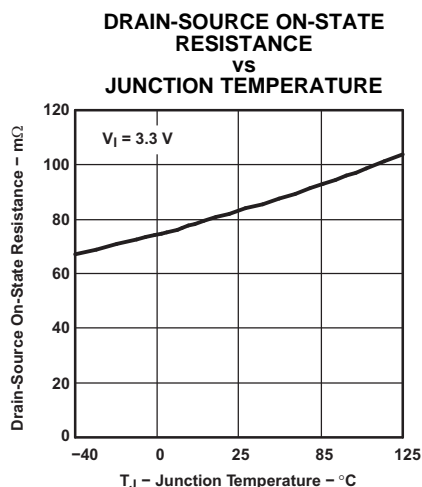


Figure 1.

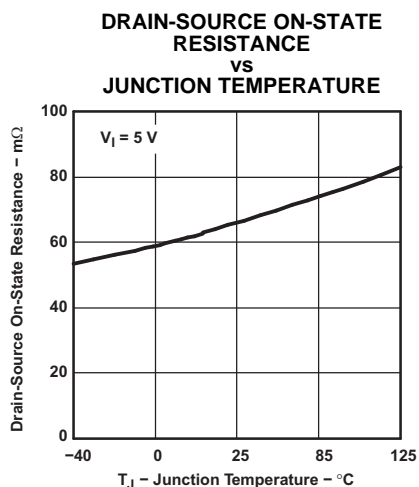


Figure 2.

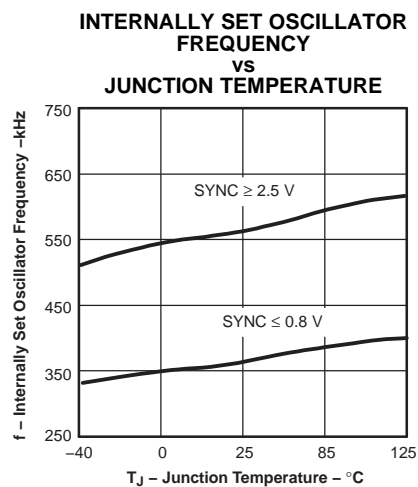


Figure 3.

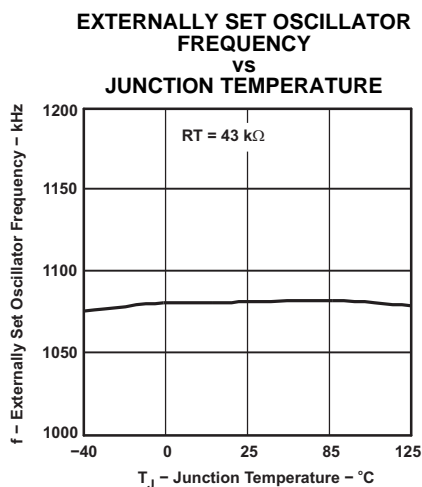


Figure 4.

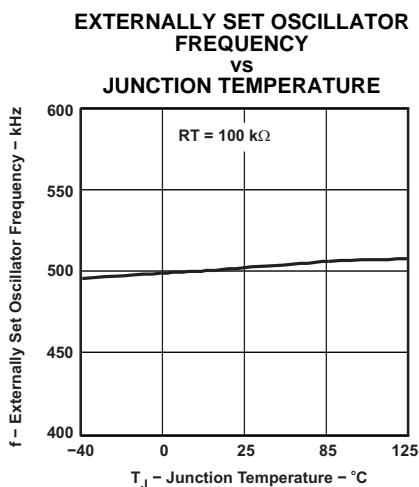


Figure 5.

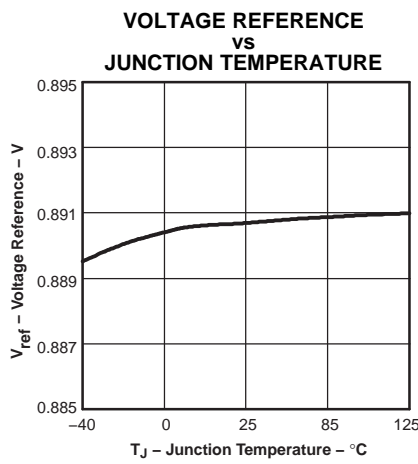


Figure 6.

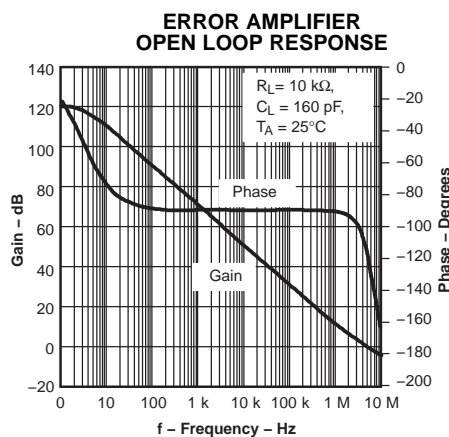


Figure 7.

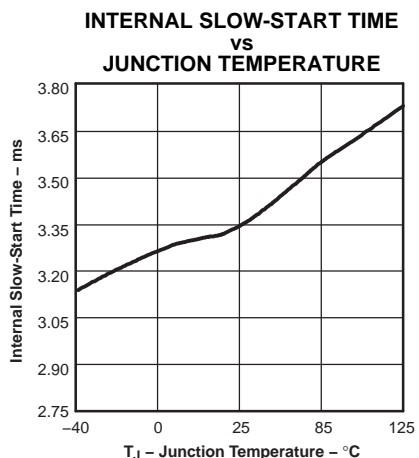


Figure 8.

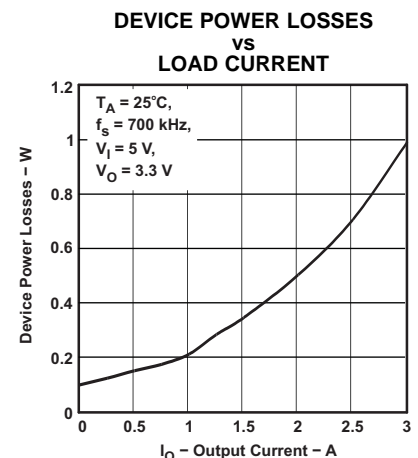


Figure 9.

## APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54377 application. The TPS54377 (U1) provides up to 3 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the power pad underneath the TPS54377 integrated circuit needs to be soldered well to the printed circuit board. The TPS54377 can be evaluated by replacing the TPS54317 on the TPS54317 EVM.

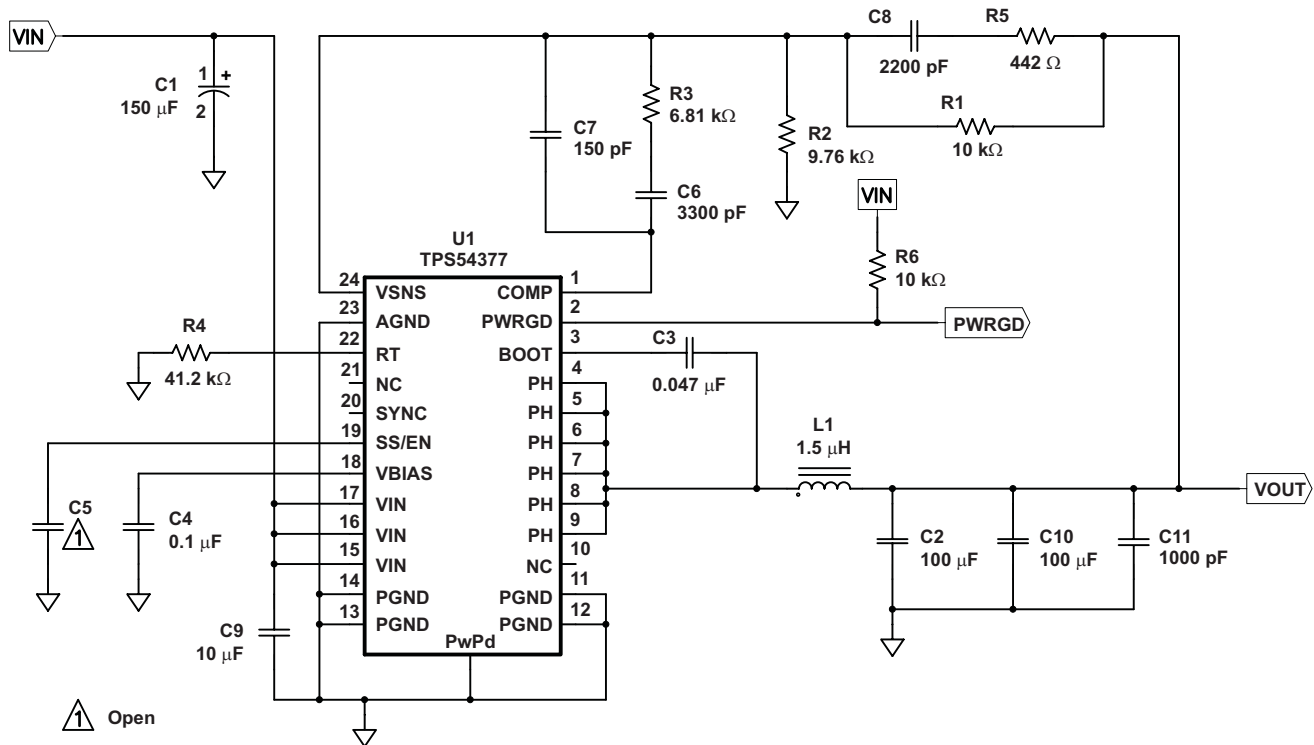


Figure 10. TPS54377 Schematic

## INPUT VOLTAGE

The input to the circuit is a nominal 3.3 VDC, applied at J1. The optional input filter (C1) is a 150-µF capacitor, with a maximum allowable ripple current of 3 A. C9 is the decoupling capacitor for the TPS54377 and must be located as close to the device as possible.

## FEEDBACK CIRCUIT

The resistor divider network of R1 and R2 sets the output voltage for the circuit at 1.8 V. R1, along with R5, R3, C5, C7, and C8 forms the loop compensation network for the circuit. For this design, a Type 3 topology is used.

## OPERATING FREQUENCY

In the application circuit, the 1.1-MHz operation is selected. Connecting a 41.2-kΩ between RT (pin 22) and analog ground can be used to set the switching frequency from 280 kHz to 1.6 MHz. To calculate the RT resistor, use the Equation 1:

$$R(\Omega) = \frac{51 \text{ k}}{f \text{ (MHz)}} - 4.7 \text{ k} \quad (1)$$

## OUTPUT FILTER

The output filter is composed of a 1.5-µH inductor and two capacitors. The inductor is a low dc resistance (0.017 Ω) type, Coilcraft DO1813P-122HC. The feedback loop is compensated so that the unity gain frequency is approximately 75 kHz.

## PCB LAYOUT

Figure 11 shows a generalized PCB layout guide for the TPS54377.

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54377 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.



The TPS54377 has two internal grounds (analog and power). Inside the TPS54377, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54377, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54377. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the voltage set point divider, timing resistor  $R_T$ , slow start capacitor and bias capacitor grounds. Connect this trace directly to AGND (pin 1).

The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins,  $L_O$ ,  $C_O$  and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they must be routed close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. The bias capacitor should be as close as possible to the VBIAS pin and analog ground. If a slow-start capacitor or  $R_T$  resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

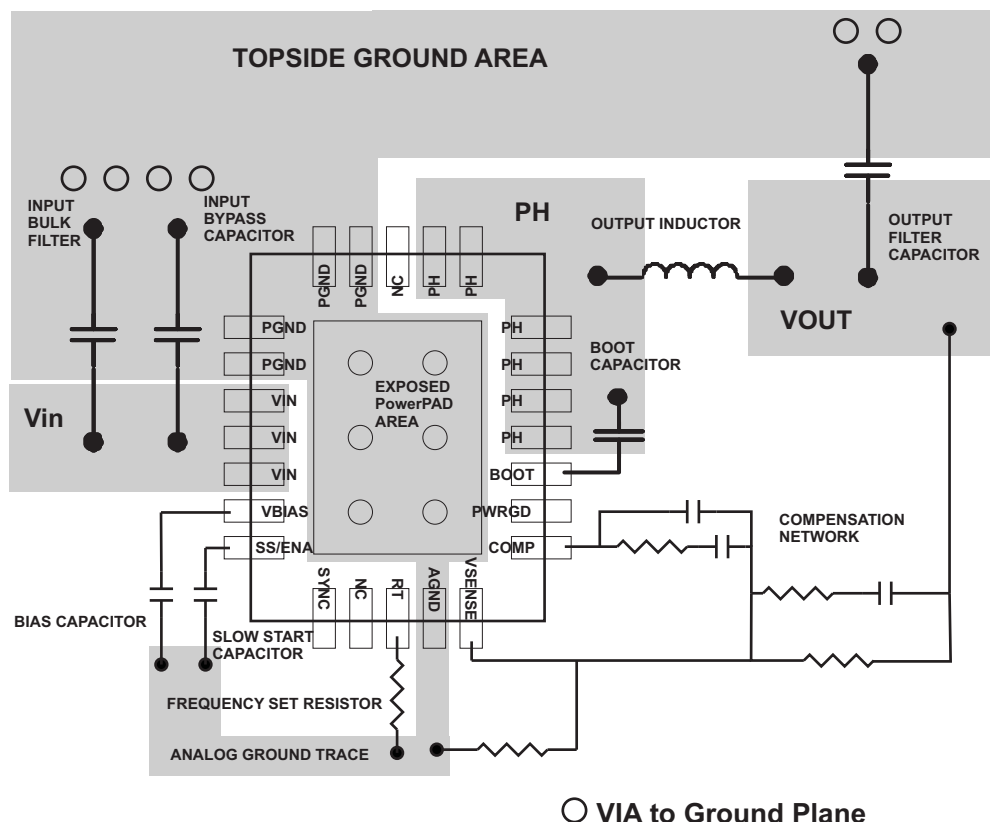


Figure 11. TPS54377 PCB Layout

## LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area additional vias located under the device package may be added to enhance thermal performance. The vias under the package, but not in the exposed thermal pad area, can be increased in size to 0.018.

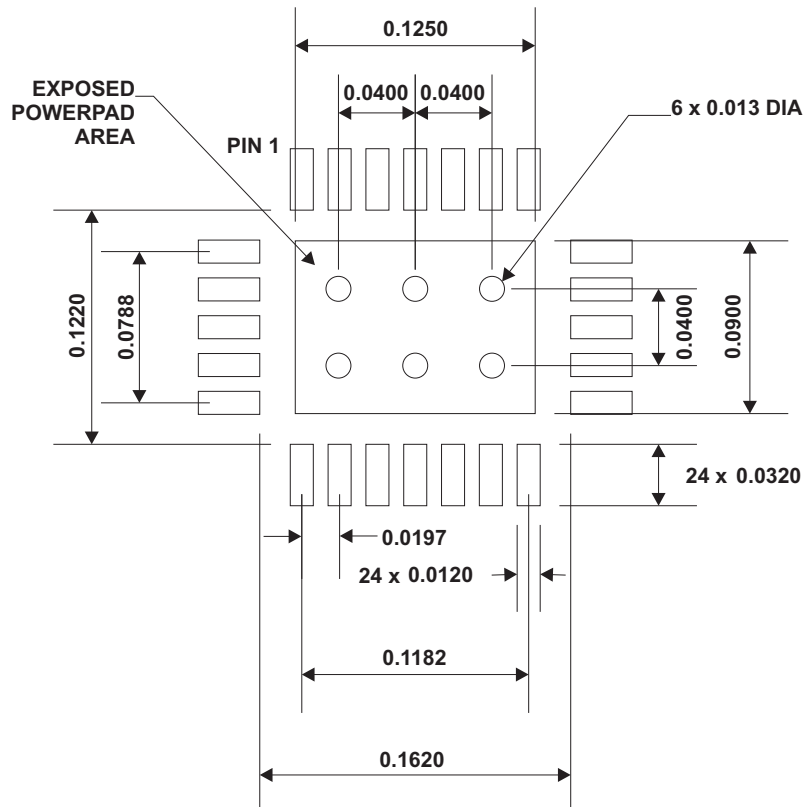


Figure 12. Recommended Land Pattern for 24-Pin QFN PowerPAD

## PERFORMANCE GRAPHS

$T_A = 25^\circ\text{C}$ ,  $f_s = 1.1\text{ MHz}$ ,  $V_I = 3.3\text{ V}$ ,  $V_O = 1.8\text{ V}$  (unless otherwise specified)

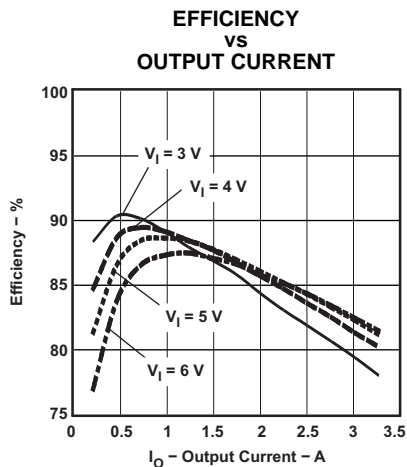


Figure 13.

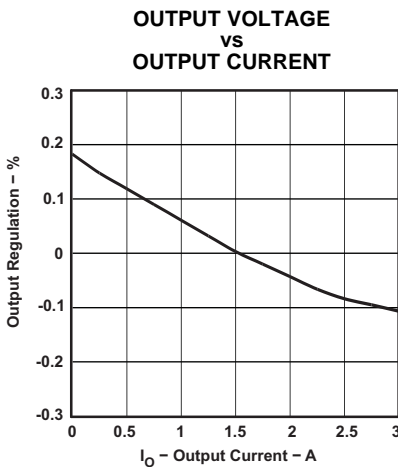


Figure 14.

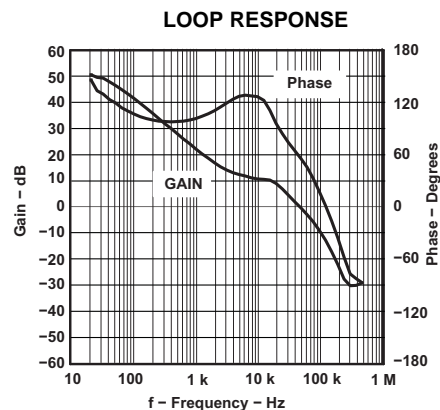


Figure 15.

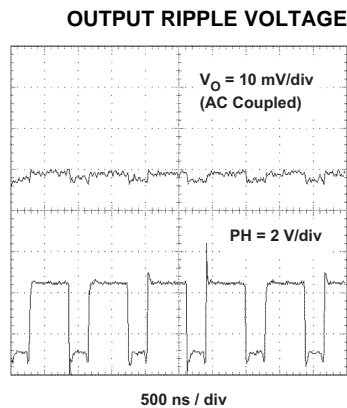


Figure 16.

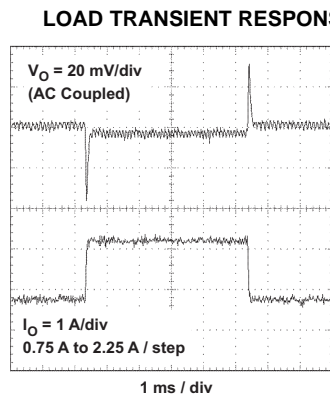


Figure 17.

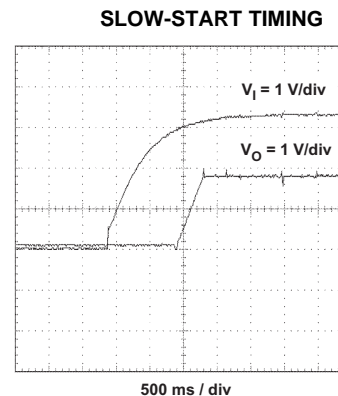


Figure 18.

$T_A = 25^\circ\text{C}$ ,  $f_s = 1.1\text{ MHz}$ ,  $V_I = 3.3\text{ V}$ ,  $V_O = 1.8\text{ V}$  (unless otherwise specified)

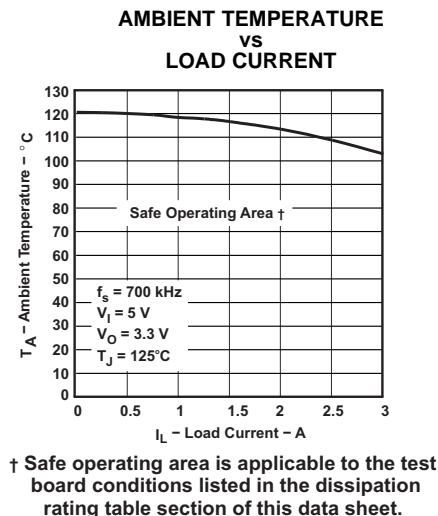


Figure 19.

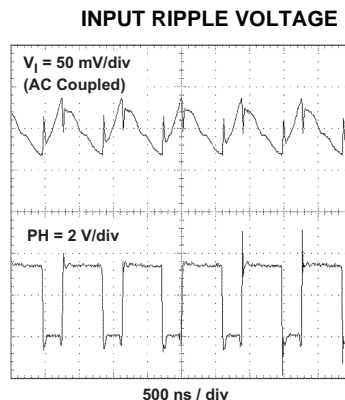


Figure 20.

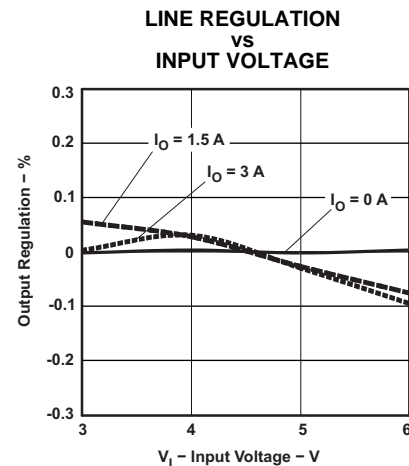


Figure 21.

## DETAILED DESCRIPTION

### Disabled Sinking During Start-Up (DSDS)

The DSDS feature enables minimal voltage drooping of output precharge capacitors at start-up. The TPS54373 is designed to disable the low-side MOSFET to prevent sinking current from a precharge output capacitor during start-up. Once the high-side MOSFET has been turned on to the maximum duty cycle limit, the low-side MOSFET is allowed to switch. Once the maximum duty cycle condition is met, the converter functions as a sourcing converter until the SS/ENA is pulled low.

### Undervoltage Lock Out (UVLO)

The TPS54377 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage ( $V_{IN}$ ) is insufficient. During power up, internal circuits are held inactive until  $V_{IN}$  exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until  $V_{IN}$  falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5- $\mu\text{s}$  rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on  $V_{IN}$ .

### Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions; first, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to

the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5- $\mu\text{s}$  falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\text{ V}}{5\text{ }\mu\text{A}} \quad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\text{ V}}{5\text{ }\mu\text{A}} \quad (3)$$

The actual slow-start is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

## VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

## Voltage Reference

The voltage reference system produces a precise  $V_{ref}$  signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54377, since it cancels offset errors in the scale and error amplifier circuits.

## Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 1600 kHz by connecting a resistor to the RT pin to ground and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY (MHz)} = \frac{51 \text{ k}}{R(\Omega) + 4.7 \text{ k}} \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 1600 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose an RT resistor that sets the free-running frequency to 80% of the synchronization signal. [Table 1](#) summarizes the frequency selection configurations.

**Table 1. Summary of the Frequency Selection Configurations**

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	$\geq 2.5 \text{ V}$	Float
Externally set 280 kHz to 1600 kHz	Float	$R = 27.4 \text{ k to } 180 \text{ k}$
Externally synchronized frequency	Synchronization signal	$R = \text{RT value for } 80\% \text{ of external synchronization frequency}$

## Error Amplifier

The high performance, wide bandwidth, voltage error amplifier sets the TPS54377 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

## PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse duration. During this period, the PWM ramp discharges rapidly

to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn off the high-side FET and turns on the low-side FET. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as  $V_{ref}$ . If the error amplifier output is low, the pwm latch is continually reset and the high-side FET does not turn on. The

low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54377 is capable of sinking current continuously until the  $C_O$  reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor, and consequently, the output current. This process is repeated each cycle in which the current limit comparator is tripped.

### Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFETs is below 2 V. The high-side and low-side drivers are designed with a 300-mA source and sink capability to drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

### Overcurrent Protection

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and differential amplifier, and comparing it to the preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

### Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for

several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown point.

### Power Good (PWRGD)

The power good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of  $V_{ref}$ , the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of  $V_{ref}$  and a 35-μs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

### OUTPUT VOLTAGE LIMITATIONS

Due to the internal design of the TPS54377, there are both upper and lower output voltage limits for any given input voltage. Additionally, the lower boundary of the output voltage set point range is also dependent on operating frequency. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 90% and is given by Equation 5:

$$V_{Omax} = 0.9 \times V_{Imin} - I_{Omax} [(-0.016 \times V_{Imin} + 0.184) + R_L] \quad (5)$$

Where:

$V_{Imin}$  = minimum input voltage

$I_{Omax}$  = maximum load current

$R_L$  = series resistance of the output inductor

Equation 5 assumes maximum on resistance for the internal high-side and low-side FETs.

The lower limit is constrained by the minimum controllable on time which may be as high as 150 ns. The approximate minimum output voltage for a given input voltage, operating frequency, and minimum load current is given in Equation 6:

$$V_{Omin} = (150E-9 \times V_{Imax} \times F_s \times 1.08) - I_{Omin} \times$$

$$\left[ \left( \frac{-0.026}{3} \times V_{Imax} + 0.111 \right) + R_L \right] \quad (6)$$

Where:

$V_I$  = maximum input voltage

$F_s$  = programmed operating frequency

$I_O$  = minimum load current

$R_L$  = series resistance of the output inductor

[Equation 6](#) assumes nominal on resistance for the high-side and low-side FETs, and has an eight percent factor for variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS54377RHFR	ACTIVE	QFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54377RHFGR4	ACTIVE	QFN	RHF	24	3000	TBD	Call TI	Call TI
TPS54377RHFT	ACTIVE	QFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54377RHFTG4	ACTIVE	QFN	RHF	24	250	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

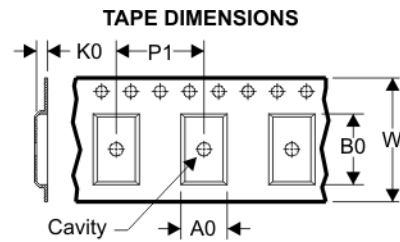
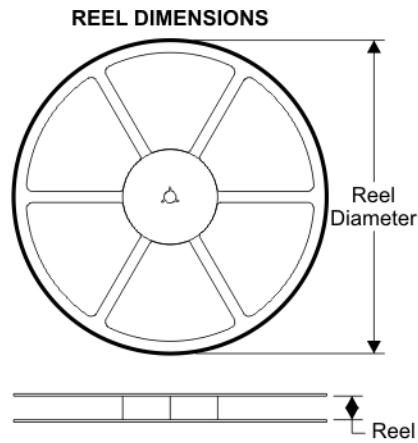
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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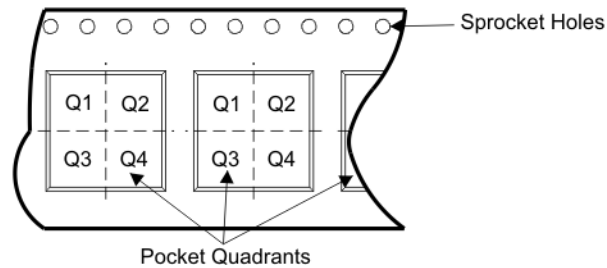


**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54377RHFR	RHF	24	SITE 41	330	12	4.3	5.3	1.3	8	12	Q1

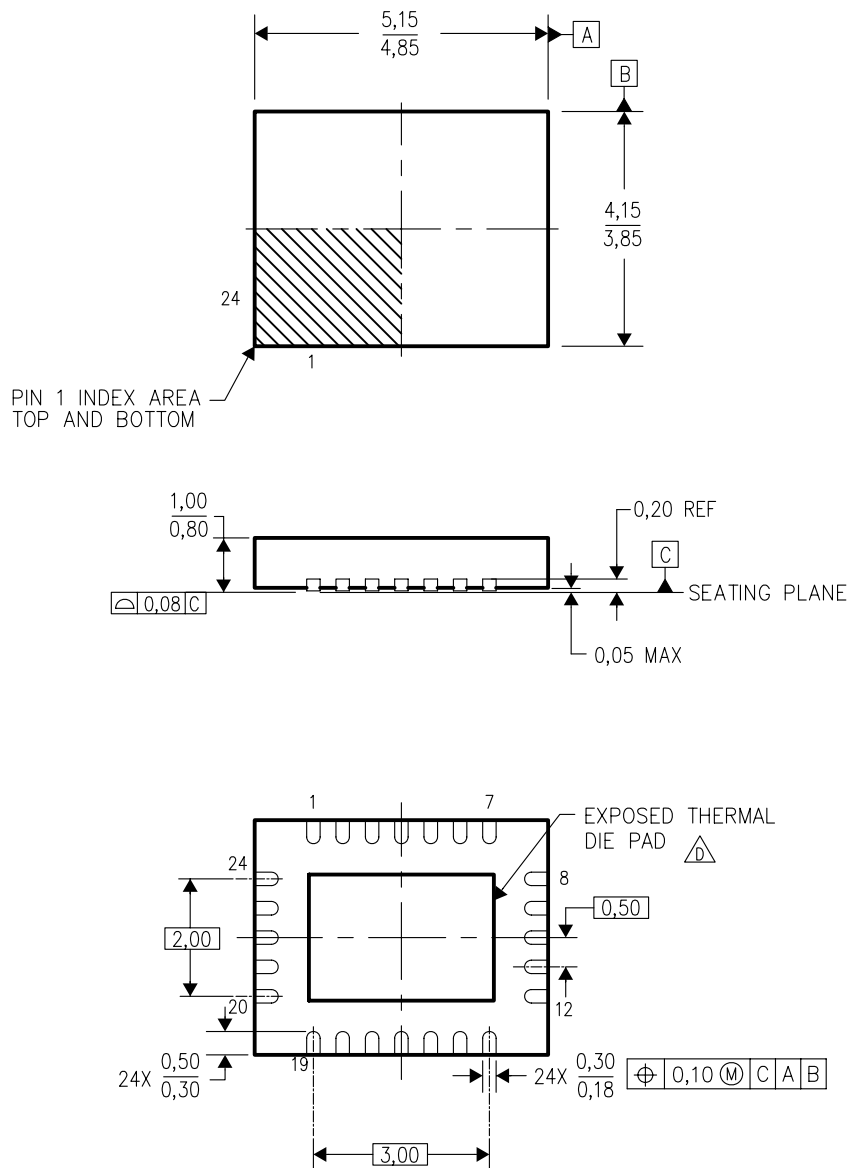
## TAPE AND REEL BOX DIMENSIONS




Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS54377RHFR	RHF	24	SITE 41	346.0	346.0	0.0

## RHF (R-PQFP-N24)

## PLASTIC QUAD FLATPACK



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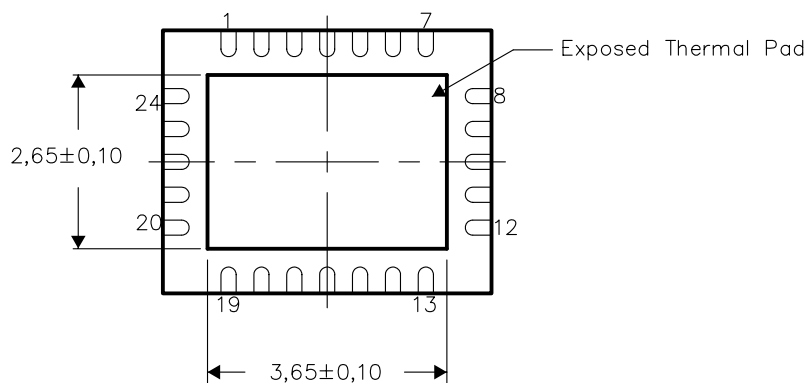
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

## Exposed Thermal Pad Dimensions

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