

STL150N3LLH5

N-channel 30V - 0.0017Ω - 34A - PowerFLAT™ (6x5) STripFET™ V Power MOSFET

Preliminary Data

Features

Туре	V _{DSS}	R _{DS(on)}	I _D
STL150N3LLH5	30 V	<0.002 Ω	34 A ⁽¹⁾

- 1. The value is rated according Rthi-pcb
- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFETTM technology. The lowest available $R_{DS(on)}^*Q_g$, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

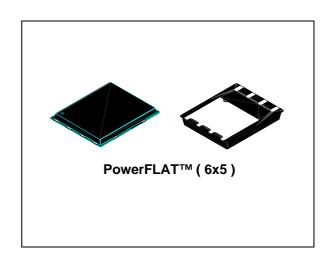


Figure 1. Internal schematic diagram

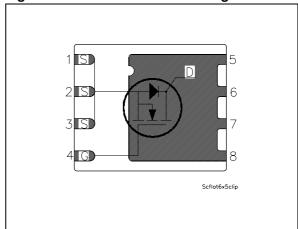


Table 1. Device summary

Order code	Marking	Package	Packaging
STL150N3LLH5	L150N3LLH5	PowerFLAT™ (6x5)	Tape & reel

Contents STL150N3LLH5

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STL150N3LLH5 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	30	V
V _{GS}	Gate-source voltage	± 20	٧
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	150	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100°C	94	Α
I _D ⁽³⁾	Drain current (continuous) at T _C =100°C	21	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	136	Α
I _D ⁽³⁾	Drain current (continuous) at T _C = 25°C	34	Α
P _{TOT} ⁽¹⁾	Total dissipation at T _C = 25°C	80	W
P _{TOT} (3)	Total dissipation at T _C = 25°C	4	W
	Derating factor	0.03	W/°C
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

^{1.} The value is rated according $R_{\text{thj-c}}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case (Drain) (steady state)	1.56	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-ambient	31.3	°C/W

^{1.} When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I _{AV}	Not-repetitive avalanche current, (pulse width limited by Tj Max)	TBD	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AV}$, $V_{DD} = 24$ V)	TBD	J

^{2.} Pulse width limited by safe operating area

^{3.} The value is rated according $R_{\mbox{\scriptsize thj-pcb}}$

Electrical characteristics STL150N3LLH5

2 Electrical characteristics

(T_{CASE} =25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$) $V_{DS} = Max rating,$ $V_{DS} = Max rating @ 125°C$				1 10	μ Α μ Α
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			V
R _{DS(on)}	Static drain-source on resistance	V_{GS} = 10V, I_{D} = 17A V_{GS} = 4.5V, I_{D} = 17A		0.0017 0.0027	0.002 0.003	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f=1 MHz, V _{GS} =0		5800 1600 200		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =15V, I_{D} = 34A V_{GS} =4.5V (see Figure 3)		42 TBD TBD		nC nC nC
R _G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain		2		Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} =15V, I_{D} = 17A, R_{G} =4.7 Ω , V_{GS} =10V (see Figure 2)		TBD TBD TBD TBD		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				34	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				136	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 34A, V _{GS} =0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 34A$, di/dt = 100A/ μ s, $V_{DD} = 25V$, $Tj = 150$ °C		TBD TBD TBD		ns nC A

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Test circuit STL150N3LLH5

3 Test circuit

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

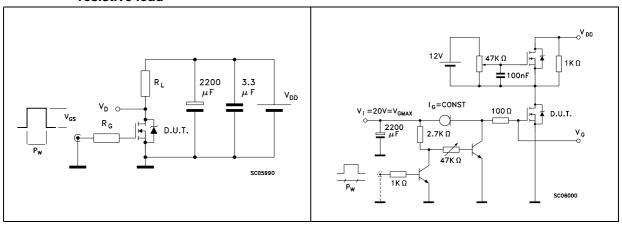


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

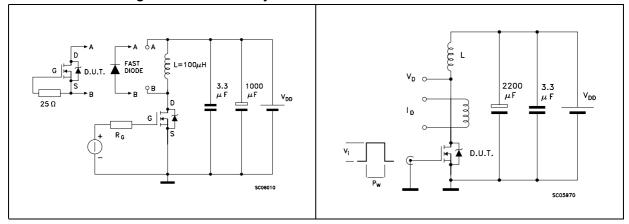
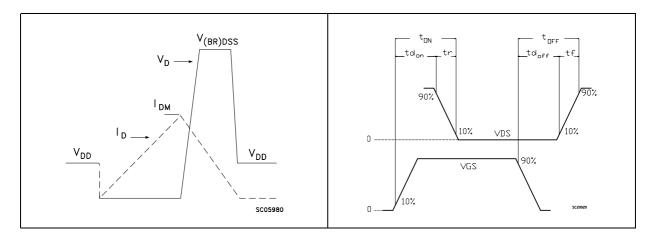


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform

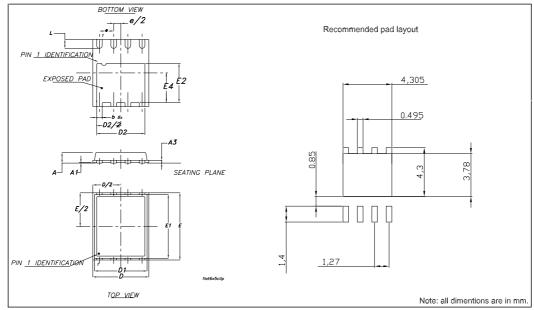


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™(6x5) mechanical data

DIM.		mm.			inch	
DIWI.	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	0.80	0.83	0.93	0.031	0.32	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
Е		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
е		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



STL150N3LLH5 Revision history

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Oct-2007	1	First release

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