



TRIPLE BI-DIRECTIONAL TVS ARRAY FOR ESD PROTECTION

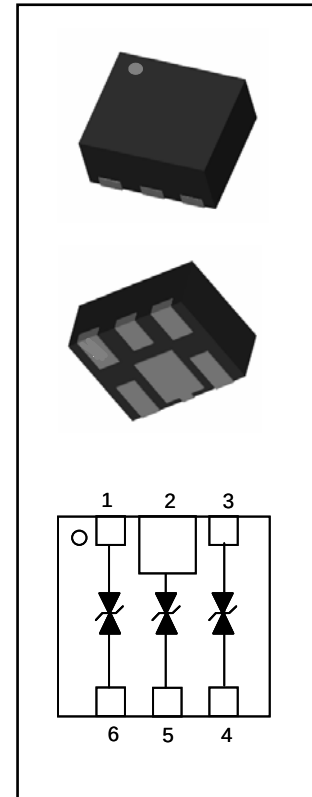
This Triple Bi-directional TVS/Zener Array family have been designed to protect sensitive equipment against ESD in CMOS circuitry operatin at 5V. This TVS array offers an integrated solution to protect up to 3 data lines in applications, where the board space is a premium, in a Quad Flat no-Lead package that only occupies an area of 1.8 sq mm.

SPECIFICATION FEATURES

- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Low Leakage Current, Maximum of 1 μ A at rated voltage
- Maximum Capacitance of 18pF per device at 0Vdc 1MHz
- Peak Power Dissipation of 50W 8/20 μ s Waveform
- Quad Flat No Lead package QFN (1.2x1.5 sq mm, Height: 0.75mm)
- Lead Free Package 100% Tin Plating, Matte finish

APPLICATIONS

- Personal Digital Assistant (PDA)
- Digital Cameras
- Portable Instrumentation
- Mobile Phones and Accessories
- MP3 Players



MAXIMUM RATINGS (Per Device)

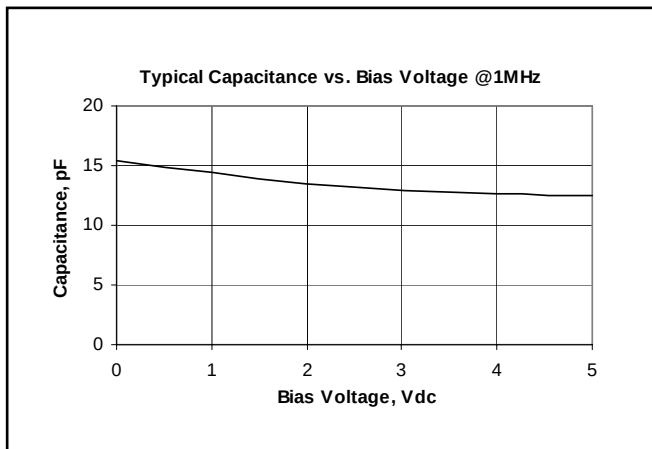
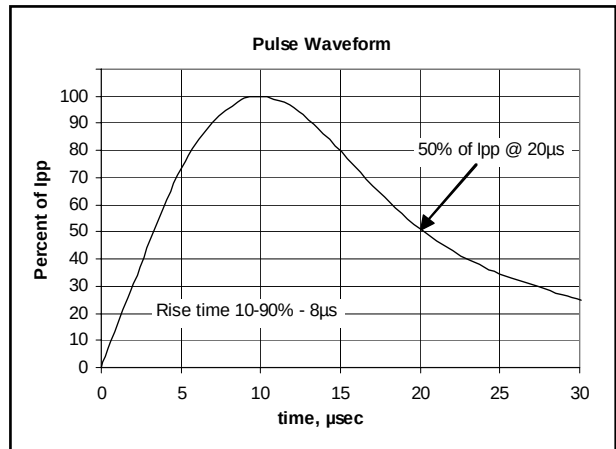
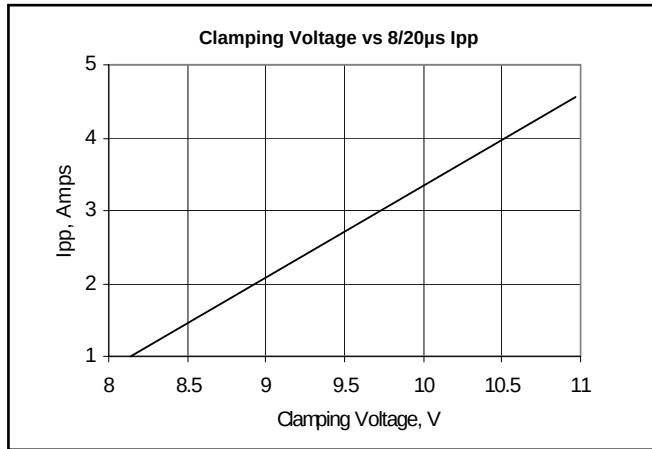
Rating	Symbol	Value	Units
Peak Pulse Power (8/20 μ s Waveform)	P _{PP}	50	W
Peak Pulse Current (8/20 μ s Waveform)	I _{PPM}	5	A
ESD Voltage (HBM Per MIL STD883C - Method 3015-6)	V _{ESD}	25	kV
Operating Temperature Range	T _J	-55 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) T_j = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V _{WRM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA	6			V
Reverse Leakage Current	I _R	V _R = 5V			1	μ A
Clamping Voltage (8/20 μ s)	V _C	I _{pp} = 4A			11	V
Off State Junction Capacitance	C _j	0 Vdc Bias f = 1MHz		15.5	18	pF

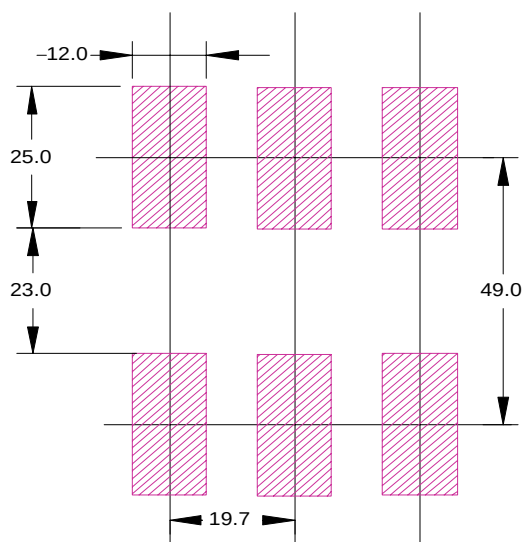
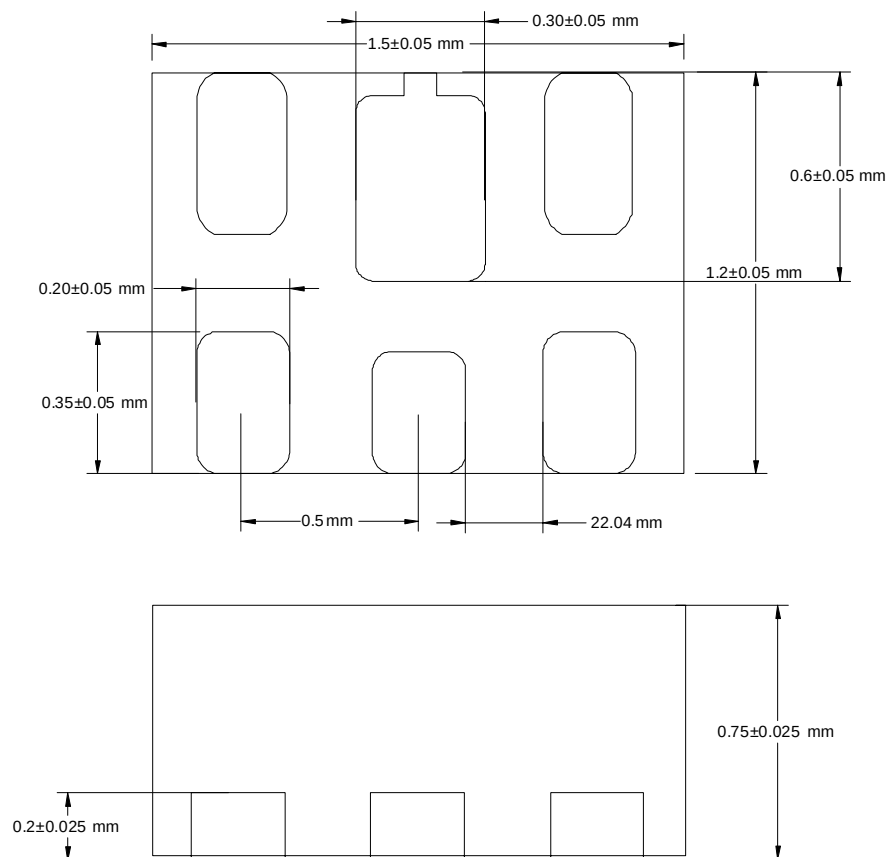
TYPICAL CHARACTERISTIC CURVES (Per Device) $T_j = 25^\circ\text{C}$

PRELIMINARY

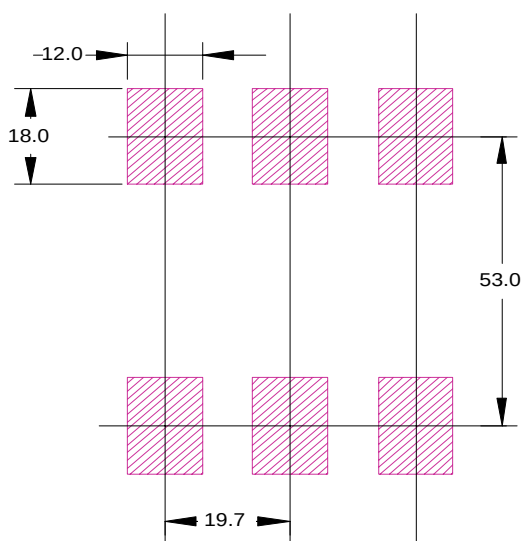




PACKAGE DIMENSIONS AND SUGGESTED PAD LAYOUT



Suggested Pad Layout (in mils)



Alternate Pad Layout SOT666 (in mils)