19-0977; Rev 0; 8/07

Low-Jitter, Precision Clock Generator with Four Outputs

MAX3624

General Description

The MAX3624 is a low-jitter precision clock generator optimized for network application. The device integrates a crystal oscillator and a phase-locked loop (PLL) clock multiplier to generate high-frequency clock outputs for Ethernet, Fibre Channel, SONET/SDH, and other networking applications.

Maxim's proprietary PLL design features ultra-low jitter (0.36ps$_{RMS}$) and excellent power-supply noise rejection, minimizing design risk for network equipment.

The MAX3624 has three LVPECL outputs and one LVCMOS output. Selectable output dividers and a selectable feedback divider allow a range of output frequencies.

Applications

Ethernet Networking Equipment

Fibre Channel Storage Area Network

SONET/SDH Network

Pin Configuration and Typical Application Circuit appear at end of data sheet.

Features

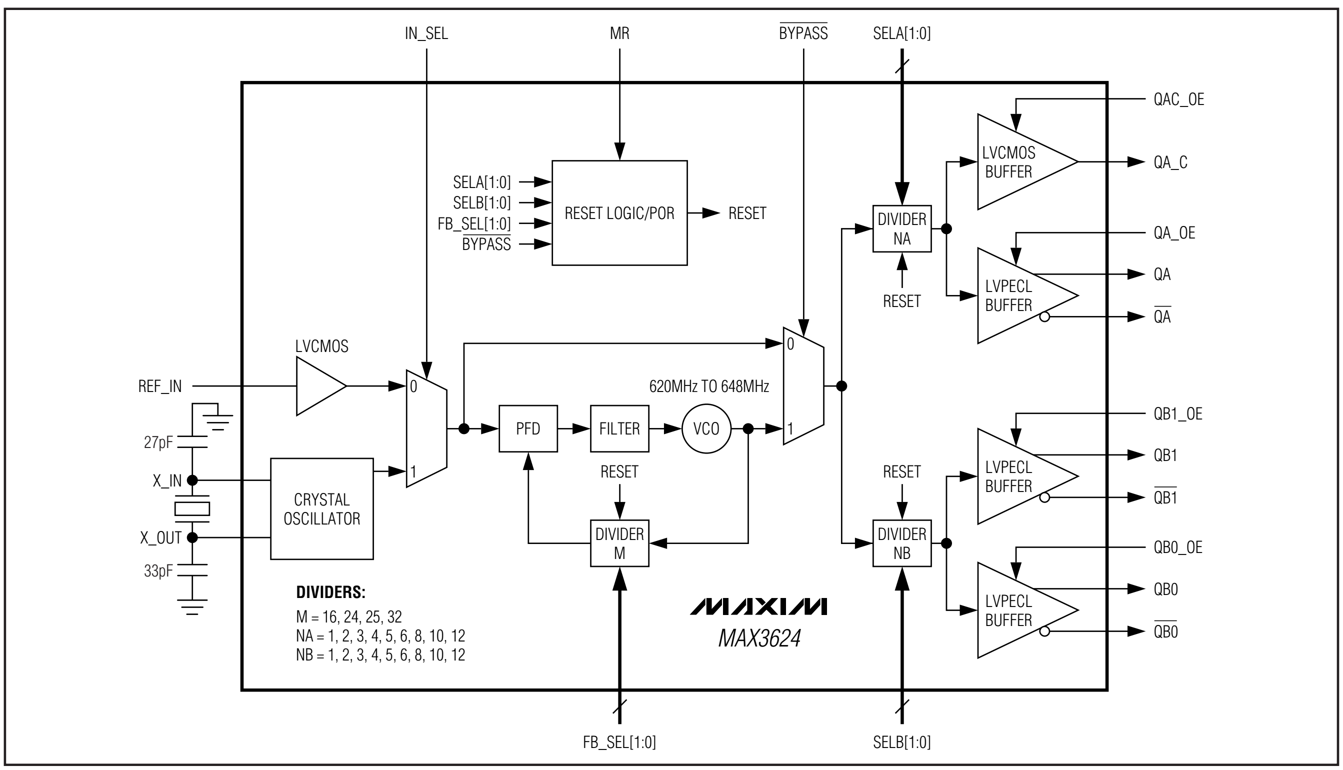
- **Crystal Oscillator Interface: 19.375MHz to 27MHz**
- **CMOS Input: 19MHz to 40.5MHz**
- **Output Frequencies**
  - **Ethernet: 62.5MHz, 125MHz, 156.25MHz, 312.5MHz**
  - **Fibre Channel: 106.25MHz, 159.375MHz, 212.5MHz, 318.5MHz**
  - **SONET/SDH: 77.76MHz, 155.52MHz, 311.04MHz**
- **Low Jitter**
  - **0.14ps$_{RMS}$ (1.875MHz to 20MHz)**
  - **0.36ps$_{RMS}$ (12kHz to 20MHz)**
- **Excellent Power-Supply Noise Rejection**
- **No External Loop Filter Capacitor Required**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3624UTJ+	0°C to +85°C	32 TQFN-EP*	T3255-3

+Denotes a lead-free package.
**EP = Exposed pad.*

Block Diagram



Low-Jitter, Precision Clock Generator with Four Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range V_{CC}, V_{CCA},
V_{DDO_A}, V_{CCO_A}, V_{CCO_B} ....-0.3V to +4.0V
Voltage Range at REF_IN, IN_SEL,
FB_SEL[1:0], SELA[1:0], SELB[1:0],
QAC_OE, QA_OE, QB0_OE, QB1_OE,
MR, $\overline{\text{BYPASS}}$ ....-0.3V to (V_{CC} + 0.3V)
Voltage Range at X_IN Pin ....-0.3V to +1.2V
Voltage Range at GNDO_A..................................-0.3V to +0.3V
Voltage Range at X_OUT Pin ....-0.3V to (V_{CC} - 0.6V)
Current into QA_C ....±50mA
Current into QA, $\overline{\text{QA}}$, QB0, $\overline{\text{QB0}}$, QB1, $\overline{\text{QB1}}$ ....-56mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2759mW
Operating Junction Temperature Range...........-55°C to +150°C
Storage Temperature Range ....-65°C to +160°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	(Note 4)		77	100	mA
CONTROL INPUT CHARACTERISTICS (SELA[1:0], SELB[1:0], FB_SEL[1:0], IN_SEL, QAC_OE, QA_OE, QB1_OE, QB0_OE, MR, $\overline{\text{BYPASS}}$ Pins)						
Input Capacitance	C_{IN}			2		pF
Input Pulldown Resistor	$R_{PULLDOWN}$	Pins MR, FB_SEL[1:0]		75		kΩ
Input Logic Bias Resistor	R_{BIAS}	Pins SELA[1:0], SELB[1:0], QB0_OE		50		kΩ
Input Pullup Resistor	R_{PULLUP}	Pins QAC_OE, QA_OE, QB1_OE, IN_SEL, $\overline{\text{BYPASS}}$		75		kΩ
LVPECL OUTPUTS (QA, $\overline{\text{QA}}$, QB0, $\overline{\text{QB0}}$, QB1, $\overline{\text{QB1}}$ PINS)						
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.7	V_{CC} - 1.55	V
Peak-to-Peak Output-Voltage Swing (Single-Ended)		(Note 2)	0.6	0.72	0.9	V_{P-P}
Clock Output Rise/Fall Time		20% to 80% (Note 2)	200	350	600	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 5)	40	50	60	
LVCMOS/LVTTL INPUTS (SELA[1:0], SELB[1:0], FB_SEL[1:0], IN_SEL, QAC_OE, QA_OE, QB1_OE, QB0_OE, MR, $\overline{\text{BYPASS}}$ Pins)						
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF_IN SPECIFICATIONS (Input DC- or AC-Coupled)						
Reference Clock Frequency		PLL enabled			40.5	MHz
		PLL bypassed			320	
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			240	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-240			µA
Reference Clock Duty Cycle		PLL enabled	30		70	%
Input Capacitance				2.5		pF
QA_C SPECIFICATIONS						
Output High Voltage	V_{OH}	QA_C sourcing 12mA	2.6			V
Output Low Voltage	V_{OL}	QA_C sinking 12mA			0.4	V
Output Rise/Fall Time		(Notes 3 and 6)	250	500	1000	ps
Output Duty Cycle Distortion		PLL enabled	42	50	58	%
		PLL bypassed (Note 5)	40		60	
Output Impedance				14		Ω
CLOCK OUTPUT AC SPECIFICATIONS						
VCO Frequency Range			620		648	MHz
Random Jitter (Note 7)	RJ_{RMS}	12kHz to 20MHz		0.36	1.0	ps_{RMS}
		1.875MHz to 20MHz		0.14		
Total Time Interval Error (TIE) with Supply Noise (Notes 7, 8, and 9)		LVPECL output		14		ps_{P-P}
		LVCMOS output		25		
Total Time Interval Error (TIE) Without Supply Noise (Notes 7, 8)		LVPECL output, LVCMOS output		0.9		ps_{RMS}
				9		ps_{P-P}
Spurs Induced by Power-Supply Noise (Notes 7, 9, 10)		LVPECL output		-57		dBc
		LVCMOS output		-47		
Nonharmonic and Subharmonic Spurs				-70		dBc

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Skew		Between QB0 and QB1		15		ps
		Between QA and QB0 or QB1, PECL outputs		20		
Clock Output SSB Phase Noise at 125MHz (Note 11)		f = 1kHz		-124		dBc/Hz
		f = 10kHz		-125		
		f = 100kHz		-130		
		f = 1MHz		-145		
		f > 10MHz		-153		

Note 1: A series resistor of up to 10.5Ω is allowed between V_{CC} and V_{CCA} for filtering supply noise when system power-supply tolerance is V_{CC} = 3.3V ±5%. See Figure 3.
Note 2: Guaranteed up to 320MHz for LVPECL output.
Note 3: Guaranteed up to 160MHz for LVCMOS output.
Note 4: All outputs enabled and unloaded. IN_SEL set high.
Note 5: Measured with crystal or AC-coupled, 50% duty-cycle signal on REF_IN.
Note 6: Measured using setup shown in Figure 1 with V_{CC} = 3.3V ±5%.
Note 7: Measured with crystal source.
Note 8: Total TIE including random and deterministic jitter. Measured with Agilent DSO81304A 40GS/s real-time oscilloscope using 2M sample record length.
Note 9: Measured with 40mV_{P-P}, 100kHz sinusoidal signal on the supply.
Note 10: Measured at 156.25MHz output.
Note 11: Measured with 25MHz crystal or 25MHz reference clock at LVCMOS input with a slew rate of 0.5V/ns or greater.

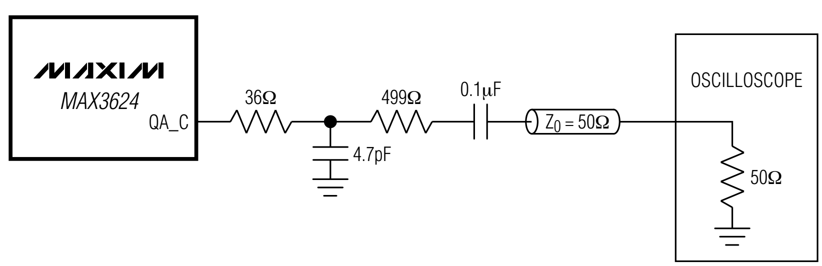
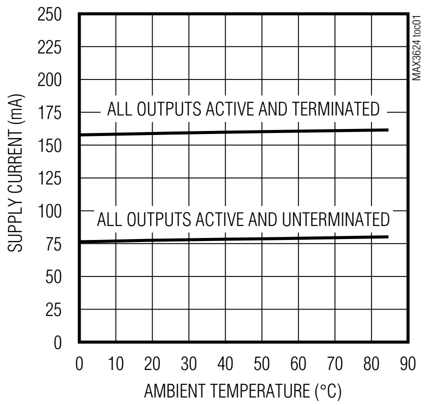


Figure 1. LVCMOS Output Measurement Setup

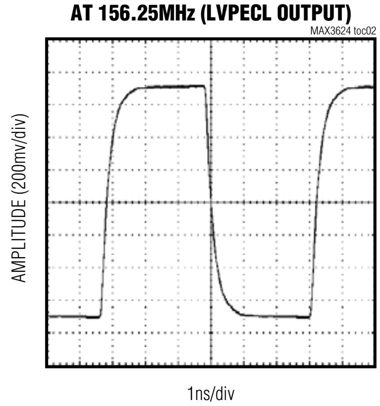
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, crystal frequency = 25MHz.)

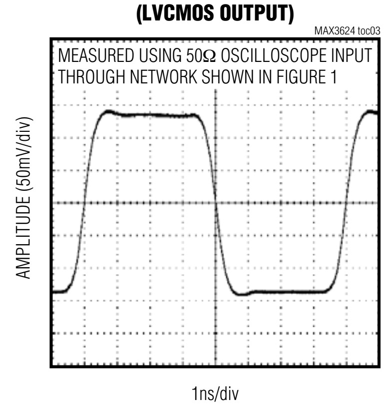
SUPPLY CURRENT vs. TEMPERATURE



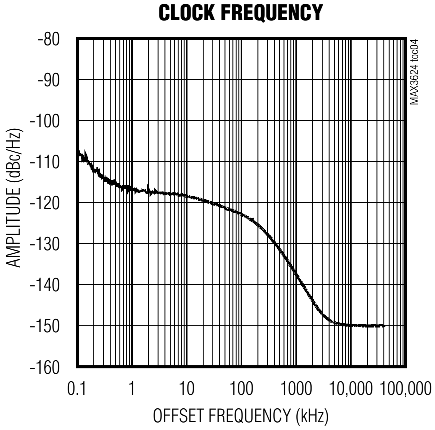
DIFFERENTIAL OUTPUT WAVEFORM AT 156.25MHz (LVPECL OUTPUT)



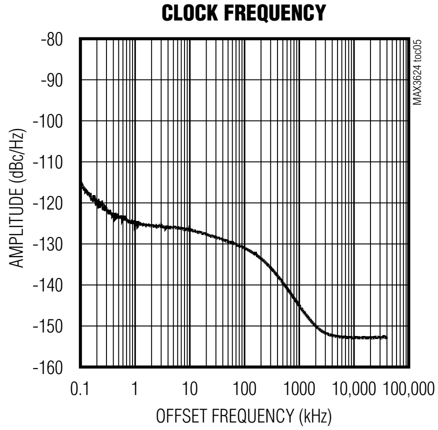
OUTPUT WAVEFORM AT 125MHz (LVCMOS OUTPUT)



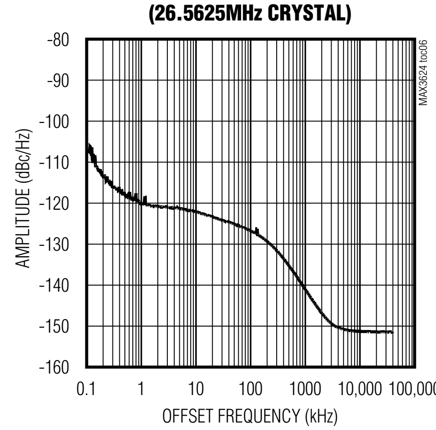
PHASE NOISE AT 312.5MHz CLOCK FREQUENCY



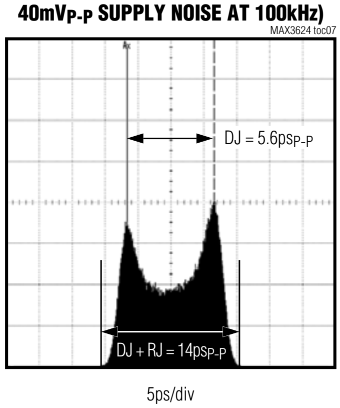
PHASE NOISE AT 125MHz CLOCK FREQUENCY



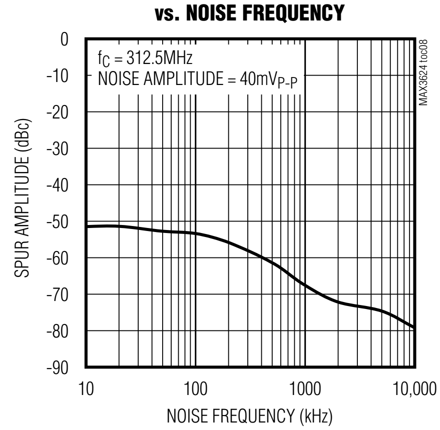
PHASE NOISE AT 212.5MHz CLOCK FREQUENCY (26.5625MHz CRYSTAL)



JITTER HISTOGRAM (312.5MHz OUTPUT, 40mVP-P SUPPLY NOISE AT 100kHz)



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	V_{CCO_B}	Power Supply for QB0 and QB1 Clock Outputs. Connect to +3.3V.
2, 19, 24	GND	Supply Ground
3	QB0_OE	LVCMOS/LVTTL Input. Enables/disables QB0 clock output. Connect pin high or leave open to enable LVPECL clock output QB0. Connect low to set QB0 to a logic 0. Has internal 50kΩ input impedance.
4, 5	SELB1, SELB0	LVCMOS/LVTTL Input. Controls NB divider setting. Has 50kΩ input impedance. See Table 2 for more information.
6	QAC_OE	LVCMOS/LVTTL Input. Enables/disables QA_C clock output. Connect pin high or leave open to enable QA_C. Connect low to set QA_C to a high-impedance state. Has internal 75kΩ pullup to V_{CC}.
7	MR	LVCMOS/LVTTL Input. Master reset input. Pulse high for > 1µs to reset all dividers. Has internal 75kΩ pulldown to GND. Not required for normal operation.
8	GNDO_A	Ground for QA_C Output. Connect to supply ground.
9	QA_C	LVCMOS Clock Output
10	V_{DDO_A}	Power Supply for QA_C Clock Output. Connect to +3.3V.
11	V_{CCO_A}	Power Supply for QA Clock Output. Connect to +3.3V.
12	QA	Noninverting Clock Output, LVPECL
13	$\overline{QA}$	Inverting Clock Output, LVPECL
14	$\overline{BYPASS}$	LVCMOS/LVTTL Input (Active Low). Connect low to bypass the internal PLL. Connect high or leave open for normal operation. When in bypass mode the output dividers are set to divide by 1. Has internal 75kΩ pullup to V_{CC}.
15, 16	FB_SEL1, FB_SEL0	LVCMOS/LVTTL Input. Controls M divider setting. See Table 3 for more information. Has internal 75kΩ pulldown to GND.
17	V_{CCA}	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can connect to V_{CC} through 10.5Ω as shown in Figure 2 (requires V_{CC} = +3.3V ±5%).
18	V_{CC}	Core Power Supply. Connect to +3.3V.
20	QA_OE	LVCMOS/LVTTL Input. Enables/disables the QA clock output. Connect this pin high or leave open to enable the LVPECL clock output QA. Connect low to set QA to a logic 0. Has internal 75kΩ pullup to V_{CC}.
21, 22	SELA0, SELA1	LVCMOS/LVTTL Input. Controls NA divider setting. See Table 2 for more information. Has 50kΩ input impedance.
23	QB1_OE	LVCMOS/LVTTL Input. Enables/disables QB1 clock output. Connect pin high or leave open to enable LVPECL clock output QB1. Connect low to set QB1 to a logic 0. Has internal 50kΩ input impedance.
25	X_OUT	Crystal Oscillator Output
26	X_IN	Crystal Oscillator Input
27	REF_IN	LVCMOS Reference Clock Input. Self-biased to allow AC- or DC-coupling.
28	IN_SEL	LVCMOS/LVTTL Input. Connect high or leave open to use a crystal. Connect low to use REF_IN. Has internal 75kΩ pullup to V_{CC}.
29	$\overline{QB1}$	LVPECL, Inverting Clock Output
30	QB1	LVPECL, Noninverting Clock Output
31	$\overline{QB0}$	LVPECL, Inverting Clock Output
32	QB0	LVPECL, Noninverting Clock Output
—	EP	Exposed Pad. Connect to supply ground for proper electrical and thermal performance.

Detailed Description

The MAX3624 is a low-jitter clock generator designed to operate at Ethernet, Fibre Channel, and SONET/SDH frequencies. It consists of an on-chip crystal oscillator, PLL, programmable dividers, LVCMOS output buffer, and LVPECL output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance.

Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X_IN and X_OUT. Crystal frequency is 19.375MHz to 27MHz.

REF_IN Buffer

An LVCMOS-compatible clock source can be connected to REF_IN to serve as the reference clock.

The LVCMOS REF_IN buffer is internally biased to allow AC- or DC-coupling. It is designed to operate up to 320MHz.

PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO) with a 620MHz to 648MHz operating range. The VCO output is connected to the PFD input through a feedback divider. See Table 3 for divider values. The PFD compares the reference frequency to the divided-down VCO output (f_{VCO}/M) and generates a control signal that keeps the VCO locked to the reference clock. The high-frequency VCO output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (V_{CCA}) is isolated from the core logic and output buffer supplies.

Output Dividers

The output divider is programmable to allow a range of output frequencies. See Table 2 for the divider input settings. The output dividers are automatically set to divide by 1 when the MAX3624 is in bypass mode ($\overline{BYPASS}$ = 0).

LVPECL Drivers

The high-frequency outputs—QA, QB0, and QB1—are differential PECL buffers designed to drive transmission lines terminated with 50Ω to V_{CC} - 2.0V. The maximum operating frequency is specified up to 320MHz. Each output can be individually disabled, if not used. The outputs go to a logic 0 when disabled.

LVCMOS Driver

QA_C, the LVCMOS output, is designed to drive a single-ended high-impedance load. The maximum operating frequency is specified up to 160MHz. This output can be disabled by the QAC_OE pin if not used and goes to a high impedance when disabled.

Reset Logic/POR

During power-on, the power-on reset (POR) signal is generated to synchronize all dividers. An external master reset (MR) signal is not required.

Applications Information

Power-Supply Filtering

The MAX3624 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. In addition to excellent on-chip power-supply noise rejection, the MAX3624 provides a separate power-supply pin, V_{CCA}, for the VCO circuitry. Figure 2 illustrates the recommended power-supply filter network for V_{CCA}. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins for best performance.

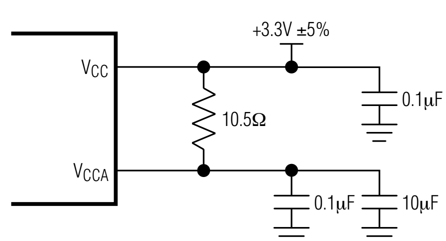


Figure 2. Analog Supply Filtering

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Table 1. Output Frequency Determination Chart

XO OR CMOS INPUT FREQUENCY (MHz)	FEEDBACK DIVIDER, M	VCO FREQUENCY (MHz)	OUTPUT DIVIDER, NA AND NB	OUTPUT FREQUENCY (MHz)	APPLICATIONS
25	25	625	2	312.5	Ethernet
			4	156.25	
			5	125	
			8	78.125	
			10	62.5	
25.78125	25	644.53125	4	161.132812	10Gbps Ethernet
26.04166	24	625	2	312.5	Ethernet
			4	156.25	
			5	125	
			8	78.125	
			10	62.5	
26.5625	24	637.5	2	318.75	Fibre Channel
			3	212.5	
			4	159.375	
			6	106.25	
			12	53.125	
19.44	32	622.08	2	311.04	SONET/SDH
			4	155.52	
			8	77.76	
38.88 (CMOS input)	16	622.08	2	311.04	SONET/SDH
			4	155.52	
			8	77.76	

Output Divider Configuration

Table 2 shows the input settings required to set the output dividers. Leakage in the OPEN case must be less than 1µA. Note that when the MAX3624 is in bypass mode ($\overline{\text{BYPASS}}$ set low), the output dividers are automatically set to divide by 1.

Table 2. Output Divider Configuration Chart

INPUT		NA/NB DIVIDER
SELA1/SELB1	SELA0/SELB0	
0	0	/ 2*
0	1	/ 3*
1	0	/ 4
1	1	/ 5
1	OPEN	/ 6
OPEN	1	/ 8
0	OPEN	/ 10
OPEN	0	/ 12
OPEN	OPEN	/ 1*

**Maximum guaranteed output frequency is 160MHz for CMOS and 320MHz for LVPECL output.*

PLL Divider Configuration

Table 3 shows the input settings required to set PLL feedback divider.

Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 4 for recommended crystal specifications. See Figure 4 for external capacitance connection.

Crystal Input Layout and Frequency Stability

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the MAX3624's X_IN and X_OUT pins to reduce crosstalk of active signals into the oscillator.

The layout shown in Figure 3 gives approximately 3pF of trace plus footprint capacitors per side of the crystal (Y1). The dielectric material is FR-4 and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C22 = 27pF and C23 = 33pF, the measured output frequency accuracy is -14ppm at +25°C ambient temperature.

Table 3. PLL Divider Configuration Chart

INPUT		M DIVIDER
FB_SEL1	FB_SEL0	
0	0	/ 25
0	1	/ 24
1	0	/ 32
1	1	/ 16

Table 4. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f_{OSC}	19.375		27	MHz
Shunt Capacitance	C_O		2.0	7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S			50	Ω
Maximum Crystal Drive Level				300	µW

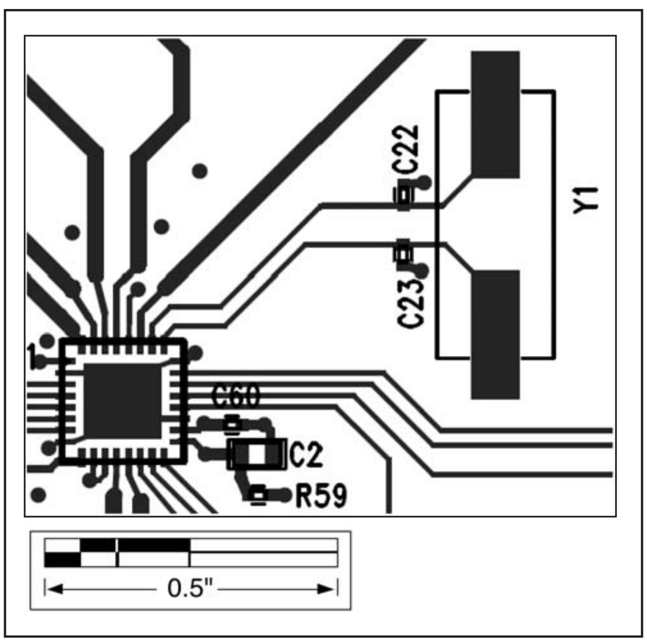


Figure 3. Crystal Layout

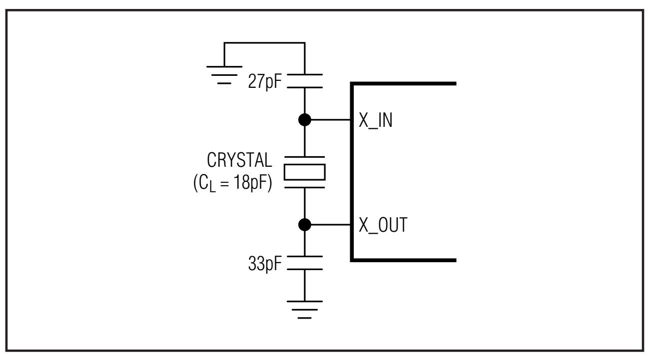


Figure 4. Crystal, Capacitors Connection

Low-Jitter, Precision Clock Generator with Four Outputs

Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 8. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to $V_{TT} = V_{CC}$ - 2V. If a separate termination voltage (V_{TT}) is not available, other terminations methods can be used such as shown in Figure 5 and Figure 6. Unused outputs should be disabled and may be left open. For more information on LVPECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

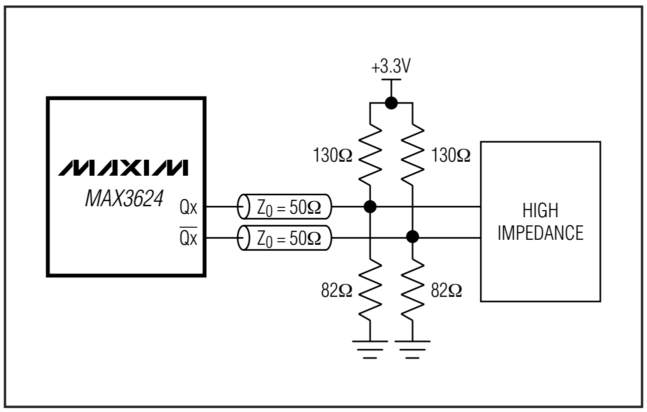


Figure 5. Thevenin Equivalent of Standard PECL Termination

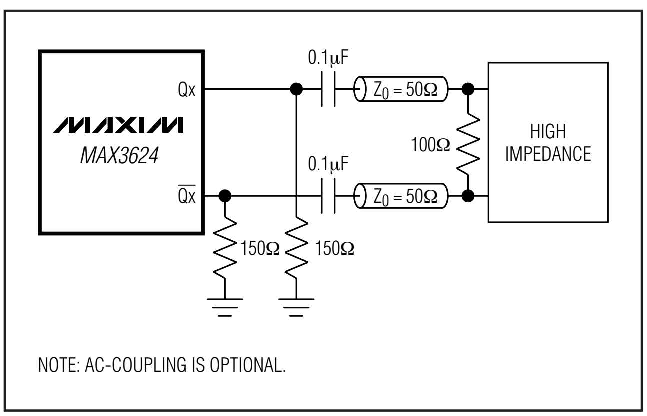


Figure 6. AC-Coupled PECL Termination

Interface Models

Figure 7, Figure 8, and Figure 9 show examples of interface models.

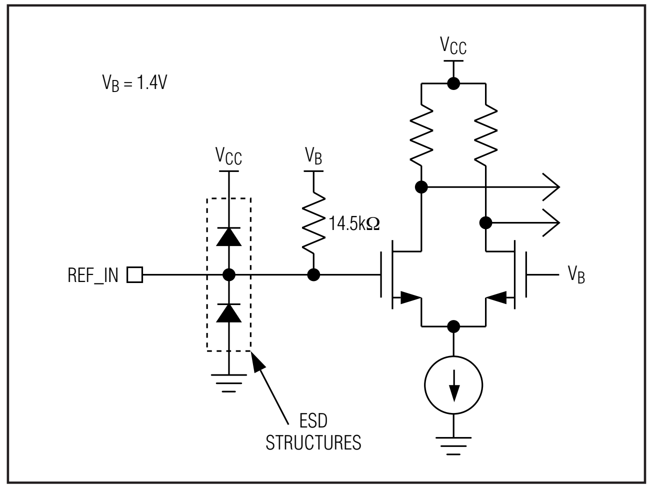


Figure 7. Simplified REF_IN Pin Circuit Schematic

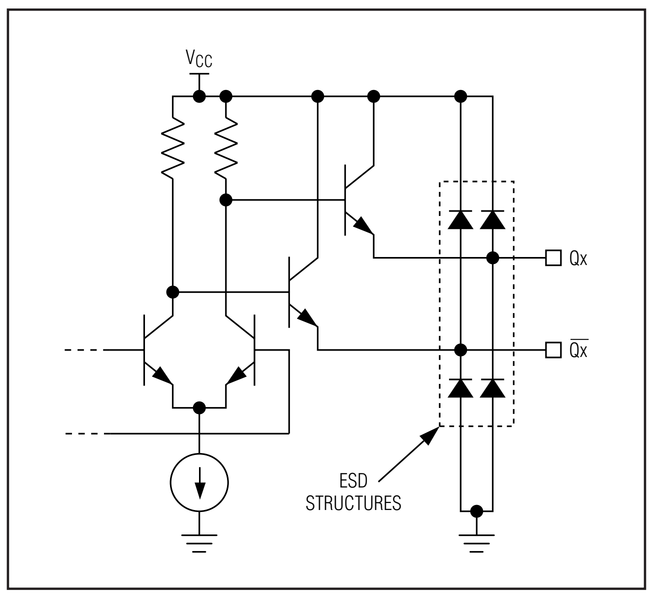


Figure 8. Simplified LVPECL Output Circuit Schematic

Low-Jitter, Precision Clock Generator with Four Outputs

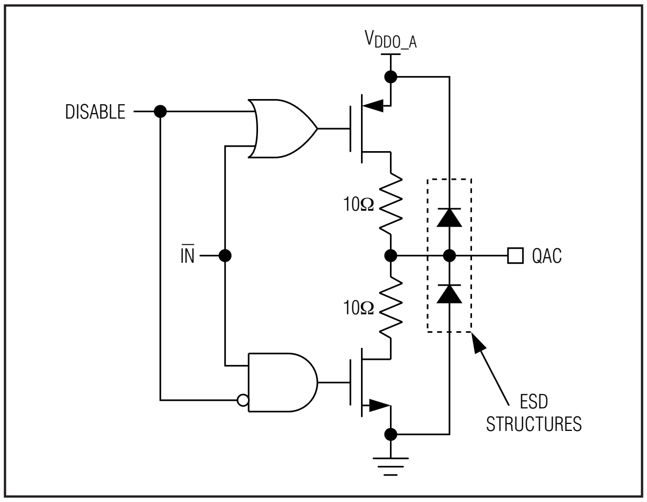


Figure 9. Simplified LVCMOS Output Circuit Schematic

Layout Considerations

The inputs and outputs are critical paths for the MAX3624, and care should be taken to minimize discontinuities on these transmission line. Here are some suggestions for maximizing the MAX3624's performance:

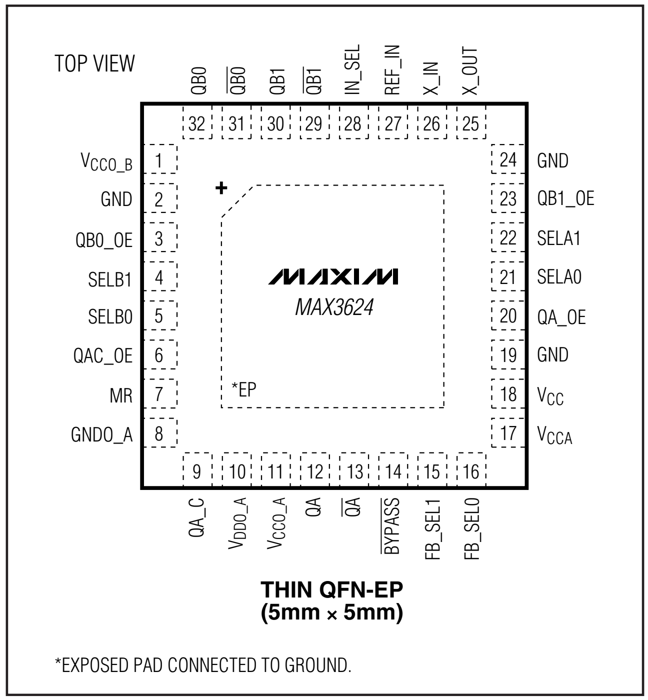
- An uninterrupted ground plane should be positioned beneath the clock I/Os.
- Ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3624 and the receive devices.
- Supply decoupling capacitors should be placed close to the MAX3624 supply pins.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance out of the MAX3624.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3624 Evaluation Kit for more information.

Exposed-Pad Package

The exposed pad on the 32-pin TQFN package provides a very low inductance path for return current traveling to the PCB ground plane. The pad is also electrical ground on the MAX3624 and must be soldered to the circuit board ground for proper electrical performance.

Pin Configuration



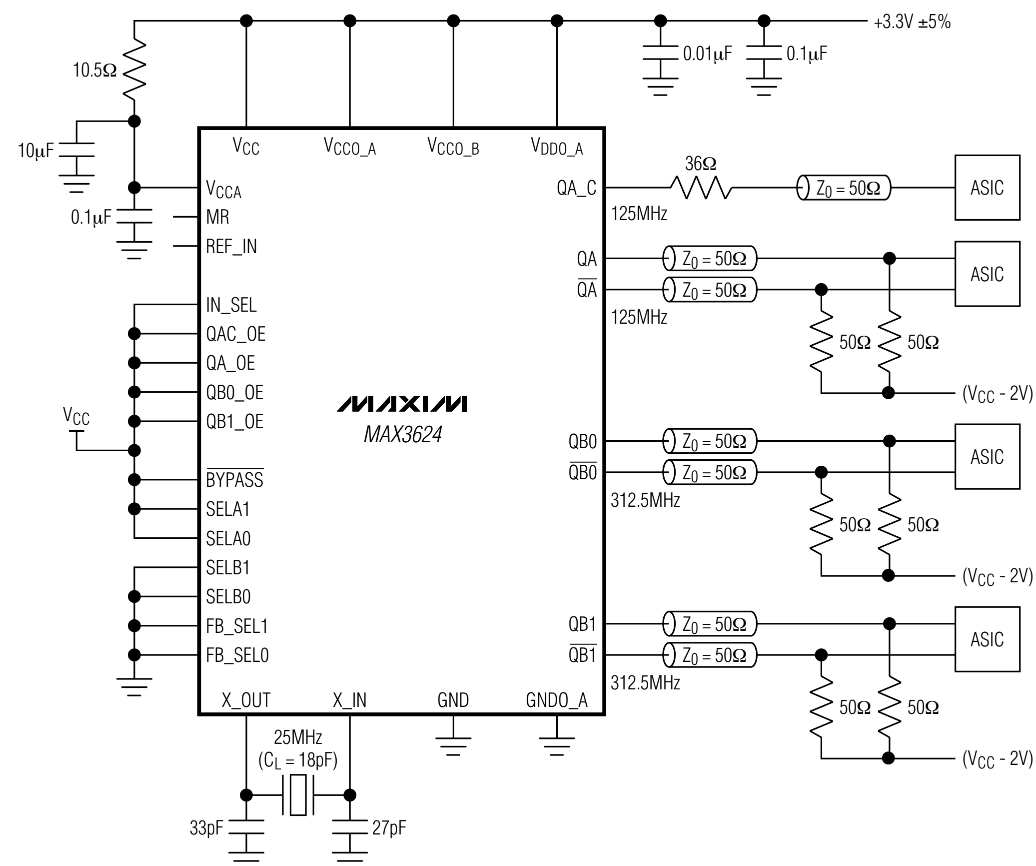
Chip Information

TRANSISTOR COUNT: 10,780

PROCESS: BiCMOS

Low-Jitter, Precision Clock Generator with Four Outputs

Typical Application Circuit



Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	DOCUMENT NO.
32 TQFN-EP	21-0140