National Semiconductor

PRELIMINARY
April 2007

LMH0344
3Gbps HD/SD SDI Adaptive Cable Equalizer

General Description

The LMH0344 3Gbps HD/SD SDI Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 143 Mbps to 2.97 Gbps and supports SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M.

The LMH0344 implements DC restoration to correctly handle pathological data conditions. The equalizer may be driven in either a single ended or differential configuration.

Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation.

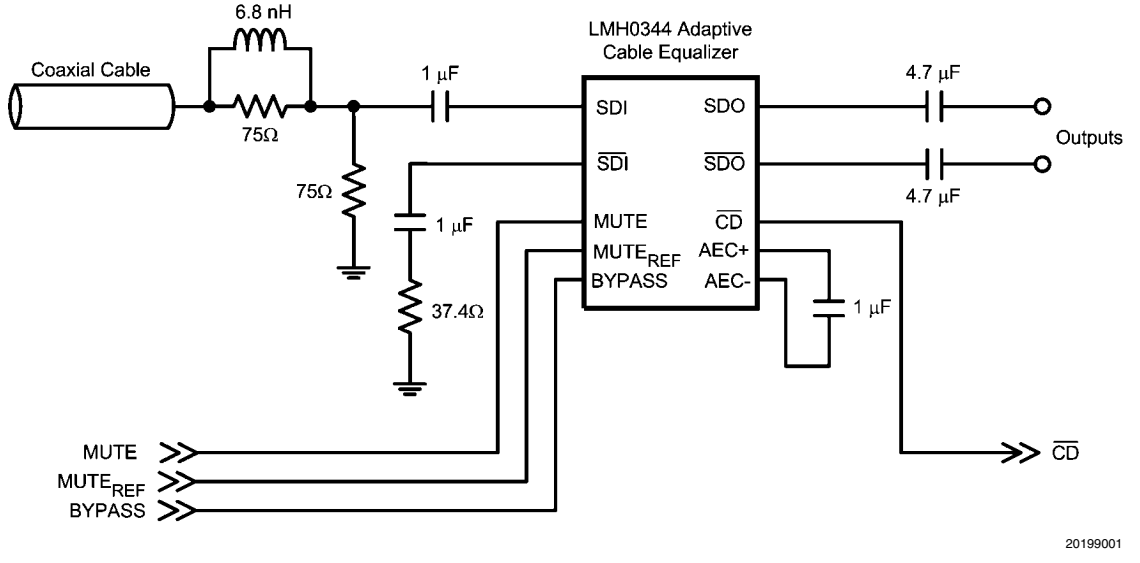
Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- Supports DVB-ASI at 270 Mbps
- High data rates: 143 Mbps to 2.97 Gbps
- Equalizes up to 120 meters of Belden 1694A at 2.97 Gbps, up to 140 meters of Belden 1694A at 1.485 Gbps, or up to 350 meters of Belden 1694A at 270 Mbps
- Equalizes 0-100m of Belden 1694A at 2.97 Gbps with 0.3 UI maximum output jitter
- Manual bypass and output mute with a programmable threshold
- Single-ended or differential input
- 50Ω differential outputs
- Single 3.3V supply operation
- 280mW typical power consumption with 3.3V supply
- Footprint compatible with the LMH0044
- Replaces the Gennum GS2974 or GS2974A

Applications

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces
- Serial digital data equalization and reception
- Data recovery equalization

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance	
θ_{JA} 16-pin LLP	+43°C/W
θ_{JC} 16-pin LLP	+8°C/W
ESD Rating (HBM)	8kV
ESD Rating (MM)	250V

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	0°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$		1.9		V
V_{SDI}	Input Voltage Swing	At LMH0344 input, (Notes 4, 5)		720	800	950	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, $\overline{SDO}$		V_{CC} – V_{SDO}/2		V
V_{SDO}	Output Voltage Swing	50Ω load, differential			750		mV_{P-P}
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.7		V
	$\overline{CD}$ Output Voltage	Carrier not present	$\overline{CD}$	2.4			V
		Carrier present				0.4	V
	MUTE Input Voltage	Min to mute outputs	MUTE	2.0			V
		Max to force outputs active				0.8	V
I_{CC}	Supply Current				85		mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SDI}	Input Data Rate		SDI, $\overline{SDI}$	143		2970	Mbps
	Jitter for various Cable Lengths (with equalizer pathological)	270 Mbps, Belden 1694A, 0-350 meters (Note 4)				0.2	UI
		1.485 Gbps, Belden 1694A, 0-140 meters (Note 4)				0.25	UI
		2.97 Gbps, Belden 1694A, 0-100 meters (Note 4)				0.3	UI
		2.97 Gbps, Belden 1694A, 100-120 meters			0.4		UI
t_r,t_f	Output Rise Time, Fall Time	20% – 80%, (Note 4)	SDO, $\overline{SDO}$		90	130	ps
	Mismatch in Rise/Fall Time	(Note 4)			2	15	ps
t_{OS}	Output Overshoot	(Note 4)			1	5	%
R_{OUT}	Output Resistance	single-ended			50		Ω
RL_{IN}	Input Return Loss	5 MHz - 1.5 GHz, (Note 6)	SDI, $\overline{SDI}$	15			dB
		1.5 GHz - 3.0 GHz, (Note 6)		10			dB
R_{IN}	Input Resistance	single-ended			1.3		kΩ
C_{IN}	Input Capacitance	single-ended			1		pF

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.

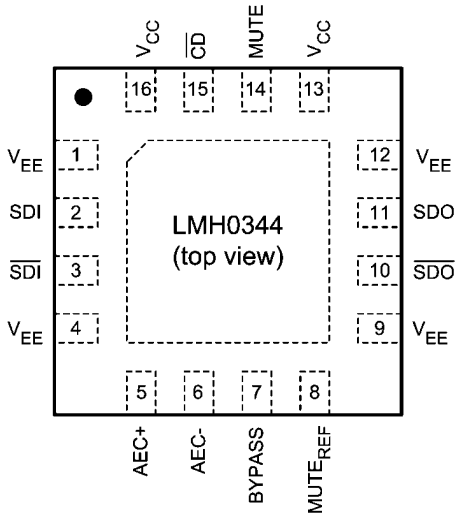
Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Note 4: Specification is guaranteed by characterization.

Note 5: The maximum input voltage swing assumes a nonstressing, DC-balanced signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.

Note 6: Input return loss is dependent on board design. The LMH0344 meets this specification on the SD344 evaluation board.

Connection Diagram



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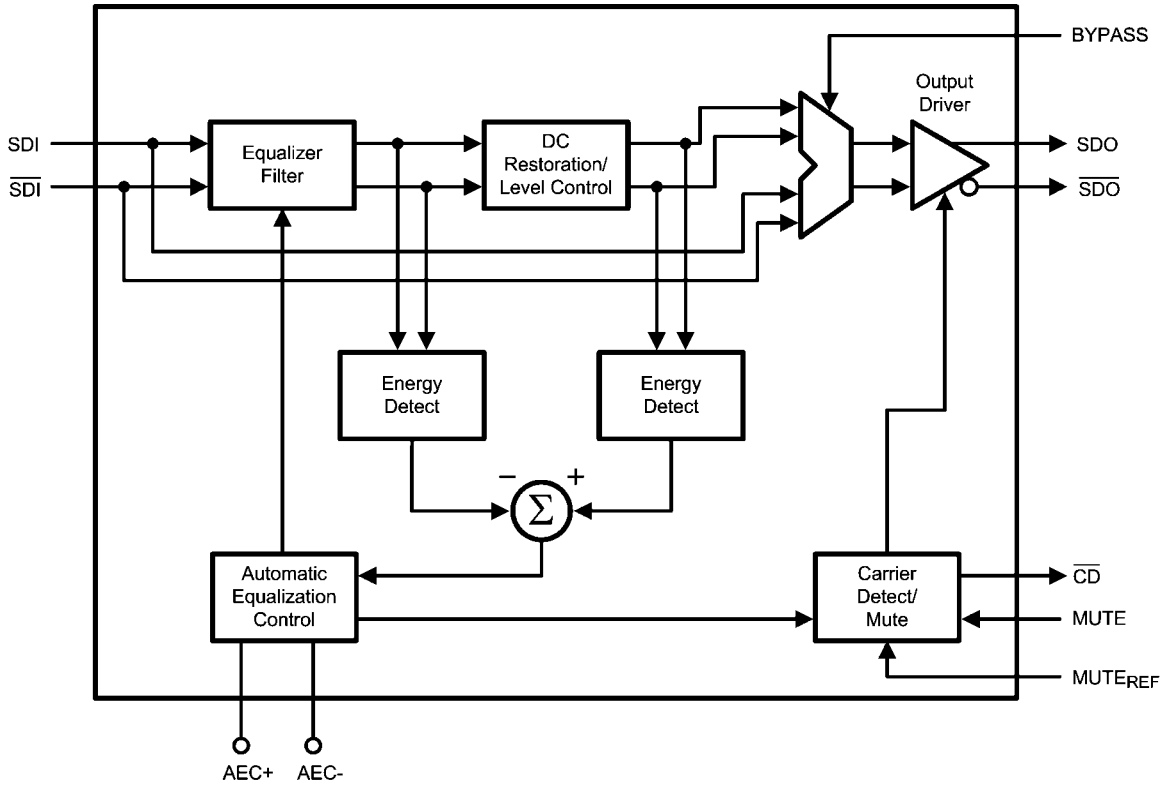
The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

16-Pin LLP
Order Number LMH0344SQ
See NS Package Number SQB16A

Pin Descriptions

Pin #	Name	Description
1	V_{EE}	Negative power supply (ground).
2	SDI	Serial data true input.
3	$\overline{SDI}$	Serial data complement input.
4	V_{EE}	Negative power supply (ground).
5	AEC+	AEC loop filter external capacitor (1µF) positive connection.
6	AEC-	AEC loop filter external capacitor (1µF) negative connection.
7	BYPASS	Bypasses equalization and DC restoration when high. No equalization occurs in this mode.
8	$MUTE_{REF}$	Mute reference. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be unconnected for maximum equalization.
9	V_{EE}	Negative power supply (ground).
10	$\overline{SDO}$	Serial data complement output.
11	SDO	Serial data true output.
12	V_{EE}	Negative power supply (ground).
13	V_{CC}	Positive power supply (+3.3V).
14	MUTE	Output mute. To disable the mute function and enable the output, MUTE must be tied to GND or a low level signal. To force the outputs to a muted state, tie to V_{CC}. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has no function in BYPASS mode.
15	$\overline{CD}$	Carrier detect. $\overline{CD}$ is high when no signal is present. $\overline{CD}$ has no function in BYPASS mode.
16	V_{CC}	Positive power supply (+3.3V).
DAP	V_{EE}	Connect exposed DAP to negative power supply (ground).

Block Diagram



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Device Operation

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1µF capacitor placed across the AEC+ and AEC- pins.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the **$\overline{\text{CD}}$** and **MUTE** signals along with **Mute Reference (MUTE_{REF})**.

The **Output Driver** produces SDO and $\overline{\text{SDO}}$.

MUTE REFERENCE (MUTE_{REF})

The mute reference sets the threshold for $\overline{\text{CD}}$ and (with $\overline{\text{CD}}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE_{REF} voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE_{REF} may be left unconnected for maximum equalization before muting.

CARRIER DETECT ($\overline{\text{CD}}$) AND MUTE

Carrier detect $\overline{\text{CD}}$ indicates if a valid signal is present at the LMH0344 input. If MUTE_{REF} is used, the carrier detect threshold will be altered accordingly. $\overline{\text{CD}}$ provides a high voltage when no signal is present at the LMH0344 input. $\overline{\text{CD}}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and $\overline{\text{SDO}}$. Applying a high input to MUTE will mute the LMH0344 outputs. Applying a low input will force the outputs to be active.

$\overline{\text{CD}}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

INPUT INTERFACING

The LMH0344 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The LMH0344 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The SDO and $\overline{\text{SDO}}$ outputs are internally loaded with 50Ω. They produce a 750 $\text{mV}_{\text{P-P}}$ differential output, or a 375 $\text{mV}_{\text{P-P}}$ single-ended output.

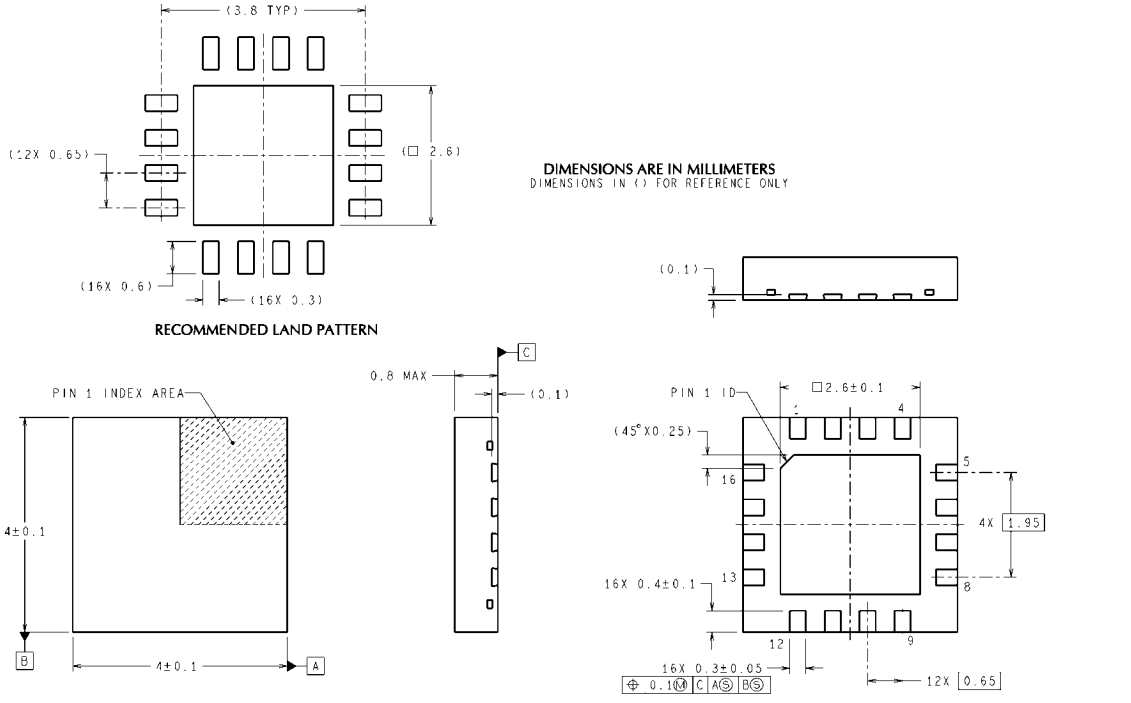
Application Information

PCB LAYOUT RECOMMENDATIONS

Please refer to the following Application Note on National's website: **AN-1372, "LMH0034 PCB Layout Techniques."**

The PCB layout techniques in the application note apply to the LMH0344 as well.

Physical Dimensions inches (millimeters) unless otherwise noted



SQB16A (Rev A)

16-Pin LLP
Order Number LMH0344SQ
NS Package Number SQB16A

Notes

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