



TRIPLE DIGITAL ISOLATORS

FEATURES

- 1, 25, and 150-Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew; 1 ns max
 - Low Pulse-Width Distortion (PWD); 2 ns max
 - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note [SLLA197](#) and [Figure 14](#))
- 4000-V_{peak} Isolation, 560-V_{peak} Working Voltage
- UL 1577 Certified
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see application note [SLLA181](#))
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

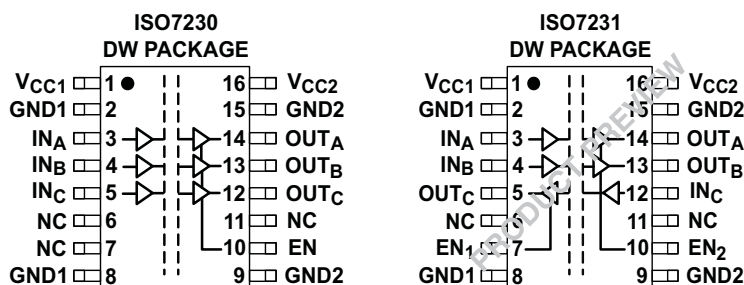
The ISO7230 and ISO7231 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO₂) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7230 triple-channel device has all three channels in the same direction while the ISO7231 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

The ISO7230A, ISO7230C, ISO7231A, and ISO7231C have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device, while the ISO7230M and ISO7231M have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter or the additional propagation delay.

In each device a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS. These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

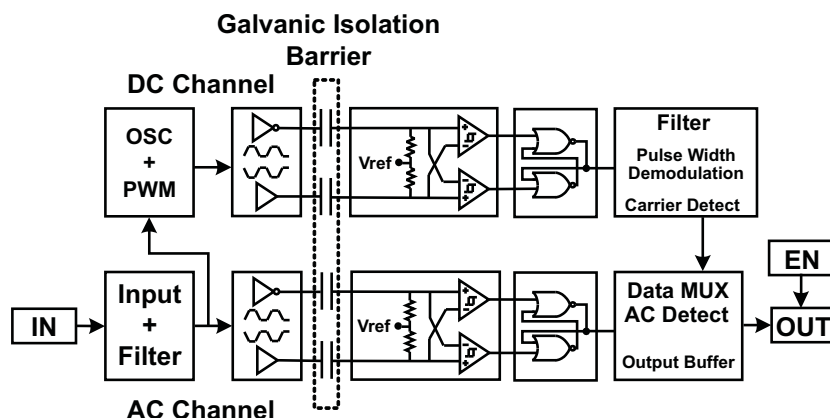


Table 1. Device Function Table ISO723x ⁽¹⁾

V _{CC1}	V _{CC2}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER
ISO7230ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	3/0	ISO7230A	ISO7230ADW (rail)
					ISO7230ADWR (reel)
ISO7230CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7230C	ISO7230CDW (rail)
					ISO7230CDWR (reel)
ISO7230MDW	150 Mbps	V _{CC} /2 (CMOS)	2/1	ISO7230M	ISO7230MDW (rail)
					ISO7230MDWR (reel)
ISO7231ADW ⁽¹⁾	1 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7231A	ISO7231ADW (rail)
					ISO7231ADWR (reel)
ISO7231CDW ⁽¹⁾	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7231C	ISO7231CDW (rail)
					ISO7231CDWR (reel)
ISO7231MDW ⁽¹⁾	150 Mbps	V _{CC} /2 (CMOS)		ISO7231M	ISO7231MDW (rail)
					ISO7231MDWR (reel)

(1) Product Preview

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

				VALUE	UNIT
V_{CC}	Supply voltage ⁽²⁾ , V_{CC1} , V_{CC2}			–0.5 to 6	V
V_I	Voltage at IN, OUT, EN			–0.5 to 6	V
I_O	Output current			±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	±1	
		Machine Model	ANSI/ESDS5.2-1996	±200	V
T_J	Maximum junction temperature			170	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

				MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage, V _{CC1} , V _{CC2}			4.5		5.5	V
				3		3.6	
I _{OH}	High-level output current			4			mA
I _{OL}	Low-level output current			−4			mA
t _{ui}	Input pulse width	ISO723xA		1			μs
		ISO723xC		40			ns
		ISO723xM		6.67	5		
1/t _{ui}	Signaling rate	ISO723xA		0	250	1000	kbps
		ISO723xC		0	30 ⁽¹⁾	25	Mbps
		ISO723xM		0	200 ⁽¹⁾	150	
V _{IH}	High-level input voltage (IN)		ISO723xM	0.7 V _{CC}			V
V _{IL}	Low-level input voltage (IN)			0			
V _{IH}	High-level input voltage (IN) (EN on all devices)		ISO723xA, ISO723xC	2			V
V _{IL}	Low-level input voltage (IN) (EN on all devices)			0			
T _J	Junction temperature			150			°C
H	External magnetic field-strength immunity per IEC 61000-4-8 & IEC 61000-4-9 certification			1000			A/m

- (1) Typical sigalling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS
 V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		1	3	mA
	ISO7230A	1 Mbps			1	3	
	ISO7230C/M	25 Mbps			7	9.5	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA
	ISO7231A	1 Mbps				TBD	
	ISO7231C/M	25 Mbps				TBD	
I _{CC2}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		15	22	mA
	ISO7230A	1 Mbps			16	22	
	ISO7230C/M	25 Mbps			17	24	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA
	ISO7231A	1 Mbps				TBD	
	ISO7231C/M	25 Mbps				TBD	
ELECTRICAL CHARACTERISTICS							
I _{OFF}	Sleep mode output current	EN at V _{CC} , Single channel		0			μA
V _{OH}	High-level output voltage	I _{OH} = −4 mA, See Figure 1		V _{CC} − 0.4			V
		I _{OH} = −20 μA, See Figure 1		V _{CC} − 0.1			
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, See Figure 1				0.4	V
		I _{OL} = 20 μA, See Figure 1				0.1	
V _{I(HYS)}	Input voltage hysteresis			150			mV
I _{IH}	High-level input current	IN from 0 V to V _{CC}				10	μA
I _{IL}	Low-level input current			−10			
C _I	Input capacitance to ground	IN at V _{CC} , V _I = 0.4 sin (4E6πt)		1			pF
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V, See Figure 4		25	50		kV/μs

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	40		80	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				10	
t_{PLH} , t_{PHL}	Propagation delay		18		42	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				2.5	ns
t_{PLH} , t_{PHL}	Propagation delay		10		22	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	2	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO723xA/C			9	ns
		ISO723xM		0		
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO723xA/C		0	2	ns
		ISO723xM		0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM 150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I _{CC1}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V			1	3	mA
	ISO7230A	1 Mbps				1	3	
	ISO7230C/M	25 Mbps				7	9.5	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V				TBD	mA
	ISO7231A	1 Mbps					TBD	
	ISO7231C/M	25 Mbps					TBD	
I _{CC2}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V			9	15	mA
	ISO7230A	1 Mbps				9.5	15	
	ISO7230C/M	25 Mbps				10	17	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V				TBD	mA
	ISO7231A	1 Mbps					TBD	
	ISO7231C/M	25 Mbps					TBD	
ELECTRICAL CHARACTERISTICS								
I _{OFF}	Sleep mode output current	EN at V _{CC} , Single channel			0			μA
V _{OH}	High-level output voltage	I _{OH} = −4 mA, See Figure 1		ISO7230	V _{CC} − 0.4		V	
				ISO7231 (5-V side)	V _{CC} − 0.8			
		I _{OH} = −20 μA, See Figure 1			V _{CC} − 0.1			
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, See Figure 1			0.4		V	
		I _{OL} = 20 μA, See Figure 1			0.1			
V _{I(HYS)}	Input voltage hysteresis				150		mV	
I _{IH}	High-level input current	IN from 0 V to V _{CC}			10		μA	
I _{IL}	Low-level input current				−10			
C _I	Input capacitance to ground	IN at V _{CC} , V _I = 0.4 sin (4E6πt)			1		pF	
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V, See Figure 4			25	50	kV/μs	

SWITCHING CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	40		80	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				11	
t_{PLH} , t_{PHL}	Propagation delay, low-to-high-level output		20		46	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				3	
t_{PLH} , t_{PHL}	Propagation delay, low-to-high-level output		12		28	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	2	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO723xA/C			7.5	ns
		ISO723xM		0		
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO723xA/C		0	2.5	ns
		ISSO723xM		0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM 150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also known as pulse skew

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3-V, V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I _{CC1}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		0.5		1	mA
	ISO7230A	1 Mbps			1		2	
	ISO7230C/M	25 Mbps			3		5	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA	
	ISO7231A	1 Mbps				TBD		
	ISO7231C/M	25 Mbps				TBD		
I _{CC2}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V		15		22	mA
	ISO7230A	1 Mbps			16		22	
	ISO7230C/M	25 Mbps			17		24	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA	
	ISO7231A	1 Mbps				TBD		
	ISO7231C/M	25 Mbps				TBD		
ELECTRICAL CHARACTERISTICS								
I _{OFF}	Sleep mode output current		EN at V _{CC} , Single channel		0			μA
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	ISO7230	V _{CC} − 0.4			V
				ISO7231 (5-V side)	V _{CC} − 0.8			
			I _{OH} = −20 μA, See Figure 1		V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1				0.4	V
			I _{OL} = 20 μA, See Figure 1				0.1	
V _{I(HYS)}	Input voltage hysteresis				150			mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}				10	μA
I _{IL}	Low-level input current				−10			
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		1			pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 4		25	50		kV/μs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3-V and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	40		80	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				11	
t_{PLH} , t_{PHL}	Propagation delay		22		51	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				3	
t_{PLH} , t_{PHL}	Propagation delay		12		26	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	2	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO723xA/C			10	ns
		ISO723xM		0		
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO723xA/C		0	2.5	ns
		ISO723xM		0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1	ns

- (1) Also known as pulse skew
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₂ at 3 V		0.5	1	mA
	ISO7230A	1 Mbps			1	2	
	ISO7230C/M	25 Mbps			3	5	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA
	ISO7231A	1 Mbps				TBD	
	ISO7231C/M	25 Mbps				TBD	
I _{CC2}	ISO7230A/C/M	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₂ at 3 V		9	15	mA
	ISO7230A	1 Mbps			9.5	15	
	ISO7230C/M	25 Mbps			10	17	
	ISO7231A/C/M	Quiescent	V _I = V _{CC} or 0 V, all channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			TBD	mA
	ISO7231A	1 Mbps				TBD	
	ISO7231C/M	25 Mbps				TBD	
ELECTRICAL CHARACTERISTICS							
I _{OFF}	Sleep mode output current		EN at V _{CC} , single channel		0		μA
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 1	V _{CC} − 0.4			V
			I _{OH} = −20 μA, See Figure 1	V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1			0.4	V
			I _{OL} = 20 μA, See Figure 1			0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V or V _{CC}			10	μA
I _{IL}	Low-level input current				−10		
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 4	25	50		kV/μs

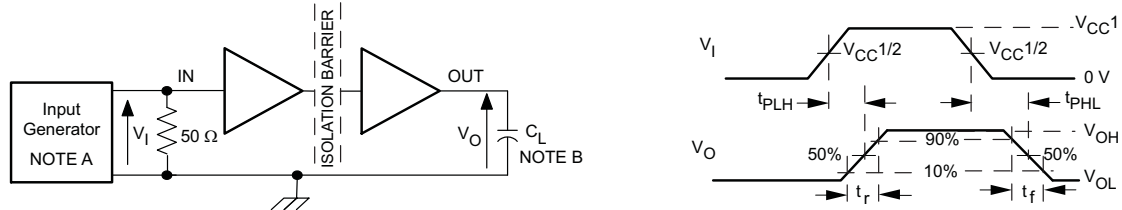
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	45		85	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				12	
t_{PLH} , t_{PHL}	Propagation delay		25		56	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				4	
t_{pLH} , t_{pHL}	Propagation delay		12		32	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{pHL} - t_{pLH} $			1	2	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO723xA/C			9	ns
		ISO723xM		0		
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO723xA/C		0	3	ns
		ISO723xM		0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2	15		20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		15		20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		15		20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output		15		20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM		1		ns

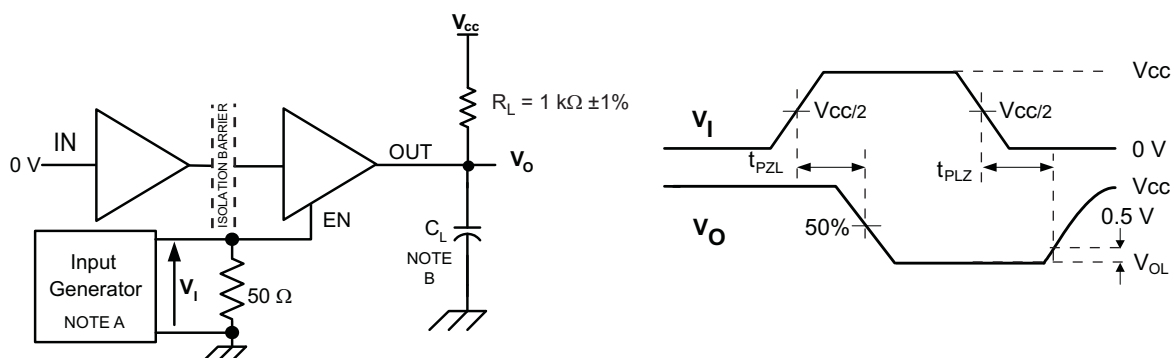
- (1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

PARAMETER MEASUREMENT INFORMATION



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

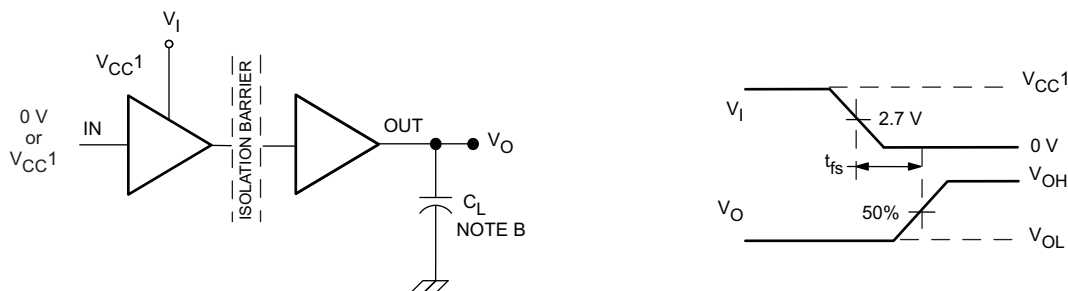
Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

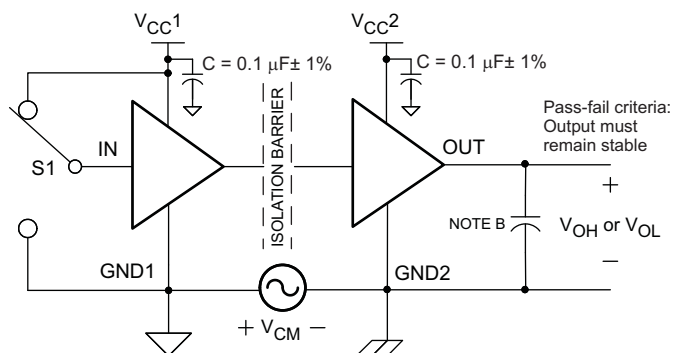
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



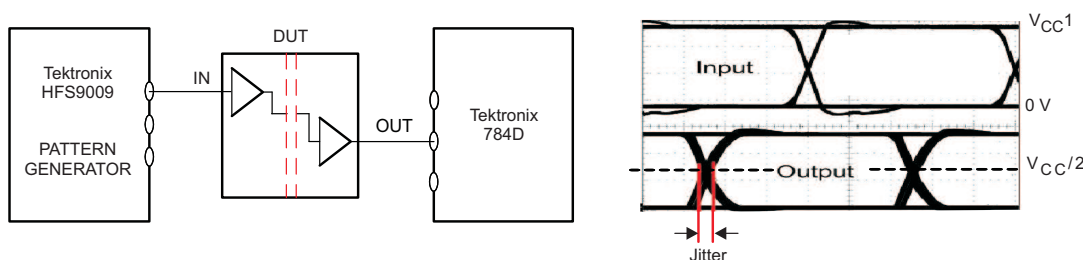
- The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_0 = 50 \Omega$.
- $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_0 = 50 \Omega$.
- $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Pek Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

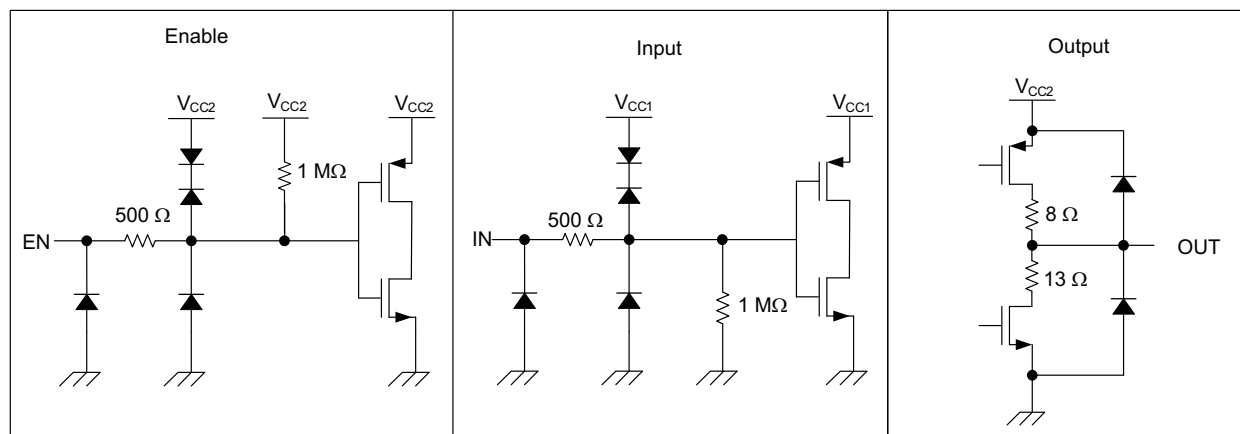
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	7.7			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R _{IO}	Isolation resistance	Input to output, V _{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T _A < 100°C		>10 ¹²		Ω
		Input to output, V _{IO} = 500 V, 100°C ≤ T _A ≤ T _A max		>10 ¹¹		Ω
C _{IO}	Barrier capacitance Input to output	V _I = 0.4 sin (4E6πt)		1		pF
C _I	Input capacitance to ground	V _I = 0.4 sin (4E6πt)		1		pF

REGULATORY INFORMATION

UL
Recognized under 1577 Component Recognition Program ⁽¹⁾
File Number: E181974

- (1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		168		°C/W
	High-K Thermal Resistance		96.1		
θ_{JB} Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC} Junction-to-Case Thermal Resistance			48		°C/W
P_D Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

**3.3-V RMS SUPPLY CURRENT
VS
SIGNALING RATE**

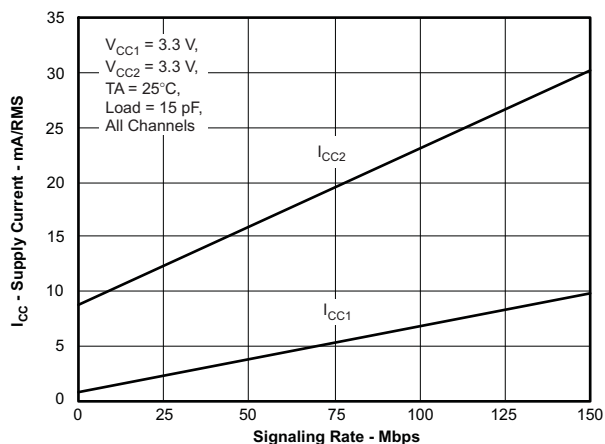


Figure 6.

**5-V RMS SUPPLY CURRENT
VS
SIGNALING RATE**

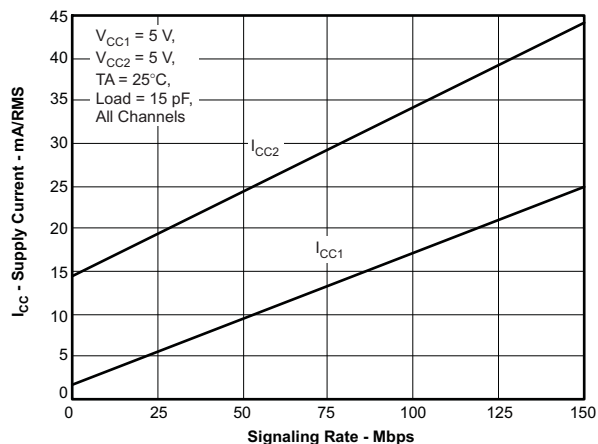


Figure 7.

**PROPAGATION DELAY
VS
FREE-AIR TEMPERATURE**

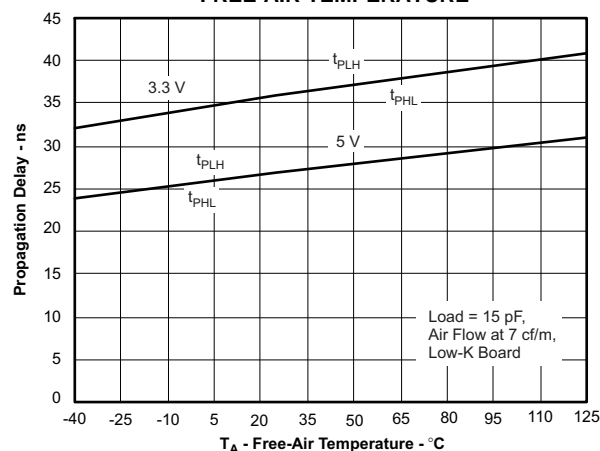


Figure 8.

**INPUT THRESHOLD VOLTAGE
VS
FREE-AIR TEMPERATURE**

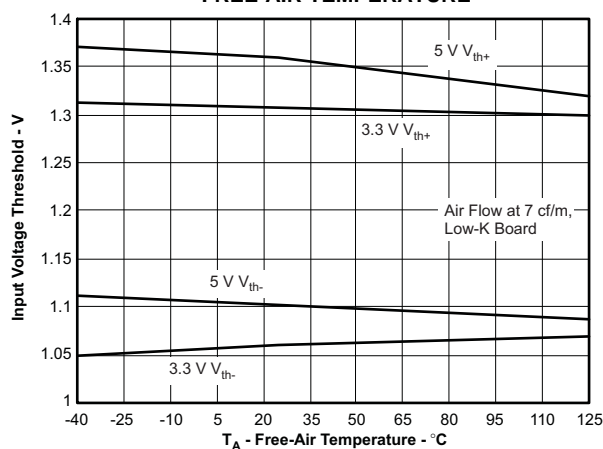
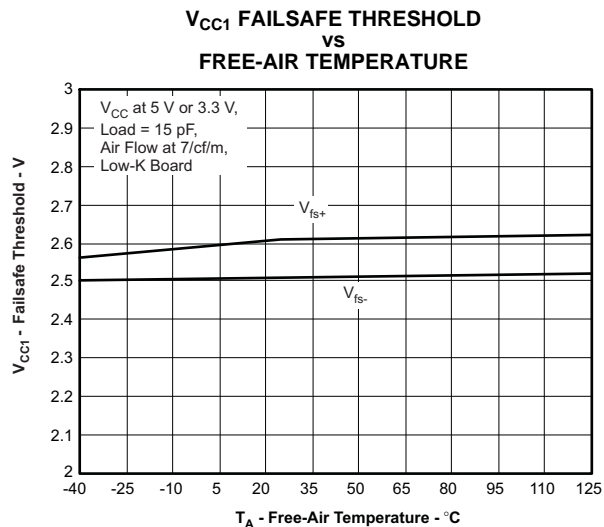
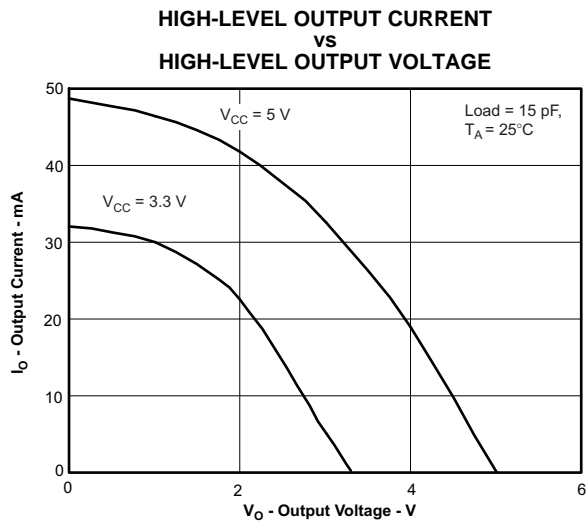
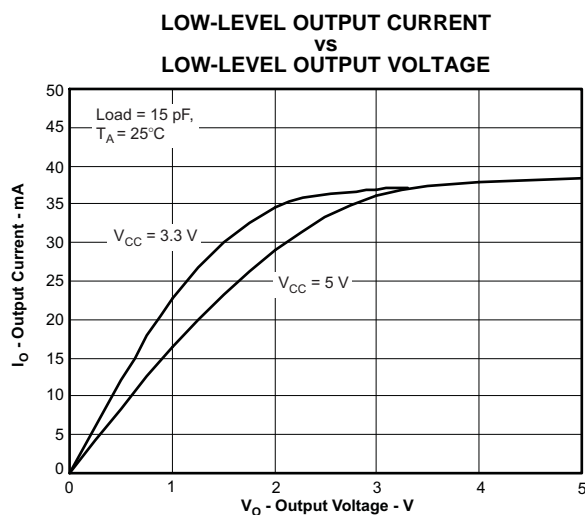


Figure 9.

TYPICAL CHARACTERISTIC CURVES (continued)**Figure 10.****Figure 11.****Figure 12.**

APPLICATION INFORMATION

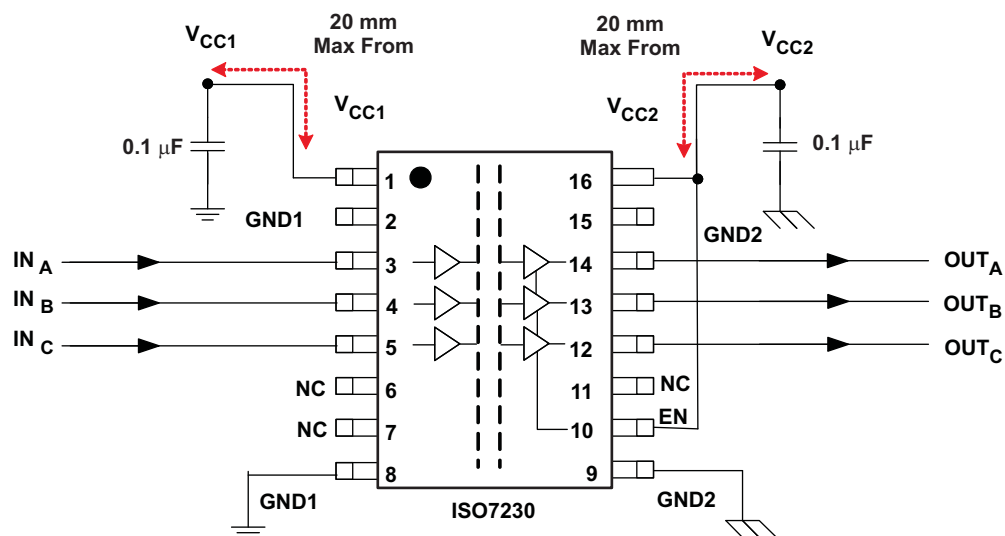


Figure 13. Typical ISO723x Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

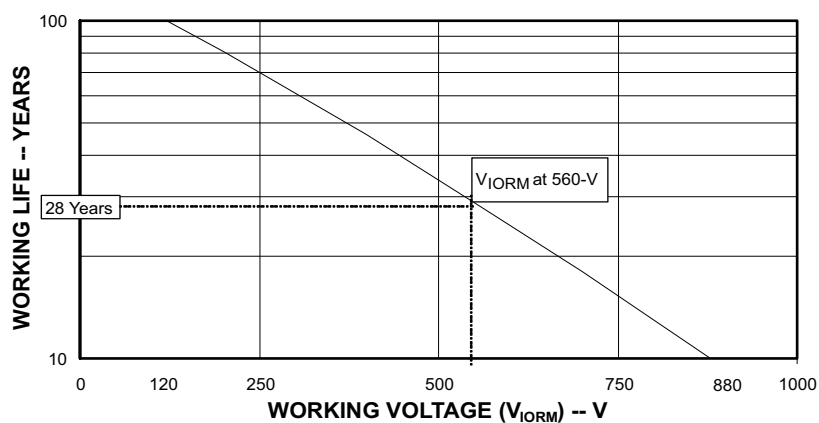
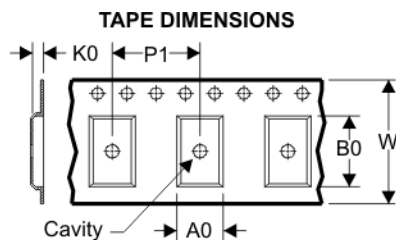
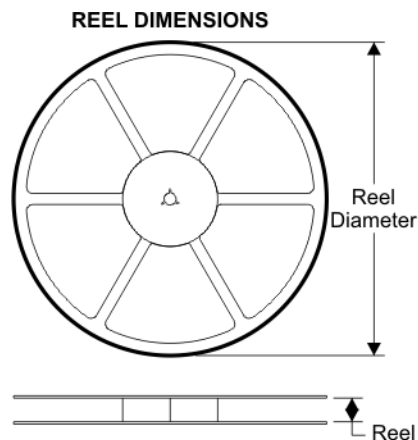


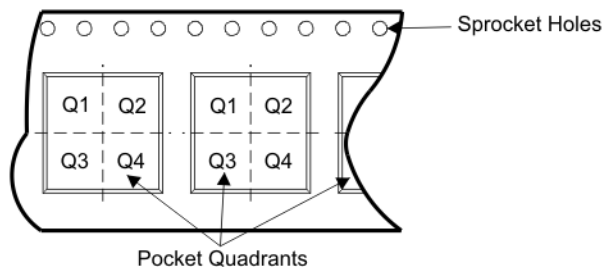
Figure 14. Time Dependant Dielectric Breakdown Testing Results

TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230ADWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7230CDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7230MDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1

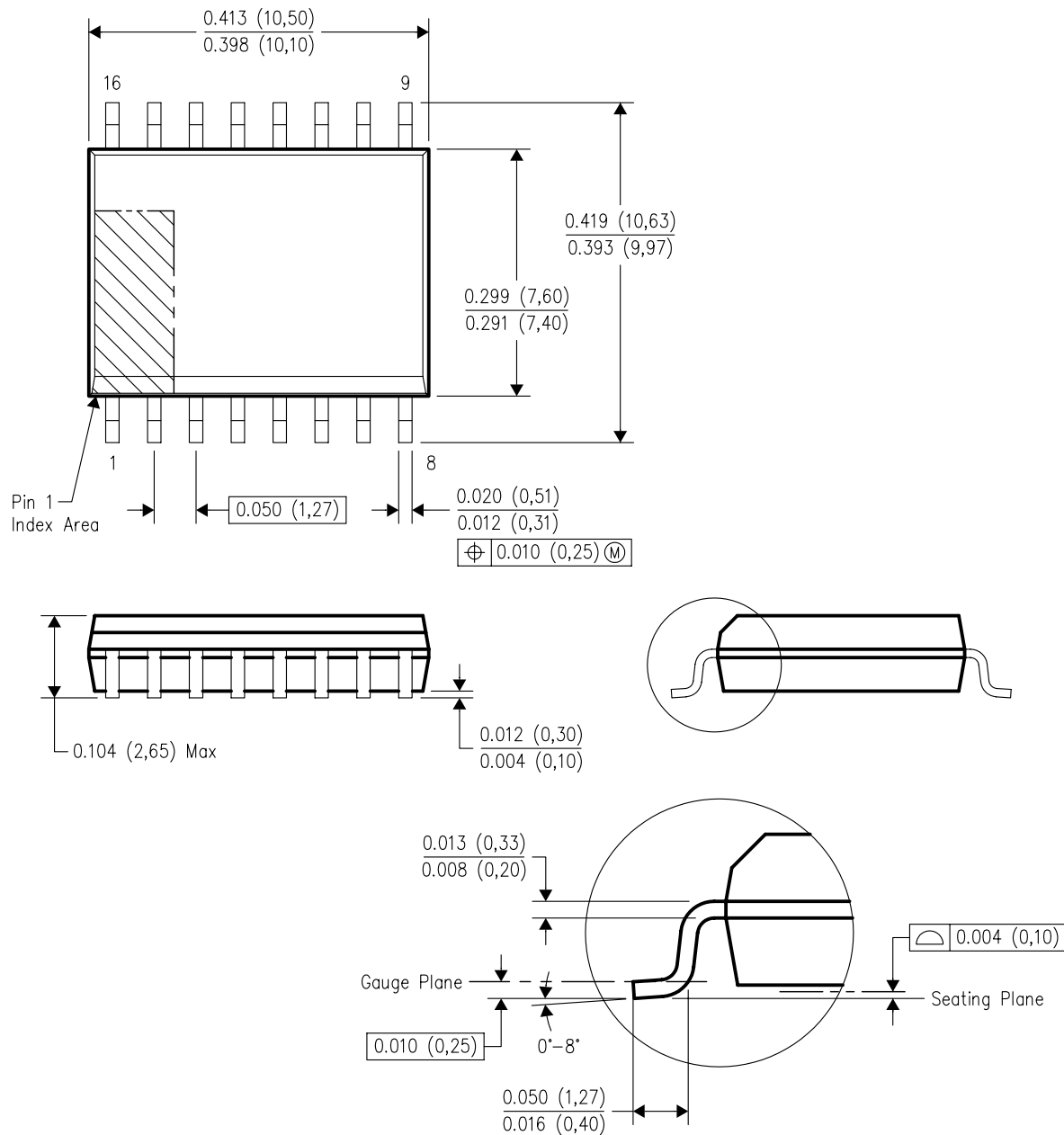
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ISO7230ADWR	DW	16	SITE 35	406.0	348.0	0.0
ISO7230CDWR	DW	16	SITE 35	406.0	348.0	0.0
ISO7230MDWR	DW	16	SITE 35	406.0	348.0	0.0

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
Low Power Wireless	www.ti.com/lpw

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated