CS42324

10-In, 6-Out, 2 Vrms Audio CODEC

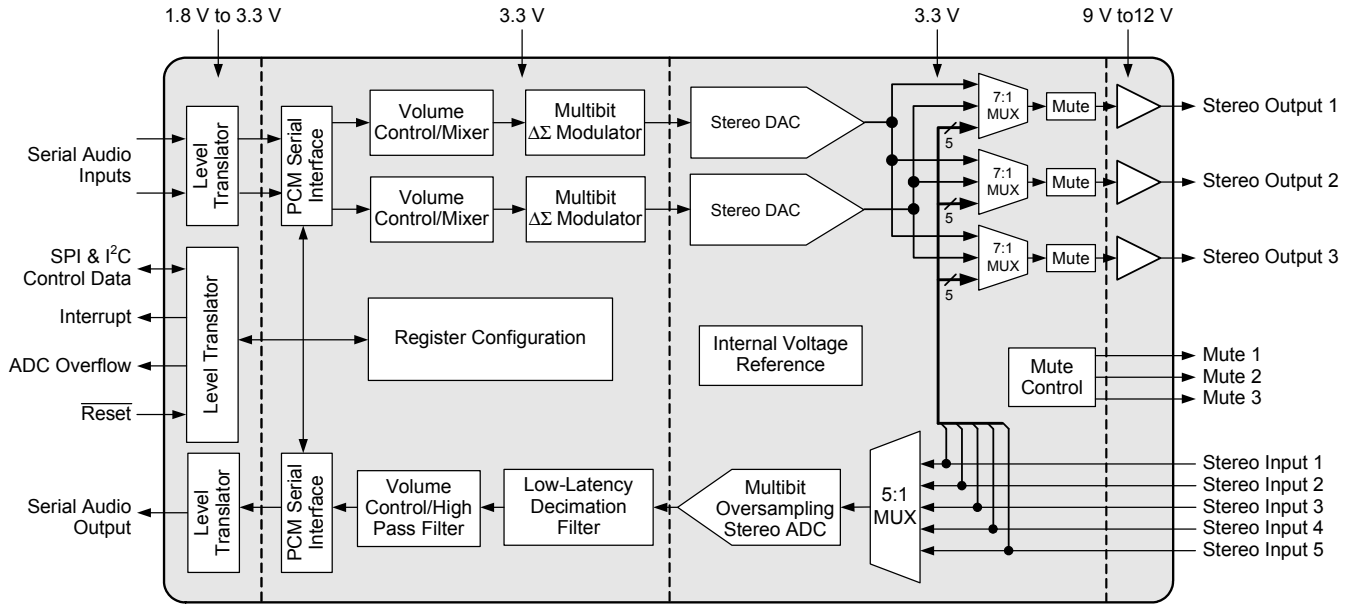
D/A Features

- Dual 24-bit Stereo DACs
- Multi-bit Delta-Sigma Modulator
- 100 dB Dynamic Range (A-Wtd)
- -90 dB THD+N
- Integrated Line Driver
  - 2 Vrms Output
  - Single-Ended Outputs
- Up to 96 kHz Sampling Rates
- Stereo 7:1 Output Multiplexer
- Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing Click-Free Transitions
- Selectable Serial Audio Interface Formats
  - Left- or Right-Justified, Up to 24-bit
  - I²S Up to 24-bit
- Selectable 50/15 µs De-Emphasis
- Internal Analog Mute
- Control Output for External Muting
- Popguard® Technology

A/D Features

- Multi-bit Delta-Sigma Modulator
- 24-bit Conversion
- Up to 96 kHz Sampling Rates
- 95 dB Dynamic Range (A-Wtd)
- -88 dB THD+N
- Stereo 5:1 Input Multiplexer
- Digital Volume Control with Soft Ramp
  - 0.5 dB Step Size
- Selectable Serial Audio Interface Formats
  - Left-Justified
  - I²S
- High-Pass Filter or DC Offset Calibration

See System Features, General Description, and Ordering information on page 2.



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

System Features

- Direct Interface with 1.8 V to 3.3 V Logic Levels
- Supports Asynchronous Serial Port Operation
  - Two Independent Clock Domains
  - ADC, DAC1, and DAC2 can be Independently Assigned to the Two Clock Domains
  - Each Serial Port Supports Master or Slave Operation
- Internal Digital Loopback
- +3.3 V Analog Power Supply
- +3.3 V Digital Power Supply
- +9 V to +12 V High-Voltage Power Supply
- Hardware or Software Mode Configuration
  - Supports I²C® and SPI™ Software Interface

General Description

The CS42324 is a highly integrated stereo audio CODEC. The CS42324 performs stereo analog-to-digital (A/D) and up to four channels of digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 96 kHz.

A 5:1 stereo input multiplexer is included for selecting between line-level inputs. The output of the input multiplexer is followed by an advanced 3rd-order, multi-bit delta-sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 96 kHz, in either Slave or Master Mode.

The D/A converter is based on a 5th-order multi-bit delta-sigma modulator with an ultra-linear low-pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

An integrated 7:1 stereo output multiplexer on each of the three stereo 2 Vrms line-level outputs is used to select any of the 5 stereo analog inputs, for analog bypass support, or the outputs of the 2 internal DACs. Each 2 Vrms output can be muted with the selectable analog mute function.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated digital level translators allow easy interfacing between the CS42324 and other devices operating over a wide range of logic levels.

The CS42324 is available in a 48-pin LQFP package in Commercial (-40° to +85° C) and Automotive (-40° to +105° C) grades. The CDB42324 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering information" on page 71 for complete details.

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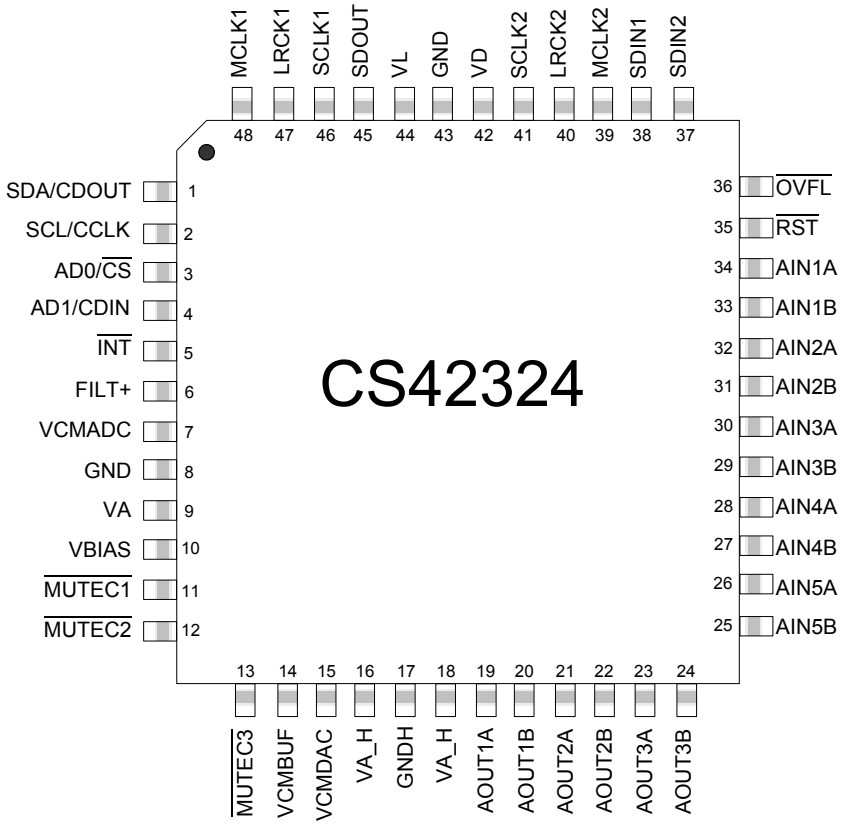
1. PIN DESCRIPTIONS

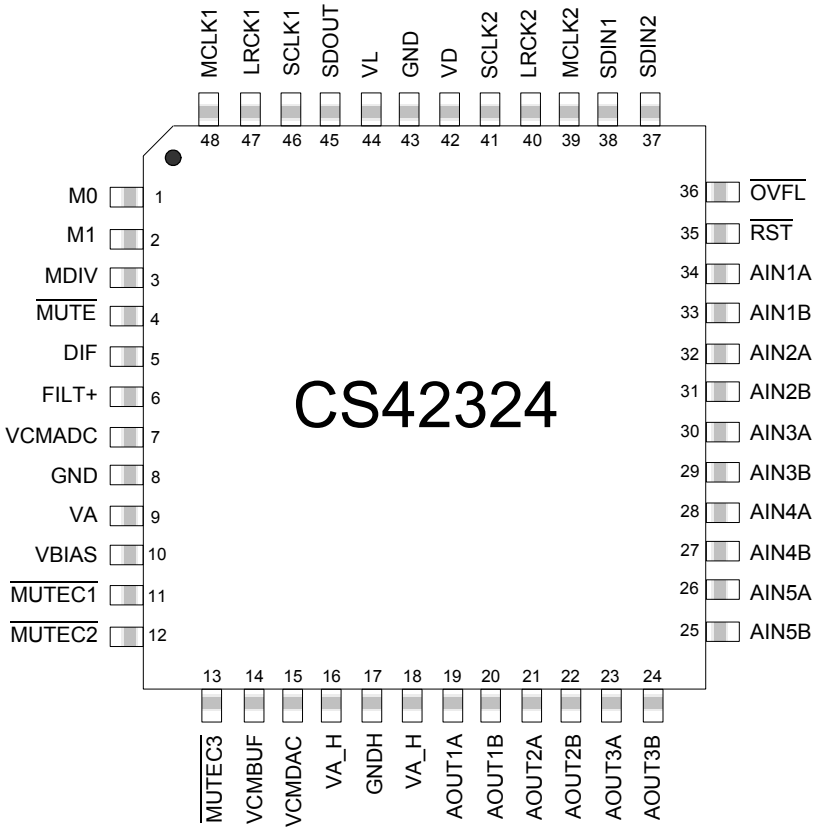
1.1 Software Mode



Pin Name	#	Pin Description
SDA/CDOUT	1	**I²C Format SDA** (*Input/Output*) - Acts as an input/output data pin. **SPI Format CDOUT** (*Output*) - Acts as an output only data pin.
SCL/CCLK	2	**I²C Format, SCL** (*Input*) - Acts as the serial clock output from the CS42324. **SPI Format, CCLK** (*Input*) - Acts as the serial clock output from the CS42324.
AD0/$\overline{CS}$	3	**I²C Format, AD0** (*Input*) - Forms the device address input AD[0]. **SPI Format, CS** (*Input*) - Acts as the active low chip select input.
AD1/CDIN	4	**I²C Format, AD1** (*Input*) - Forms the device address input AD[1]. **SPI Format, CDIN** (*Input*) - Becomes the input data pin.
$\overline{INT}$	5	**Interrupt** (*Output*) - Indicates an interrupt condition has occurred.
FILT+	6	**FILT+** (*Output*) - Full-scale reference voltage for ADC.
VCMADC	7	**ADC Common-Mode Voltage** (*Output*) - Filter connections for the ADC internal quiescent reference voltage.
GND	8	**Analog Ground** (*Input*) - Analog ground reference.
VA	9	**Analog Power** *(Input)* - Positive power for the internal analog section.
VBIAS	10	**Bias Voltage** (*Output*) - Positive reference voltage for the internal DAC.
$\overline{MUTEC1}$	11	**Mute Control 1** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.

$\overline{\text{MUTEC2}}$	12	**Mute Control 2** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
$\overline{\text{MUTEC3}}$	13	**Mute Control 3** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
VCMBUF	14	**VCMBUF** (*Output*) - Internally buffered VCMDAC
VCMDAC	15	**DAC Common-Mode Voltage** (*Output*) - Filter connections for the DAC internal quiescent reference voltage.
VA_H	16 18	**Analog High Voltage Power** *(Input)* - Positive power for the internal output buffer section.
GNDH	17	**Analog Ground** (*Input*) - Ground reference for high-voltage section.
AOUT1A, AOUT1B AOUT2A, AOUT2B AOUT3A, AOUT3B	19, 20 21, 22 23, 24	**DAC Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AIN5B, AIN5A AIN4B, AIN4A AIN3B, AIN3A AIN2B, AIN2A AIN1B, AIN1A	25, 26 27, 28 29, 30 31, 32 33, 34	**Stereo Analog Inputs 1-5** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
$\overline{\text{OVFL}}$	36	**ADC Overflow** (*Output*) - Indicates an ADC overflow condition is present.
SDIN2 SDIN1	37 38	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
MCLK2	39	**Master Clock 2** (*Input*) - Optional asynchronous clock source for the DAC's delta-sigma modulators.
LRCK2	40	**Serial Port 2 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio input data line.
SCLK2	41	**Serial Port 2 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 2.
VD	42	**Digital Power** (*Input*) - Positive power for the internal digital section.
GND	43	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VL	44	**Digital Interface Power** (*Input*) - Determines the required signal level for the control and serial port interfaces as shown in "I/O Power Rails" on page 12. Refer to the"Recommended Operating Conditions" on page 13 for appropriate voltages.
SDOUT	45	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK1	46	**Serial Port 1 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 1.
LRCK1	47	**Serial Port 1 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio output data line.
MCLK1	48	**Master Clock 1** (*Input*) - Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.

1.2 Hardware Mode



Pin Name	#	Pin Description
M0, M1	1, 2	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MDIV	3	**MCLK Divider** (*Input*) - Setting this pin high places a divide-by-2 circuit in the MCLK path to the core device circuitry.
$\overline{\text{MUTE}}$	4	**$\overline{\text{MUTE}}$** (*Input*) - Engages the internal digital mute and activates the $\overline{\text{MUTECx}}$ pins
DIF	5	**DIF** (*Input*) - Sets the serial audio interface format. Setting DIF high selects I²S audio format and low selects LJ audio format.
FILT+	6	**FILT+** (*Output*) - Full-scale reference voltage for ADC.
VCMADC	7	**ADC Common-Mode Voltage** (*Output*) - Filter connections for the ADC internal quiescent reference voltage.
GND	8	**Analog Ground** (*Input*) - Analog ground reference.
VA	9	**Analog Power** *(Input)* - Positive power for the internal analog section.
VBIAS	10	**Bias Voltage** (*Output*) - Positive reference voltage for the internal DAC.
$\overline{\text{MUTEC1}}$	11	**Mute Control 1** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
$\overline{\text{MUTEC2}}$	12	**Mute Control 2** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.

$\overline{\text{MUTEC3}}$	13	**Mute Control 3** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
VCMBUF	14	**VCMBUF** (*Output*) - Internally buffered VCMDAC
VCMDAC	15	**DAC Common-Mode Voltage** (*Output*) - Filter connections for the DAC internal quiescent reference voltage.
VA_H	16, 18	**Analog High Voltage Power** *(Input)* - Positive power for the internal output buffer section.
GNDH	17	**Analog Ground** (*Input*) - Ground reference for high-voltage section.
AOUT1A, AOUT1B AOUT2A, AOUT2B AOUT3A, AOUT3B	19, 20 21, 22 23, 24	**DAC Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AIN5B, AIN5A AIN4B, AIN4A AIN3B, AIN3A AIN2B, AIN2A AIN1B, AIN1A	25, 26 27, 28 29, 30 31, 32 33, 34	**Stereo Analog Inputs 1-5** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
$\overline{\text{OVFL}}$	36	**ADC Overflow** (*Output*) - Indicates an ADC overflow condition is present.
SDIN2 SDIN1	37 38	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
MCLK2	39	**Master Clock 2** (*Input*) - Optional asynchronous clock source for the DAC's delta-sigma modulators.
LRCK2	40	**Serial Port 2 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio input data line.
SCLK2	41	**Serial Port 2 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 2.
VD	42	**Digital Power** (*Input*) - Positive power for the internal digital section.
GND	43	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VL	44	**Digital Interface Power** (*Input*) - Determines the required signal level for the control and serial port interfaces as shown in "I/O Power Rails" on page 12. Refer to the"Recommended Operating Conditions" on page 13 for appropriate voltages
SDOUT	45	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK1	46	**Serial Port 1 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 1.
LRCK1	47	**Serial Port 1 Left Right/Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio output data line.
MCLK1	48	**Master Clock 1** (*Input*) - Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.

1.3 Digital I/O Pin Characteristics

The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
Software Mode					
VL	1	SDA CDOUT	Input/Output Hi-Z/Output	1.8 V - 3.3 V, Open Drain 1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V, with Hysteresis
	2	SCL CCLK	Input	-	1.8 V - 3.3 V, with Hysteresis
	3	AD0 $\overline{CS}$	Input	-	1.8 V - 3.3 V, with Hysteresis
	4	AD1 CDIN	Input	-	1.8 V - 3.3 V, with Hysteresis
	5	INT	Output	1.8 V - 3.3 V, Open Drain	1.8 V - 3.3 V, with Hysteresis
Hardware Mode					
VL	1	M0	Input	-	1.8 V - 3.3 V, with Hysteresis
	2	M1	Input	-	1.8 V - 3.3 V, with Hysteresis
	3	MDIV	Input	-	1.8 V - 3.3 V, with Hysteresis
	4	MUTE	Input	-	1.8 V - 3.3 V, with Hysteresis
	5	DIF	Input	-	1.8 V - 3.3 V, with Hysteresis
All Modes					
VL	35	$\overline{RST}$	Input	-	1.8 V - 3.3 V
	47 40	LRCK1 LRCK2	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	46 41	SCLK1 SCLK2	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	48 39	MCLK1 MCLK2	Input	-	1.8 V - 3.3 V
	38 37	SDIN1 SDIN2	Input	-	1.8 V - 3.3 V
	45	SDOUT	Output	1.8 V - 3.3 V, CMOS	-
	36	OVFL	Output	1.8 V - 3.3 V, Open Drain	-
VA_H	11 12 13	MUTEC1 MUTEC2 MUTEC3	Output	9.0 V - 12.0 V	-

Table 1. I/O Power Rails

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = GNDH = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.13	3.3	3.47	V
	Digital	VD	3.13	3.3	3.47	V
	Logic	VL	1.71	3.3	3.47	V
	High Voltage Analog	VA_H	8.55	9.0	12.60	V
Ambient Operating Temperature (Power Applied)						
	Commercial(-CQZ)	T_A	-40	-	+85	°C
	Automotive(-DQZ)		-40	-	+105	°C

ABSOLUTE MAXIMUM RATINGS

GND = GNDH = 0 V; All voltages with respect to ground. (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+4.50	V
	Digital	VD	-0.3	+4.50	V
	Logic	VL	-0.3	+4.50	V
	High Voltage Analog	VA_H	-0.3	+17.0	V
Input Current	(Note 2)	I_{in}	-10	+10	mA
Analog Input Voltage		V_{INA}	GND - 0.3	VA_H + 0.3	V
Digital Input Voltage	Logic	V_{IND}	-0.3	VL + 0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS - COMMERCIAL (-CQZ)

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V, VA_H = 9 V, GND = GNDH = 0 V; T_A = 25° C; 997 Hz Full-Scale Output Sine Wave. Decoupling capacitors, Filter capacitors, and Recommended output filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Range		(Note 3)					
	18 to 24-Bit	A-weighted		94	100	-	dB
		unweighted		91	97	-	dB
	16-Bit	A-weighted		88	93	-	dB
		unweighted		85	90	-	dB
Total Harmonic Distortion + Noise		(Note 3)					
	18 to 24-Bit	0 dB		-	-90	-84	dB
		-20 dB		-	-77	-73	dB
		-60 dB	THD+N	-	-37	-33	dB
	16-Bit	0 dB		-	-87	-82	dB
		-20 dB		-	-77	-62	dB
		-60 dB		-	-37	-22	dB
Interchannel Isolation		(1 kHz)		-	-100	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full-Scale Output Voltage				1.9	2.0	2.1	V_{rms}
Max current draw from an AOUT pin			I_{OUT}	-	575	-	µA
AC-Load Resistance		(Note 4)	R_L	5	-	-	kΩ
Load Capacitance		(Note 4)	C_L	-	-	100	pF
Output Impedance			Z_{OUT}	-	50	-	Ω

Notes: 3. One-half LSB of triangular PDF dither added to data.

4. See Figures 1 and 2 on page 16. R_L and C_L reflect the minimum resistance and maximum capacitance allowed in order to maintain stability in the internal op-amp. C_L affects the dominant pole of the internal output amp; increasing C_L beyond 100 pF can cause the internal op-amp to become unstable.

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DQZ)

Test Conditions (unless otherwise specified): VA = 3.13 V to 3.47 V, VD = 3.13 V to 3.47 V, VL = 1.71 V to 3.47 V, VA_H = 8.55 V to 12.60 V, GND = GNDH = 0 V; T_A = -40° C to +85° C; 997 Hz Full-Scale Output Sine Wave. Decoupling capacitors, filter capacitors, and recommended output filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Range		(Note 3)					
	18 to 24-Bit	A-weighted		90	100	-	dB
		unweighted		87	97	-	dB
	16-Bit	A-weighted		83	93	-	dB
		unweighted		80	90	-	dB
Total Harmonic Distortion + Noise		(Note 3)					
	18 to 24-Bit	0 dB		-	-90	-80	dB
		-20 dB		-	-77	-67	dB
		-60 dB	THD+N	-	-37	-27	dB
	16-Bit	0 dB		-	-87	-77	dB
		-20 dB		-	-77	-67	dB
		-60 dB		-	-37	-27	dB
Interchannel Isolation		(1 kHz)		-	-100	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full-Scale Output Voltage				1.9	2.0	2.1	V_{rms}
Max current draw from an AOUT pin			I_{OUT}	-	575	-	µA
AC-Load Resistance		(Note 4)	R_L	5	-	-	kΩ
Load Capacitance		(Note 4)	C_L	-	-	100	pF
Output Impedance			Z_{OUT}	-	50	-	Ω

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 5)		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 6)	to -0.01 dB corner to -3 dB corner		0 0	- -	.454 .499	Fs Fs
Frequency Response (10 Hz to 20 kHz)			-0.01	-	+0.01	dB
StopBand			0.547	-	-	Fs
StopBand Attenuation	(Note 6)		102	-	-	dB
Group Delay		tgd	-	9.4/Fs	-	s
De-emphasis Error (Note 7)	Fs = 44.1 kHz		-	-	+/-0.14	dB
Double-Speed Mode						
Passband (Note 6)	to -0.01 dB corner to -3 dB corner		0 0	- -	.43 .499	Fs Fs
Frequency Response (10 Hz to 20 kHz)			-0.01	-	+0.01	dB
StopBand			.583	-	-	Fs
StopBand Attenuation	(Note 6)		80	-	-	dB
Group Delay		tgd	-	4.6/Fs	-	s

Notes: 5. Response is clock-dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 31 to 42) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

6. For Single-Speed Mode, the measurement bandwidth is from StopBand to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is from StopBand to 3 Fs.

7. De-emphasis is available only in Single-Speed Mode.

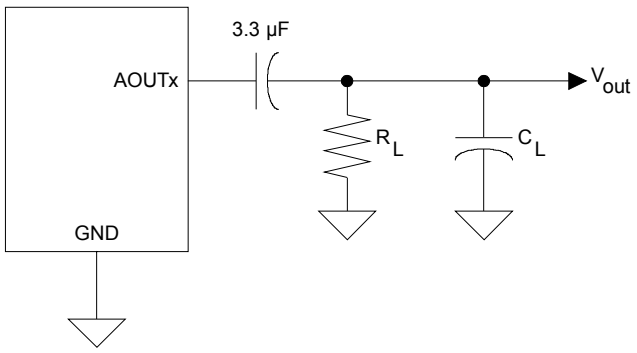


Figure 1. Equivalent Analog Output Load

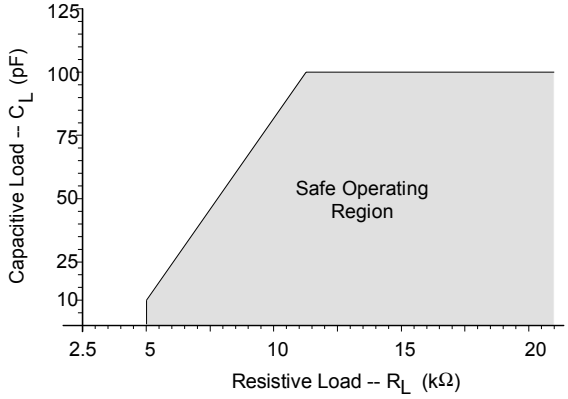


Figure 2. Maximum Analog Output Loading

ADC ANALOG CHARACTERISTICS - COMMERCIAL (-CQZ)

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V, VA_H = 9 V, GND = GNDH = 0 V; T_A = 25° C; 997 Hz Input Sine Wave. Decoupling capacitors, filter capacitors, and recommended input filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Dynamic Range	A-weighted		89	95	-	dB
	unweighted		86	92	-	dB
Total Harmonic Distortion + Noise	(Note 8)					
	-1 dB	THD+N	-	-88	-80	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
Double-Speed Mode						
Dynamic Range	A-weighted		89	95	-	dB
	unweighted		86	92	-	dB
Total Harmonic Distortion + Noise	(Note 8)					
	-1 dB	THD+N	-	-88	-80	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	+5	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Input Voltage			0.576•VA	0.606•VA	0.636•VA	V_{rms}
Input Impedance			-	200	-	kΩ
Maximum Interchannel Input Impedance Mismatch			-	2	-	%
Interchannel Isolation	(1 kHz)		-	-90	-	dB

Note: 8. Referred to the typical line-level full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DQZ)

Test Conditions (unless otherwise specified): VA = 3.13 V to 3.47 V, VD = 3.13 V to 3.47 V, VL = 1.71 V to 3.47 V, VA_H = 8.55 V to 12.60 V, GND = GNDH = 0 V; T_A = -40° C to +85° C; 997 Hz Input Sine Wave. Decoupling capacitors, filter capacitors, and recommended input filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Dynamic Range	A-weighted		85	95	-	dB
	unweighted		82	92	-	dB
Total Harmonic Distortion + Noise	(Note 8)					
	-1 dB	THD+N	-	-88	-78	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
Double-Speed Mode						
Dynamic Range	A-weighted		85	95	-	dB
	unweighted		82	92	-	dB
Total Harmonic Distortion + Noise	(Note 8)					
	-1 dB	THD+N	-	-88	-78	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	+5	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Input Voltage			0.576•VA	0.606•VA	0.636•VA	V_{rms}
Input Impedance			-	200	-	kΩ
Maximum Interchannel Input Impedance Mismatch			-	2	-	%
Interchannel Isolation	(1 kHz)		-	-90	-	dB

Note: 9. Referred to the typical line-level full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 10)			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)			0	-	0.489	Fs
Passband Ripple				-	-	0.035	dB
Stopband				0.569	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)			0	-	0.489	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay			t_{gd}	-	9/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	 (Note 11)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 11)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

Notes: 10. Response is clock dependent and will scale with sample rate (Fs). Note that the response plots (Figures 23 to 30) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

11. Response shown is for Fs = 48 kHz.

ANALOG PASS-THRU CHARACTERISTICS

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V; VA_H = 9 V; GND = GNDH = 0 V; T_A = 25° C; Input test signal is a 1 kHz sine wave; Measurement Bandwidth is 10 Hz to 20 kHz; Synchronous Mode.

Parameter	Symbol	Min	Typ	Max	Unit
Analog Input to Analog Output Characteristics (Gain=0dB)					
Dynamic Range					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
Total Harmonic Distortion + Noise (Note 8)					
0 dB	THD+N	-	-87	-81	dB
-3 dB		-	-93	-	dB
Frequency Response 10 Hz to 20 kHz		-	±0.1	-	dB
Analog Characteristics					
Max Input Voltage		-	2.0	-	V_{rms}
Max Output Voltage		-	2.0	-	V_{rms}
Max current draw from an AOUT pin	I_{OUT}	-	575	-	µA
AC-Load Resistance (Note 4)	R_L	5	-	-	kΩ
Load Capacitance (Note 4)	C_L	-	-	100	pF
Output Impedance	Z_{OUT}	-	50	-	Ω
Interchannel Isolation (1 kHz)		-	-90	-	dB

Note: 12. Referred to the typical line-level full-scale input voltage.

DC ELECTRICAL CHARACTERISTICS

GND = GNDH = 0 V; all voltages with respect to ground. MCLK1=12.288 MHz; MCLK2=static; Fs=48 kHz; Master Mode.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current (Normal Operation)	VA_H = 9 V	I_{A_H}	-	24	32	mA
	VA = 3.3 V	I_A	-	19	25	mA
	VD = 3.3 V	I_D	-	22	29	mA
	VL = 3.3 V	I_L	-	10	13	mA
Power Supply Current	VA _H= 9 V	I_{PD}	-	0	-	µA
(Power-Down Mode) (Note 13)	VL=VD=VA=3.3 V		-	200	-	µA
Power Consumption (Normal Operation)	VA_H = 9 V	-	-	216	289	mW
	VL=VD=VA = 3.3 V	-	-	169	225	mW
(Power-Down Mode)	All supplies	-	-	0.7	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 14)	PSRR	-	60	-	dB
Reference Voltages						
VCMADC Nominal Voltage		VCMADC	-	0.5•VA	-	V
VCMDAC Nominal Voltage		VCMDAC	-	4	-	V
DC Current from VCMADC or VCMDAC	(Note 15)	I_{CM}	-	-	1	µA
VCMADC or VCMDAC Output Impedance		Z_{CM}	-	23	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	V
VBIAS Nominal Voltage		VBIAS	-	VA-0.8	-	V

Notes: 13. Power-Down Mode is defined as $\overline{RST}$ = Low, with all clock and data lines held static low and no analog input.

14. Valid with the recommended capacitor values on FILT+, VCMDAC, VCMADC and VCMBUF as shown in Figure 7 on page 26 and Figure 8 on page 27.

15. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Parameters (Note 16)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	0.7•VL	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.2•VL	V
High-Level Output Voltage at I_o=2 mA	Digital Interface	V_{OH}	VL-1.0	-	-	V
	$\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$	V_{OH}	VA_H-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Digital Interface	V_{OL}	-	-	0.4	V
	$\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	+10	µA
Input Capacitance			-	-	1	pF
Maximum $\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$ Drive Current			-	3	-	mA
Minimum $\overline{OVFL}$ Active Time			$\frac{10^6}{LRCKX}$			µs

Note: 16. Digital Interface signals include all pins sourced from the VL supply as shown in "I/O Power Rails" on page 12.

SWITCHING CHARACTERISTICS - SERIAL AUDIO

Logic '0' = GND = GNDH = 0 V; Logic '1' = VL; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock (MCLKx = MCLK1, MCLK2)						
MCLKx Frequency MCLKx Duty Cycle			1.024 40	- 50	41.4720 60	MHz %
Sample Rates						
	Single-Speed Mode Double-Speed Mode	-	4 50	-	54 108	kHz
Master Mode						
SCLKx Frequency SCLKx Period SCLKx Duty Cycle (Note 17)	 1/(128*108 kHz) 	- t_{PERIOD} $t_{HIGH} \div t_{PERIOD}$	64•Fs 72.3 40	- - 50	64•Fs - 60	Hz ns %
LRCKx setup LRCKx hold	before SCLK rising after SCLK rising	t_{SETUP1} t_{HOLD1}	20 20	-	-	ns
SDOUT setup SDOUT hold	before SCLK rising after SCLK rising	t_{SETUP2} t_{HOLD2}	10 10	-	-	ns
Slave Mode						
SCLKx Frequency (Note 18) SCLKx Period SCLKx Duty Cycle	 1/(128•108 kHz) 	- t_{PERIOD} $t_{HIGH} \div t_{PERIOD}$	- 72.3 40	64•Fs - 50	- - 60	Hz ns %
LRCKx setup LRCKx hold	before SCLK rising after SCLK rising	t_{SETUP1} t_{HOLD1}	20 20	-	-	ns
SDOUT setup SDOUT hold	before SCLK rising after SCLK rising	t_{SETUP2} t_{HOLD2}	10 10	-	-	ns

Notes: 17. Duty cycle of generated SCLKx in Master Mode depends on duty cycle of the corresponding MCLKx as specified under "System Clocking" on page 28.

18. In Slave Mode, the SCLK/LRCK ratio can be set according to preference. However, specified performance is guaranteed only when using the ratios in Section 4.2.1 Master Mode on page 30 and Section 4.2.2 Slave Mode on page 30.

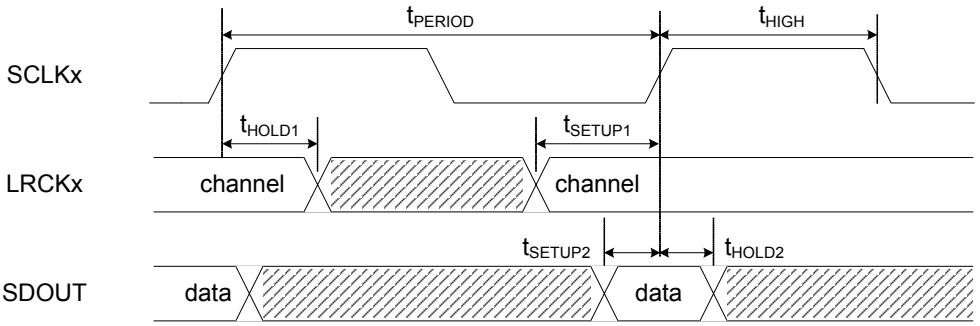


Figure 3. Serial Input Timing

SWITCHING CHARACTERISTICS - SERIAL AUDIO (CONT.)

Logic '0' = GND = GNDH = 0 V; Logic '1' = VL; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Mode						
SDINx setup SDINx hold	before SCLK rising after SCLK rising	t_{SETUP3} t_{HOLD3}	10 10	-	-	ns
Slave Mode						
SDINx setup SDINx hold	before SCLK rising after SCLK rising	t_{SETUP3} t_{HOLD3}	10 10	-	-	ns

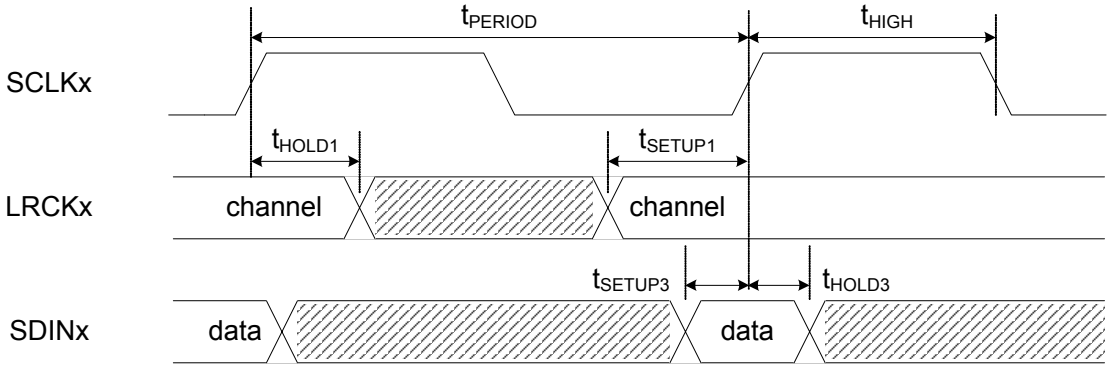


Figure 4. Serial Output Timing

SWITCHING CHARACTERISTICS - SOFTWARE MODE - I²C FORMAT

Inputs: Logic '0' = GND = GNDH = 0 V, Logic '1' = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note Note:)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Note: 19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

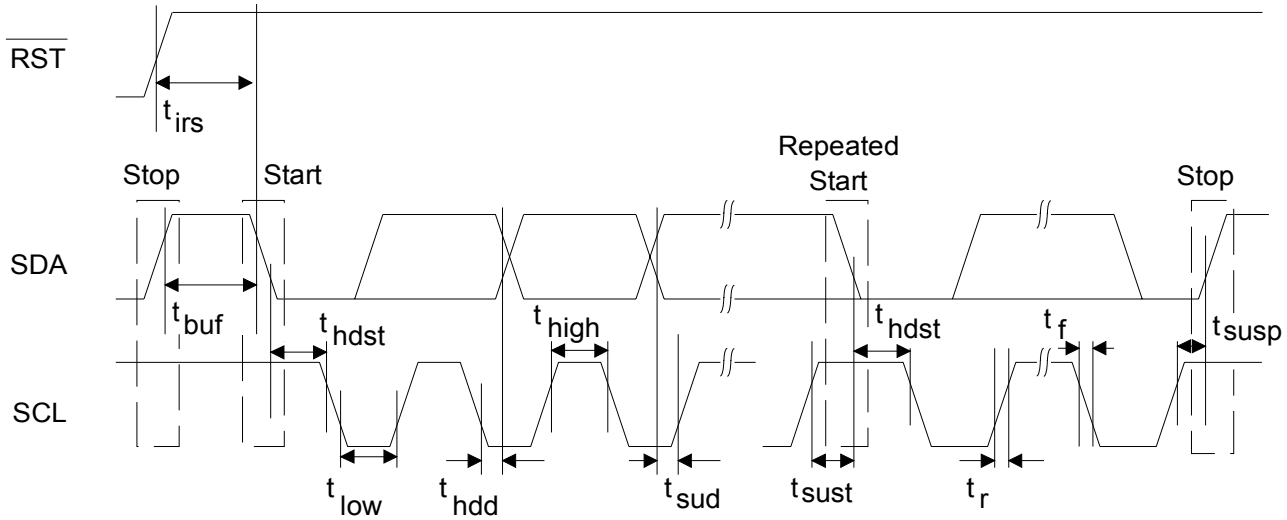


Figure 5. Software Mode Timing - I²C Format

SWITCHING CHARACTERISTICS - SOFTWARE MODE - SPI FORMAT

Inputs: Logic '0' = GND = GNDH = 0 V; Logic '1' = VLC; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling (Note 20)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 21)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 22)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 22)	t_{f2}	-	100	ns
Transition Time from CCLK to CDOUT Valid (Note 23)	t_{r2}	-	100	ns
Time from CS rising to CDOUT High-Z	t_{f2}	-	100	ns

Notes: 20. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

21. Data must be held for sufficient time to bridge the transition time of CCLK.
22. For F_{SCK} < 1 MHz.
23. CDOUT should *not* be sampled during this time.

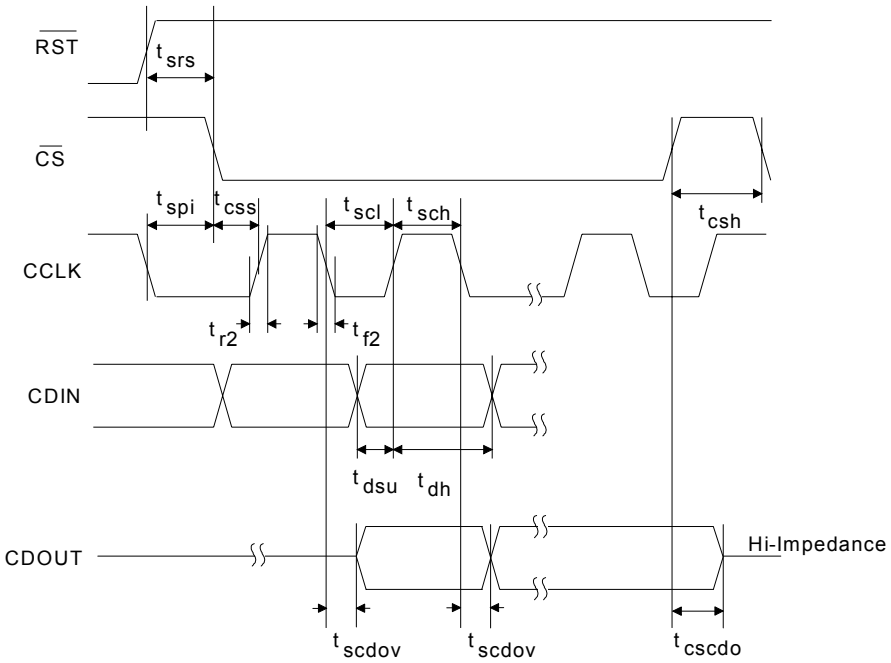


Figure 6. Software Mode Timing - SPI Mode

3. TYPICAL CONNECTION DIAGRAMS

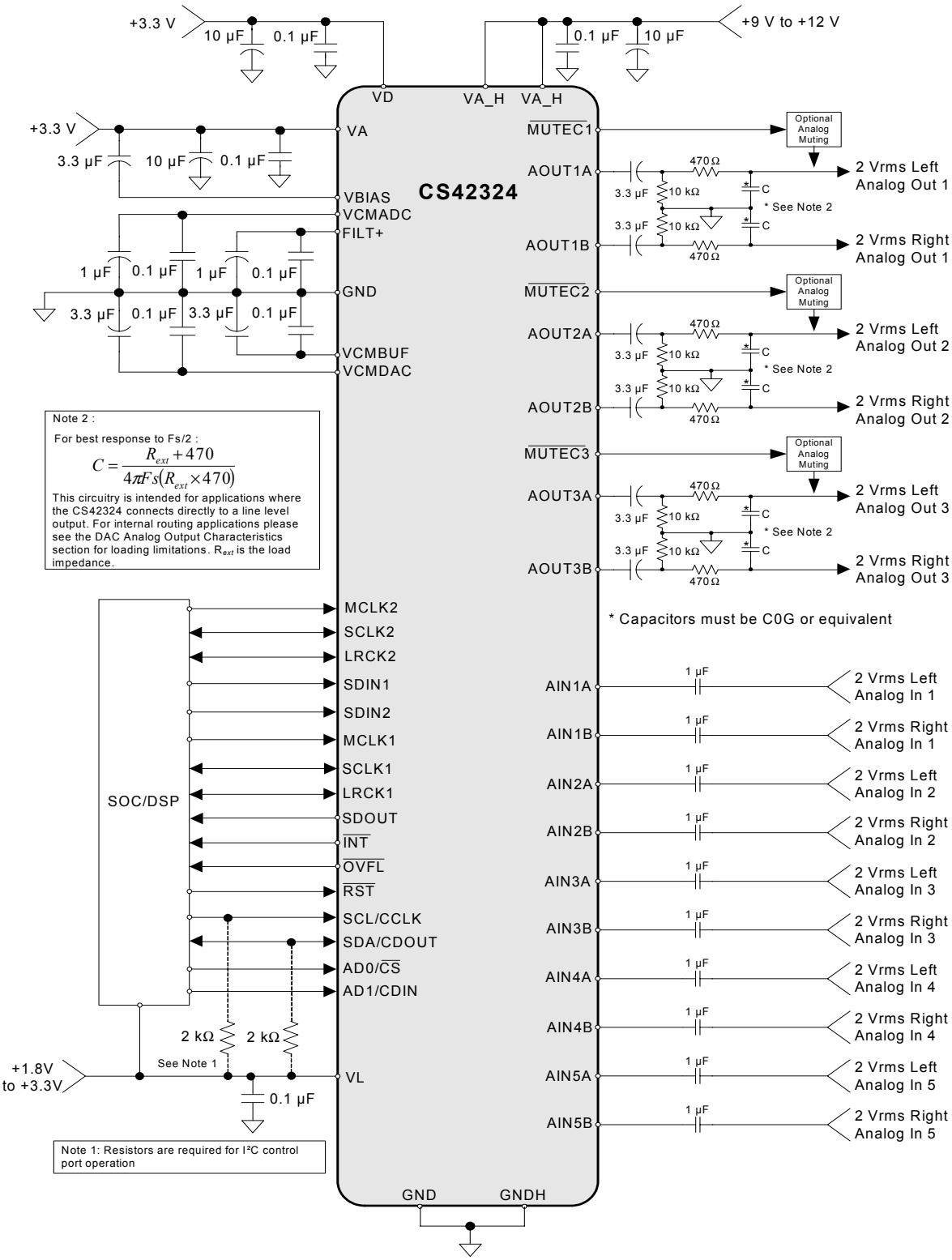


Figure 7. Typical Connection Diagram - Software Mode

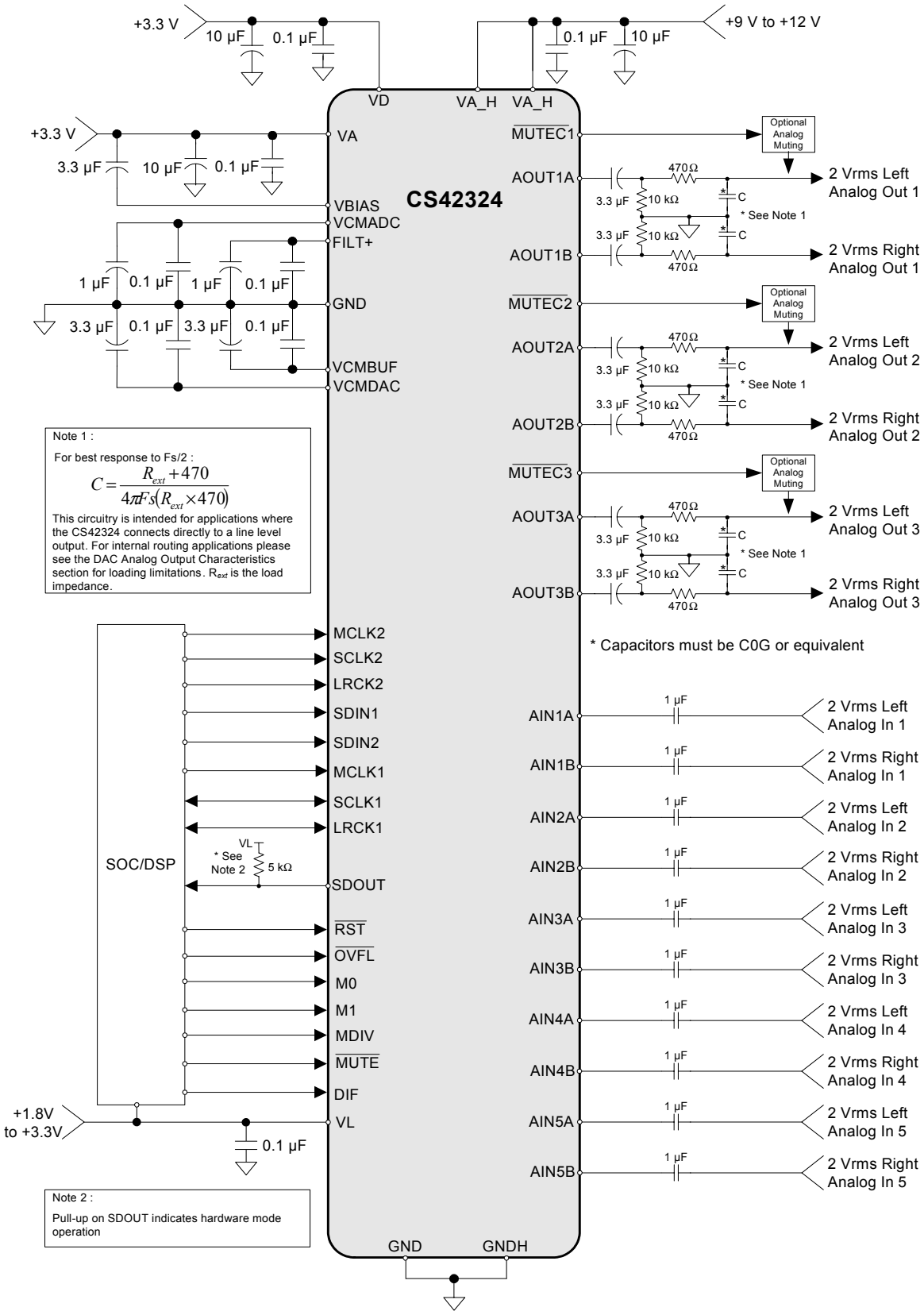


Figure 8. Typical Connection Diagram - Hardware Mode

4. APPLICATIONS

4.1 System Clocking

The CS42324 will operate at sampling frequencies from 4 kHz to 108 kHz. This range is divided into two speed modes as shown in Table 2.

Speed Mode	Master Mode Sampling Frequency	Slave Mode Sampling Frequency
Single-Speed	4-54 kHz	4-54 kHz
Double-Speed	50-108 kHz	50-108 kHz

Table 2. Speed Modes

The CS42324 has two serial ports which can operate synchronously or asynchronously. Serial Port 1 (SP1) consists of the SCLK1 and LRCK1 signals. Serial Port 2 (SP2) consists of the SCLK2 and LRCK2 signals. The serial audio output, SDOUT, and serial audio inputs, SDIN1 and SDIN2, can be independently assigned to either of the two serial ports for ease of clocking. Each serial port may be independently placed into Single- or Double-Speed Mode. The serial ports may also be independently placed into Master or Slave Mode.

4.1.1 Master Clock

In both Synchronous and Asynchronous Modes, MCLKx (MCLK1 and/or MCLK2) and the corresponding LRCKx must maintain an integer ratio. Some common ratios are shown in Tables 3 and 4. The LRCKx frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device. The SP1_SPEED and SP2_SPEED bits and the MCLKx FREQ bits configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode when auto detect mode is disabled. Tables 3 and 4 illustrate several standard audio sample rates and the required MCLKx and LRCKx frequencies.

Mode	LRCKx (kHz)	MCLKx (MHz)					
		128x	192x	256x	384x	512x	768x
SINGLE SPEED MODE (SSM)	32	-	-	8.1920	12.2880	16.3840	24.5760
	44.1	-	-	11.2896	16.9344	22.5792	33.8680
	48	-	-	12.2880	18.4320	24.5760	36.8640
MCLKx FREQ [1:0]		-	-	00	01	10	11
MDIV pin		-	-	0	-	1	-

Table 3. Single-Speed Mode Common Clock Frequencies

Mode	LRCKx (kHz)	MCLKx (MHz)					
		128x	192x	256x	384x	512x	768x
DOUBLE SPEED MODE (DSM)	64	8.1920	12.2880	16.3840	24.5760	-	-
	88.2	11.2896	16.9344	22.5792	33.8680	-	-
	96	12.2880	18.4320	24.5760	36.8640	-	-
MCLKx FREQ [1:0]		00	01	10	11	-	-
MDIV pin		0	-	1	-	-	-

Table 4. Double-Speed Mode Common Clock Frequencies

4.1.2 Synchronous / Asynchronous Mode

By default, the CS42324 operates in Synchronous Mode with both serial ports synchronous to MCLK1. In this mode, the serial ports may operate at different synchronous rates as set by the SP1_SPEED and SP2_SPEED bits, and MCLK2 does not need to be provided (the MCLK2 pin should be left unconnected if not required).

If the SPx_MCLK (SPx = SP1 and/or SP2) bits in serial ports 1 and 2 are set differently, the CS42324 will operate in Asynchronous Mode. The serial ports will operate asynchronously with Serial Port 1 clocked from its SP1_MCLK selection and Serial Port 2 clocked from its SP2_MCLK selection. In this mode, the serial ports may operate at different asynchronous rates.

In Hardware Mode MCLK1 is the master clock source for all internal circuits. Clock selection and asynchronous operation are not available.

4.2 Serial Port Operation

Each CS42324 serial audio interface port operates as either a clock slave or master. They accept externally generated clocks in slave mode (LRCKx and SCLKx pins are inputs, generated clocks shown in Figure 9 are disabled) and will generate synchronous clocks derived from an input master clock (MCLK1/MCLK2) in master mode (LRCKx and SCLKx pins are outputs, generated clocks shown in Figure 9 are enabled).

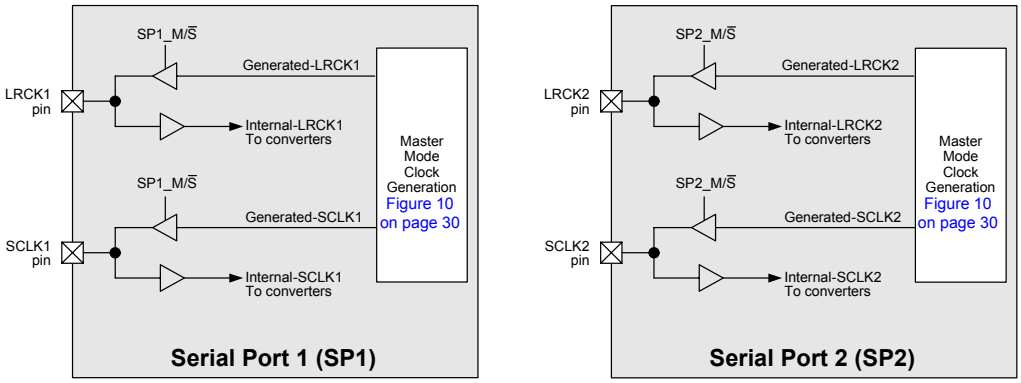


Figure 9. Serial Port Topology

The LRCK, Fs, is the frequency at which audio samples for each channel are clocked into or out of the device. In slave mode, LRCK should be synchronously derived from the MCLK selected in SPx_MCLK register.
The SCLK is the bit clock which is used to clock in the serial audio data stream. SCLK should adhere to the timing requirements outlined in "Switching Characteristics - Serial Audio" on page 22.

The SP1_SPEED, SP2_SPEED, MCLK1 FREQ[1:0] and MCLK2 FREQ[1:0] Software Mode control bits or the M1, M0, and MDIV hardware control pins, configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. In hardware mode, control pins M1 and M0 configure the master/slave mode setting for the serial ports as well as the speed mode as shown in Table 5.

M0 (Pin 1)	M1 (Pin 2)	Serial Port Configuration
0	0	Clock Master, Single-Speed Mode
0	1	Clock Master, Double-Speed Mode
1	0	Reserved
1	1	Clock Slave, Auto-detect Speed Mode

Table 5. M1 and M0 Mode Pins in Hardware Mode

4.2.1 Master Mode

As a clock master, the LRCKx and SCLKx of each serial port will operate as outputs. The two serial ports may be independently placed into Master or Slave Mode. Each LRCKx and SCLKx are internally derived from the MCLKx selected by the SP1_MCLK and SP2_MCLK signals as shown in Figure 10.

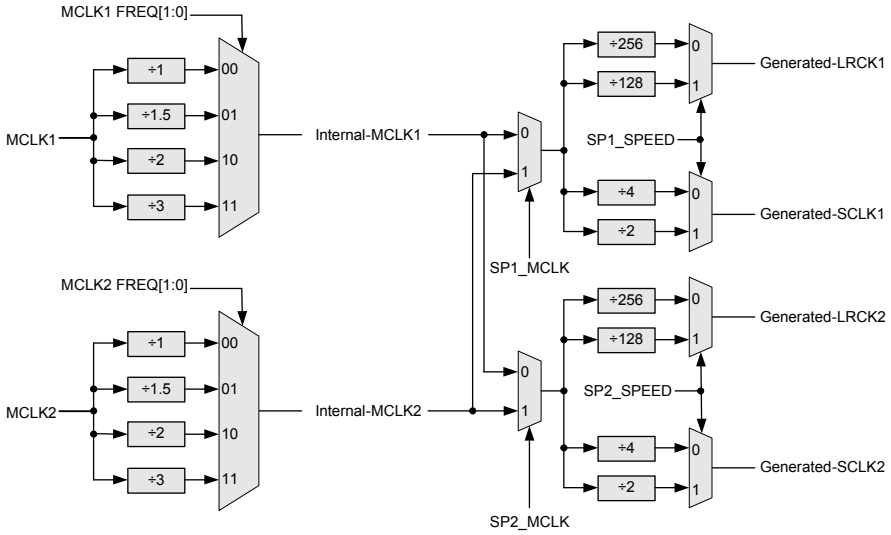


Figure 10. Master Mode Clock Generation

4.2.2 Slave Mode

In Slave Mode, SCLKx and LRCKx operate as inputs. Each serial port may be independently placed into Slave Mode. The Left/Right clock signal, LRCKx, must be equal to the sample rate, Fs. The serial bit clock, SCLKx, must be equal to 128x, 64x, 48x, or 32x Fs depending on the desired speed mode. Refer to Table 6 for required serial bit clock to Left/Right clock ratios.

If operating in Asynchronous Mode, LRCK1 and SCLK1 must be synchronously derived from the SP1's selected MCLK, and LRCK2 and SCLK2 must be synchronously derived from SP2's selected MCLK. If operating in Synchronous Mode, SCLK1, LRCK1, SCLK2 and LRCK2 must be synchronously derived from the same MCLK. For more information on Synchronous and Asynchronous Modes, see "Synchronous / Asynchronous Mode" on page 29.

Serial Data Format	SCLKx to LRCKx Ratio	
	Single Speed Mode	Double Speed Mode
I²S, LJ or RJ Data Format	32, 48, 64, 128	32, 48, 64

Table 6. Slave Mode SCLK/LRCK Ratios

The speed of each serial port is automatically determined based on the input MCLKx to LRCKx ratio when the Auto-Detect function is enabled. Certain input clock ratios will then require an internal divide-by-two of MCLKx using either the MCLKx FREQ bits or the MDIV hardware control pin.

Mode	MCLKx to LRCKx Ratio	
	Single Speed Mode	Double Speed Mode
SW Auto Mode Detect	256, 384, 512, 768	128, 192, 256, 384
HW Auto Mode Detect	256, 512	128, 256

See Table 3 an Table 4 on page 28 for clock ratio configuration.

Table 7. MCLKx to LRCKx Ratios

4.2.3 ADC, DAC1, and DAC2 clock selection

The ADC, DAC1, and DAC2 can be independently set to use either of the two serial ports as a clock source. Each also has control over which MCLK to use. This allows for full flexibility in configuration of the converter. Master/Slave control is achieved at the serial port level (See Figure 9 on page 29); the internal converters discussed here are always slave.

Each converter has a bit in the registers (xxx_SP, where xxx = ADC, DAC1, or DAC2) which allows selection of the SCLK/LRCK pair used for the converter. The xxx_MCLK bits select which MCLK source to use for the converter. If the serial port selected for use is in master mode, this selection must be the same as the MCLK_SPx for the serial port which is in use. In Slave mode the MCLK selected must be synchronous to the LRCK/SCLK selected by xxx_SP.

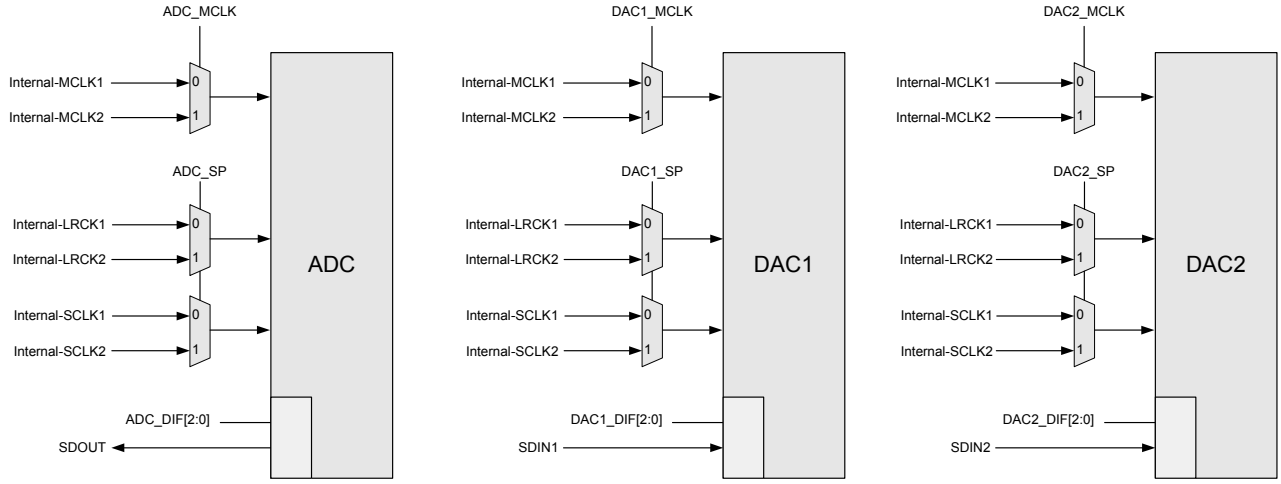


Figure 11. Converter Clocking

4.2.4 High-Impedance Digital Output

Each serial port may be placed on a clock/data bus that allows multiple masters, without the need for external buffers. The 3ST_SP1, 3ST_SP2 and 3ST_SDOUT bits place the internal buffers for the serial port signals in a high-impedance state, allowing another device to transmit clocks or data without bus contention.

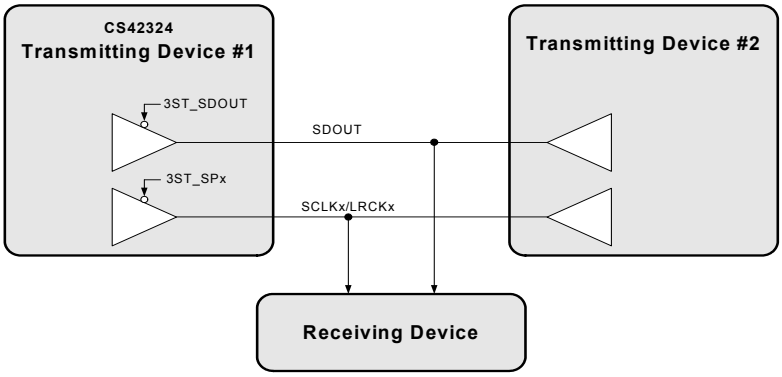


Figure 12. Tri-State Serial Port

4.2.5 Digital Interface Formats

Each converter (ADC, DAC1, and DAC2) has independent selection for serial formats (I²S, Left-Justified, etc.). Data is clocked out of the ADC or into the DAC on the rising edge of SCLK. Figures 13-17 illustrate the general structure of each format. Refer to "Switching Characteristics - Serial Audio" on page 22 or "Switching Characteristics - Serial Audio (Cont.)" on page 23 for exact timing relationship between clocks and data. For a complete overview of Serial Audio Interface Formats, please reference Application Note AN282.

DIF (Pin 5) Setting	Selection
LO	Left-Justified Interface
HI	I²S Interface

Table 8. Hardware Mode Interface Format Control

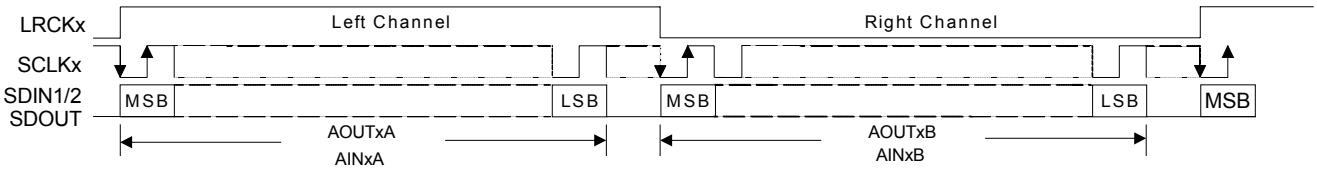


Figure 13. Left-Justified up to 24-Bit Data

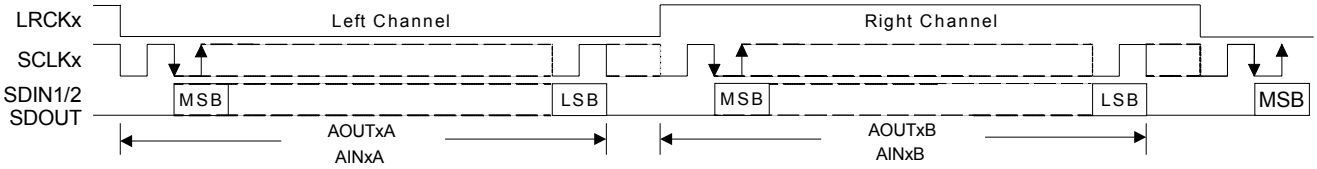


Figure 14. I²S up to 24-Bit Data

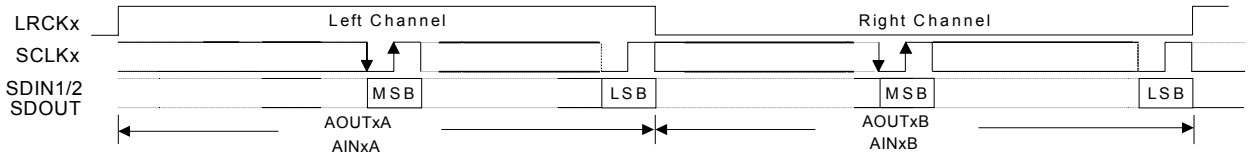


Figure 15. Right-Justified 16-Bit Data, Right-Justified 24-Bit Data

4.2.6 Synchronization of Multiple Devices

In systems where multiple ADCs and DACs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the master clocks and left/right clocks must be the same for all of the CS42324's in the system. If only one master clock source is needed, one solution is to place one CS42324 in Master Mode, and slave all of the other devices to the one master.

4.3 Analog-to-Digital Data Path

4.3.1 ADC Analog Input Multiplexer

AINxA and AINxB are the analog inputs, internally biased to VCMADC. The CS42324 contains a stereo 5-to-1 analog input multiplexer which can select one of 5 possible stereo analog input sources and route it to the ADC. Figure 16 shows the architecture of the input multiplexer.

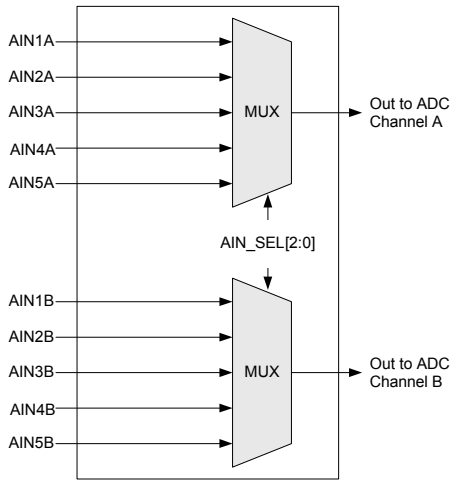


Figure 16. Analog Input Architecture

"Section 6.9 "ADC Control (Address 0Ah)" on page 52" outlines the bit settings necessary to control the input multiplexer. By default, line level input 1 is selected.

4.3.2 ADC Description

The ADC analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) the digital passband frequency, where n=0,1,2,... Refer to the Typical Connection Diagram for the recommended analog input circuit that will attenuate noise energy at 6.144 MHz. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. Any unused analog input pairs should be left unconnected.

The ADC output data is in two's complement binary format. For inputs above positive full-scale or below negative full-scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC overflow bit to be set to a '1'.

Given the two's complement format, low-level signals may cause the MSB of the serial data to periodically toggle between '1' and '0', possibly introducing noise into the system as the bit switches back and forth. To prevent this phenomena, a constant DC offset is added to the serial data bringing the low-level signal just above the point at which the MSB would normally toggle, thus reducing the noise introduced. Note that this offset is not removed (refer to "ADC Analog Characteristics - Commercial (-CQZ)" on page 17 for the specified offset level).

4.3.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS42324, a small DC offset may be driven into the A/D converter. The CS42324 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42324 with the high-pass filter enabled until the filter settles. See "ADC Digital Filter Characteristics" on page 19 for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset for continuous subtraction.

A system calibration performed in this way eliminates offsets anywhere in the signal path between the calibration point and the CS42324.

4.3.4 Digital Attenuation Control

Digital attenuation control functions are implemented, offering independent channel control for the ADC PCM signal path. The volume controls are programmable to ramp in increments of 0.5 dB at a rate controlled by the ADC soft ramp.

Each ADC signal path may also be independently muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the ADC_SOFT.

4.4 Digital-to-Analog Data Path

4.4.1 Digital Volume Control

Two stereo digital volume control functions are implemented, offering independent channel control for DAC1 and DAC2 PCM signal paths into the digital mixer. The volume controls are programmable to ramp in increments of 0.5 dB at a rate controlled by the DAC1/2 soft ramp/zero cross settings.

Each DAC1/2 signal path may also be independently muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the DAC1/2_SOFT and DAC1/2_ZC bits.

4.4.2 Mono Channel Mixer

Independent channel mixers for DAC1 and DAC2 may be used to create a mix of the left and right channels PCM signals. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

4.4.3 De-Emphasis Filter

The CS42324 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 17. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction. De-emphasis is only available in Single-Speed Mode

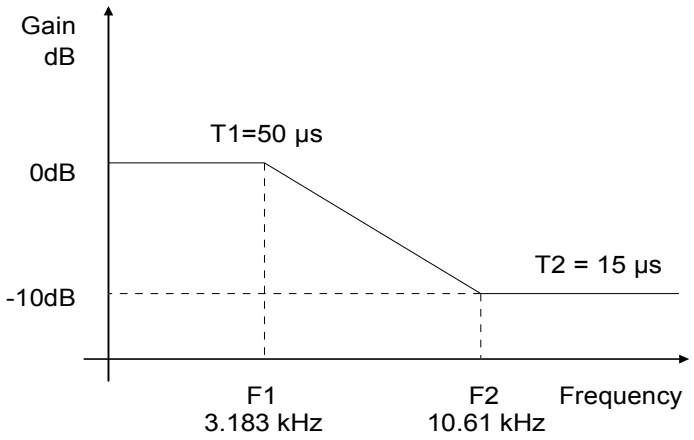


Figure 17. De-Emphasis Curve

4.4.4 Internal Digital Loopback

The CS42324 supports an internal digital loopback mode in which the ADC's output data can be internally routed to either of the DAC inputs. This mode may be activated by setting the DACx_LOOP_BACK bit in "DAC1 Control (Address 0Bh)" on page 53 and "DAC2 Control (Address 0Ch)" on page 55. During this mode, the ADC and DAC will need to operate at the same synchronous sample rate. When the DACx_LOOP_BACK bit is set, the respective DACx_DIF[2:0] bits must be set to the same value as the ADC_DIF[2:0] register.

During loop back mode, the ADC data will continue to be present on the SDOUT pin in the format selected by the ADC_DIF[2:0] bits.

4.4.5 DAC Description

The CS42324 uses a switched current architecture followed by on chip current to voltage conversion and continuous time low-pass filter. The digital interpolator response is shown in the "DAC Digital Filter Response Plots" on page 67. The recommended external analog circuitry is shown in the "Typical Connection Diagrams" on page 26.

The CS42324 DAC does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

4.4.6 Analog Output Multiplexer

The CS42324 contains three independent stereo 7-to-1 analog output multiplexers which can select one of seven possible stereo analog output sources and route it to the AOUTxA and AOUTxB pins. Figure 18 shows the architecture of the analog output multiplexer.

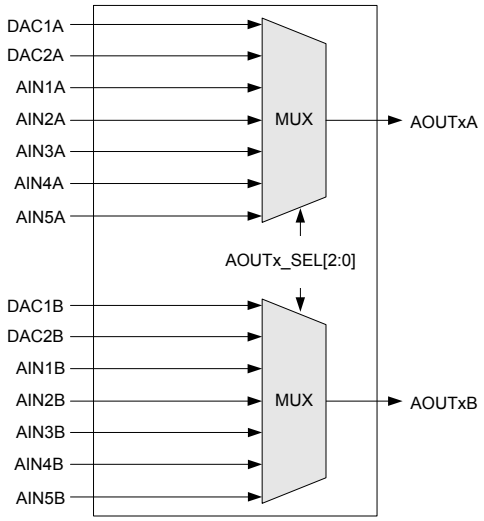


Figure 18. Analog Output Architecture

"Section 6.12 "AOUT1 Control (Address 0Dh)" on page 56" and Section 6.13 "AOUT2 Control (Address 0Eh)" on page 57 outline the bit settings necessary to control the output multiplexer.

4.4.7 Output Transient Control

The CS42324 uses Popguard technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

4.4.7.1 Power-Up

When the device is initially powered up, the audio outputs AOUTxA and AOUTxB are clamped to VCMBUF which is initially low. After the PDN bit is released (set to '0') the outputs begin to ramp with VCMBUF towards the nominal quiescent voltage. This ramp takes approximately 200 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VCMBUF, effectively blocking the quiescent DC voltage. Audio output from the DACs will begin after approximately 2000 sample periods.

4.4.7.2 Power-Down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this, either the PDN bit should be set or the device should be reset about 250 ms before removing power. During this time, the voltage on VCMBUF and the AOUTx outputs discharge gradually to GND. If power is removed before this 250 ms time period has passed, a transient will occur when the VA supply drops below that of VCMBUF. There is no minimum time for a power cycle; power may be re-applied at any time.

4.4.7.3 Serial Interface Clock Changes

When changing the serial port clock ratio or sample rate, it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change, the DAC outputs will always be in a zero data state. If non-zero serial audio input is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to it's zero data state.

4.4.8 Mute Control

The $\overline{\text{MUTECx}}$ pins become active during power-up initialization, reset, software/hardware muting, and power-down mode (PDN=1). The $\overline{\text{MUTECx}}$ pins are intended to be used as control for an external mute circuit in order to add off-chip mute capability.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The $\overline{\text{MUTECx}}$ pins are active-low CMOS drivers.

4.5 Initialization

The initialization and Power-Down sequence flow chart is shown in Figure 19 on page 39. The CODEC enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and software registers are reset. The internal voltage reference, multi-bit DACs and ADC, and on-chip amplifiers are powered down.

4.5.1 Determining Hardware or Software Mode

The device will remain in the Power-Down state until the $\overline{\text{RST}}$ pin is brought high. If there is a pull-up on SDOUT, or SDOUT is held high by any other means at the time $\overline{\text{RST}}$ pin is brought high, the device will enter Hardware mode and begin powering up immediately. If no pull-up is present, or SDOUT is held low by any other means at the time $\overline{\text{RST}}$ pin is brought high, the device will enter software mode.

4.5.2 Hardware Mode Start-Up

When the pull-up on SDOUT is present Hardware Mode is selected. Once hardware mode is selected, the hardware mode configuration pins are used to set up the device and power-up will occur following the HW startup path as shown in Figure 19 on page 39. The modes of configuration for this mode can be found in Section 4.6.1 "Hardware Mode" on page 40. Because of the limited configuration abilities in Hardware mode, many modes of operation are not available.

Only MCLK1 needs to be applied. Once the appropriate MCLK1 is valid and $\overline{\text{RST}}$ is high, the quiescent voltage, VCMADC and VCMBUF, and the internal voltage references, FILT+ and VCM_ADC, will begin powering up to normal operation. During this voltage reference ramp delay, both SDOUT and the AOUTxA/AOUTxB outputs will be automatically muted. Once LRCKx is valid, MCLKx occurrences are counted over one LRCKx period to determine the MCLKx/LRCKx frequency ratio and normal operation begins.

It is recommended that $\overline{\text{RST}}$ be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

4.5.2.1 Recommended Power-Up Sequence, Hardware Mode

1. Hold $\overline{\text{RST}}$ low until MCLK1 and the power supplies are stable.
2. Bring $\overline{\text{RST}}$ high (SDOUT must be pulled high).
3. Apply all LRCKx, SCLKx and SDIN signals for normal operation to begin.
4. Bring $\overline{\text{RST}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.5.2.2 Recommended Power-Down Sequence, Hardware Mode

To minimize audible pops when turning off or placing the CODEC in standby:

1. Mute the SDIN1 and SDIN2 streams feeding the CODEC.
2. Bring $\overline{\text{RST}}$ low.

4.5.3 Software Mode Start-Up

When no pull-up on SDOUT is present, the Software Mode is accessible once $\overline{\text{RST}}$ is high. The desired register settings can be loaded per the interface descriptions in "Software Mode - I²C Control Port" on page 41. When the desired configuration is complete the PDN bit in "Operational Control (Address 02h)" on page 47 should be set to 0 to initiate the power up sequence. The quiescent voltage, VCMADC and VCMBUF, and the internal voltage references, FILT+ and VCM_ADC, will then begin powering up to normal operation. During this voltage reference ramp delay, both SDOUT and the AOUTxA/AOUTxB outputs will be automatically muted. Once LRCKx is valid, MCLKx occurrences are counted over one LRCKx period to determine the MCLKx/LRCKx frequency ratio and normal operation begins.

It is recommended that $\overline{\text{RST}}$ be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

4.5.3.1 Recommended Power-Up Sequence, Software Mode

1. Hold $\overline{\text{RST}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RST}}$ high, the device will be in "standby".
3. Load the desired register settings while keeping the PDN bit set to '1'b.
4. Start MCLK1 (and MCLK2 if it is used) to the appropriate frequency, as discussed in Section 4.1.1.
5. Set the PDN bit to '0'b.
6. Apply all LRCKx, SCLKx and SDIN signals for normal operation to begin.
7. Bring $\overline{\text{RST}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.5.3.2 Recommended Power-Down Sequence, Software Mode

To minimize audible pops when turning off or placing the CODEC in standby:

1. Using the appropriate registers, 9Mute the AOUTxA, AOUTxB, DAC's & ADC's.
2. Set the PDN bit in the power control register to '1'b. The CODEC will not power down until it reaches a fully muted sate.
3. Bring $\overline{\text{RST}}$ low.

4.5.4 Initialization Flow Chart

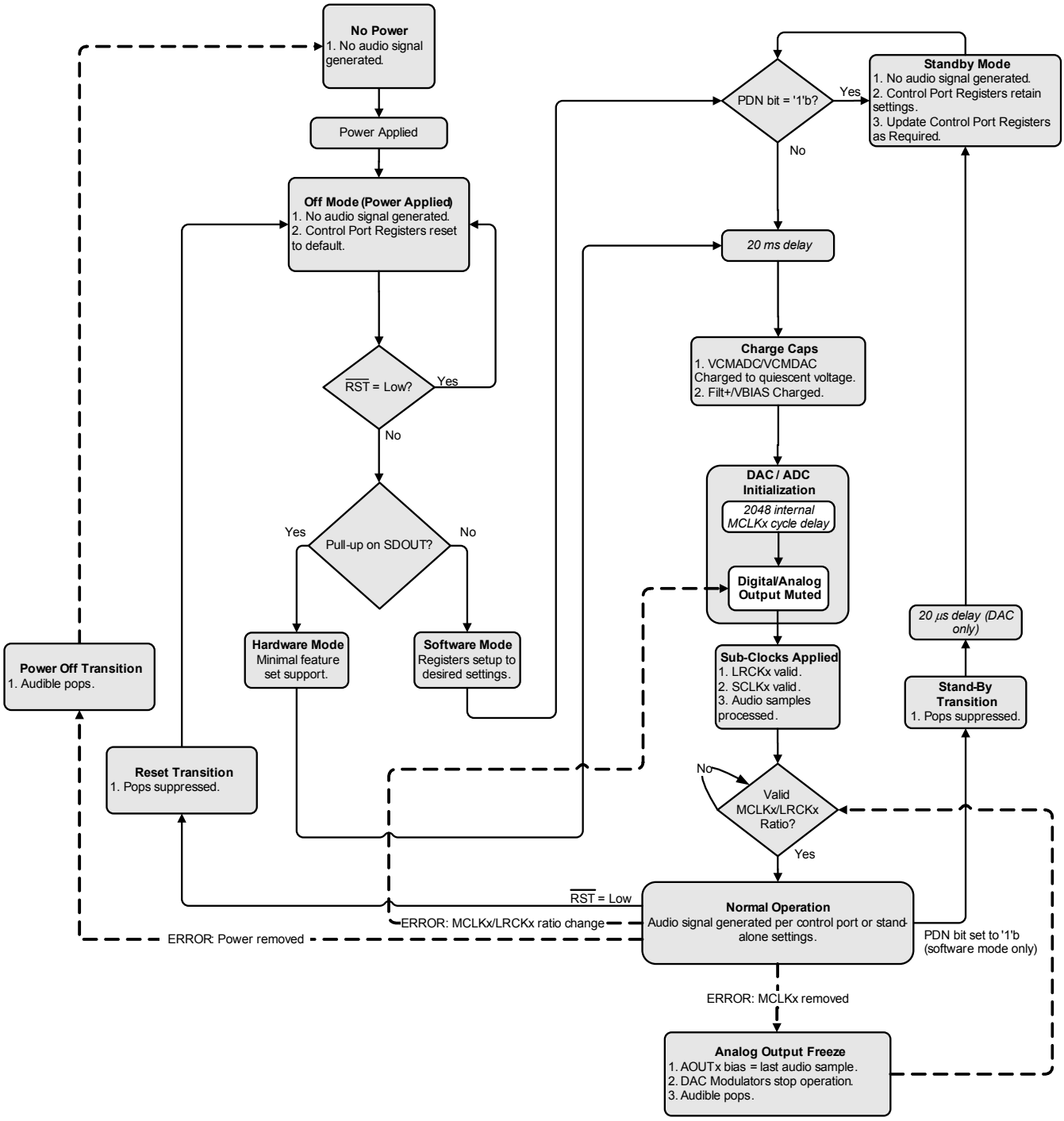


Figure 19. Initialization Flow Chart

4.6 Device Control

In Software Mode, all functions and features may be controlled either by two-wire I²C or SPI Software Mode interface. In Hardware Mode, a limited feature set may be controlled via hardware control pins.

4.6.1 Hardware Mode

A limited feature-set is available when the CS42324 powers up in Hardware Mode (see "Recommended Power-Up Sequence, Hardware Mode" on page 38) and may be controlled via hardware control pins. Table 9 shows a list of functions/features, the default configuration and the associated hardware control available.

Hardware Mode Feature Summary			
Feature/Function		**Default Configuration**	**Hardware Control**
Power Control	ADC DAC1 DAC2	Powered Up Powered Up Powered Up	- - -
SP_ERROR		Enabled; Active low, open drain	-
Auto Detect		Enabled (256x/128xFs, 512x/256xFs only)	-
Serial Port Master/Slave and Speed Mode		(Selectable)	"M0" and "M1", pins 1 and 2 (see page 29)
Async / Sync Mode		Synchronous only	-
MCLK Divide		(Selectable)	"MDIV" pin 3 (see page 30)
Serial Port Interface Format	Serial Port 1 Serial Port 2	(Selectable)	"DIF" pin 5 (see page 32)
Freeze Bit Settings		Disabled	-
ADC Volume & Gain	Soft Ramp Zero Cross Mute Invert Volume	Enabled Disabled Disabled Disabled 0 dB	- - - - -
ADC High-Pass Filter ADC High-Pass Filter Freeze		Enabled Continuous DC Subtraction	- -
AIN Input Select to ADC	(SDOUT source)	AIN1	-
DAC1 & DAC2 Volume & Gain	Soft Ramp Zero Cross Mute Invert Mixer Volume	Enabled Disabled Disabled Disabled Disabled ('00') 0 dB	- - - - - -
DAC1 & DAC2 De-Emphasis		Disabled	-
AOUT1x	source	Output of DAC1	-
AOUT2x	source	Output of DAC2	-
AOUT3x	source	AIN1x	-
AOUTxx	MUTE	(Selectable)	$\overline{\text{MUTE}}$ pin 4 (see page 37)

Table 9. Hardware Mode Feature Summary

4.6.2 Software Mode - I²C Control Port

Software Mode is used to access the registers, allowing the CS42324 to be configured for the desired operational modes and formats. The operation in Software Mode may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the I²C pins should remain static if no operation is required. Software Mode supports the I²C interface, with the CS42324 acting as a slave device.

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or GND as desired. The state of the pin is sensed while the CS42324 is being reset.

The signal timings for a read and write cycle are shown in Figure 20 and Figure 21. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42324 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS42324, the chip address field, which is the first byte sent to the CS42324, should match 10011 followed by the settings of AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42324 after each input byte is read, and is input to the CS42324 from the microcontroller after each transmitted byte.

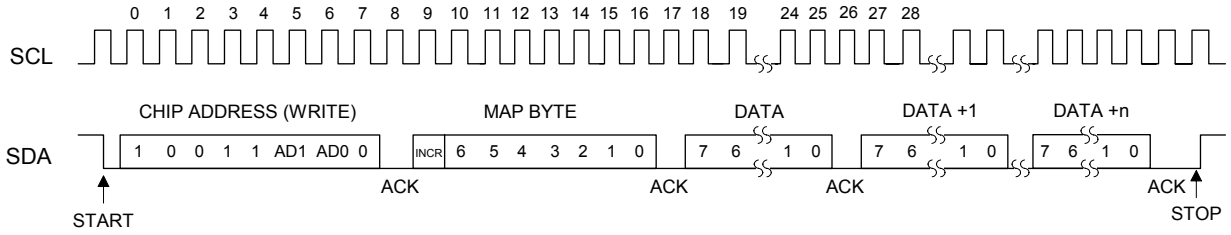


Figure 20. Software Mode Timing, I²C Write

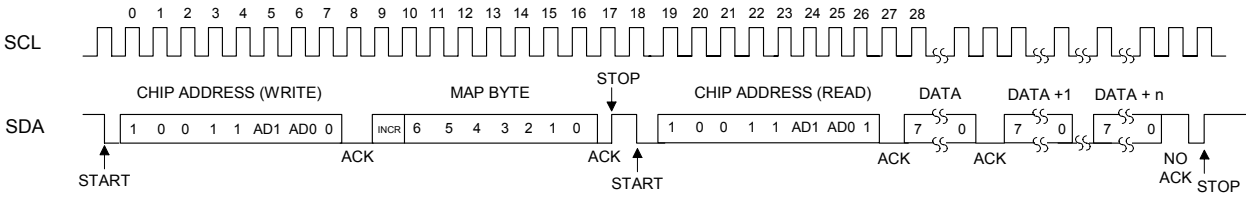


Figure 21. Software Mode Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 21, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

```
Send start condition.
Send 10011xx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10011xx1(chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.
```

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.6.3 Software Mode - SPI Control Port

In SPI Mode, data is clocked into the serial control data line, CDIN, by the serial clock, CCLK (see Figure 22 for the clock to data relationship). There are no AD0 or AD1 pins. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the registers. When the device detects a high-to-low transition on the AD0/$\overline{CS}$ pin after power-up, SPI Mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.6.3.1 SPI Write

To write to the device, follow the procedure below while adhering to the Software Mode switching specifications in "Switching Characteristics - Software Mode - SPI Format" section on page 25.

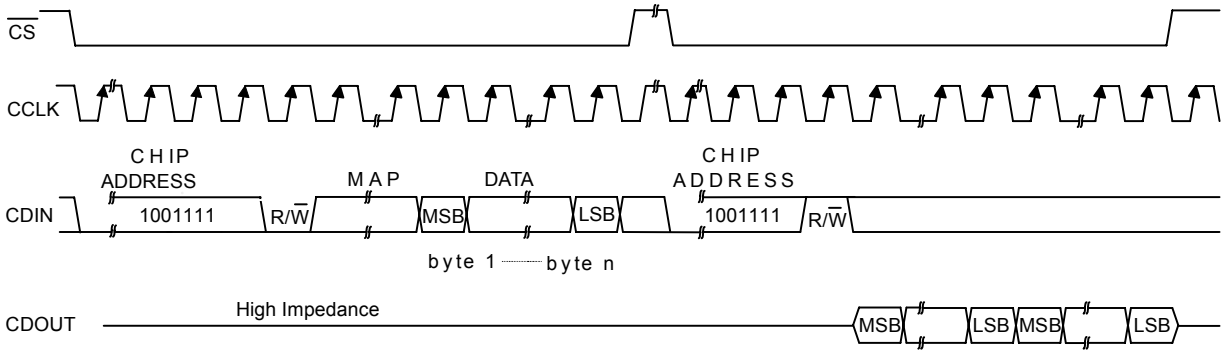
1. Bring CS low.
2. The address byte on the CDIN pin must then be 10011110 (R/$\overline{W}$ = 0).
3. Write to the memory address pointer, MAP. This byte points to the register to be written.
4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see Section 4.6.4.1) is set to 1, repeat the previous step until all the desired registers are written, then bring CS high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high

4.6.3.2 SPI Read

To read from the device, follow the procedure below while adhering to the values specified in "Switching Characteristics - Software Mode - SPI Format" section on page 25.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011111 (R/$\overline{W}$ = 1).
3. CDOUT pin will then output the data from the register pointed to by the MAP, which is set during the SPI write operation.
4. If the INCR bit (see Section 4.6.4.1) is set to 1, keep $\overline{CS}$ low and continue providing clocks on CCLK to read from multiple consecutive registers. Bring $\overline{CS}$ high when reading is complete.

5. If the INCR bit is set to 0 and further SPI reads from other registers are desired, it is necessary to bring CS high, and follow the procedure detailed from step 1. If no further reads from other registers are desired, bring CS high.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 22. Software Mode Timing, SPI Mode

4.6.4 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.6.4.1 Map Increment (INCR)

The device has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

4.7 Interrupts and Overflow

The CS42324 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may function as either an active high CMOS driver or an active low open-drain driver (see “Operational Control (Address 02h)” on page 47). When configured as active low open-drain, the INT pin has no active pull-up transistor, allowing it to be used for wired-OR hook-ups with multiple peripherals connected to the microcontroller interrupt input pin. In this configuration, an external pull-up resistor must be placed on the INT pin for proper operation.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See “Interrupt Status (Address 18h) (Read Only)” on page 61. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer. Reading the Interrupt Status register will clear the interrupt condtion.

The CS42324 also has a dedicated overflow output. The OVFL pin functions as active low open drain and has no active pull-up transistor, thereby requiring an external pull-up resistor. The OVFL pin outputs an OR of the ADC Overflow Positive and Negative conditions available in the Interrupt Status register; however, these conditions do not need to be unmasked for proper operation of the OVFL pin.

5. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values. All bits marked as “Reserved” must maintain their default values.

Addr	Function	7	6	5	4	3	2	1	0
00h	Device ID	DEVICE3	DEVICE2	DEVICE1	DEVICE0	REV3	REV2	REV1	REV0
	page 46	0	1	1	0	x	x	x	x
01h	Mute Control	Reserved	SYS_MCLK	DAC2_ MuteL	DAC2_ MuteR	DAC1_ MuteL	DAC1_ MuteR	ADC_ MuteL	ADC_ MuteR
	page 46	0	1	0	0	0	0	0	0
02h	Operational Control	Reserved	PDN	INT_HL	FREEZE	Reserved	TRI-SDOUT	TRI-SP1	TRI-SP2
	page 47	0	1	0	0	0	0	0	0
03h	Serial Port 1 Control	SP1_M/$\overline{S}$	Reserved	Reserved	SP1_ SPEED	MCLK1 FREQ1	MCLK1 FREQ0	Reserved	SP1_MCLK
	page 49	0	0	0	0	0	0	0	0
04h	Serial Port 2 Control	SP2_M/$\overline{S}$	Reserved	Reserved	SP2_ SPEED	MCLK2 FREQ1	MCLK2 FREQ0	Reserved	SP2_MCLK
	page 50	0	0	0	0	0	0	0	0
05h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
06h	ADC clocking	Reserved	ADC_ MCLK	Reserved	ADC_ SP	Reserved	Reserved	ADC_DIF1	ADC_DIF0
	page 50	0	0	0	0	1	0	0	0
07h	DAC1 clocking	Reserved	DAC1_ MCLK	Reserved	DAC1_SP	Reserved	Reserved	DAC1_DIF1	DAC1_DIF0
	page 51	0	0	0	1	1	0	0	0
08h	DAC2 clocking	Reserved	DAC2_ MCLK	Reserved	DAC2_SP	Reserved	Reserved	DAC2_DIF1	DAC2_DIF0
	page 52	0	0	0	1	1	0	0	0
09h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
0Ah	ADC Control	Reserved	ADC_ HPFRZ	ADC_ SOFT	Reserved	Reserved	AIN_SEL2	AIN_SEL1	AIN_SEL0
	page 52	1	0	1	0	0	0	0	1
0Bh	DAC1 Control	DAC1_ DEPH	DAC1_ SNGVOL	DAC1_SOFT	DAC1_ZC	DAC1_ LOOPBACK	DAC1_INV	DAC1_MIX1	DAC1_MIX0
	page 53	0	0	1	0	0	0	0	0
0Ch	DAC2 Control	DAC2_ DEPH	DAC2_ SNGVOL	DAC2_ SOFT	DAC2_ ZC	DAC2_ LOOPBACK	DAC2_INV	DAC2_MIX1	DAC2_MIX0
	page 55	0	0	1	0	0	0	0	0
0Dh	AOUT1 Control	Reserved	Reserved	Reserved	Reserved	MUTEC1	AOUT1_ SEL2	AOUT1_ SEL1	AOUT1_ SEL0
	page 56	0	0	0	0	0	1	1	0
0Eh	AOUT2 Control	Reserved	Reserved	Reserved	Reserved	MUTEC2	AOUT2_ SEL2	AOUT2_ SEL1	AOUT2_ SEL0
	page 57	0	0	0	0	0	1	1	1
0Fh	AOUT3 Control	Reserved	Reserved	Reserved	Reserved	MUTEC3	AOUT3_ SEL2	AOUT3_ SEL1	AOUT3_ SEL0
	page 57	0	0	0	0	0	0	0	1

Addr	Function	7	6	5	4	3	2	1	0
10h	ADC Ch A Volume Control	ADCA_ VOL7	ADCA_ VOL6	ADCA_ VOL5	ADCA_ VOL4	ADCA_ VOL3	ADCA_ VOL2	ADCA_ VOL1	ADCA_ VOL0
	page 58	0	0	0	0	0	0	0	0
11h	ADC Ch B Volume Control	ADCB_ VOL7	ADCB_ VOL6	ADCB_ VOL5	ADCB_ VOL4	ADCB_ VOL3	ADCB_ VOL2	ADCB_ VOL1	ADCB_ VOL0
	page 58	0	0	0	0	0	0	0	0
12h	DAC1 Ch A Volume Control	DAC1A_ VOL7	DAC1A_ VOL6	DAC1A_ VOL5	DAC1A_ VOL4	DAC1A_ VOL3	DAC1A_ VOL2	DAC1A_ VOL1	DAC1A_ VOL0
	page 58	0	0	0	0	0	0	0	0
13h	DAC1 Ch B Volume Control	DAC1B_ VOL7	DAC1B_ VOL6	DAC1B_ VOL5	DAC1B_ VOL4	DAC1B_ VOL3	DAC1B_ VOL2	DAC1B_ VOL1	DAC1B_ VOL0
	page 58	0	0	0	0	0	0	0	0
14h	DAC2 Ch A Volume Control	DAC2A_ VOL7	DAC2A_ VOL6	DAC2A_ VOL5	DAC2A_ VOL4	DAC2A_ VOL3	DAC2A_ VOL2	DAC2A_ VOL1	DAC2A_ VOL0
	page 59	0	0	0	0	0	0	0	0
15h	DAC2 Ch B Volume Control	DAC2B_ VOL7	DAC2B_ VOL6	DAC2B_ VOL5	DAC2B_ VOL4	DAC2B_ VOL3	DAC2B_ VOL2	DAC2B_ VOL1	DAC2B_ VOL0
	page 59	0	0	0	0	0	0	0	0
16h	Interrupt Mode	SP2_ CLKERR1	SP2_ CLKERR0	SP1_ CLKERR1	SP1_ CLKERR0	DAC_ AMUTE1	DAC_ AMUTE0	ADC_ OVFLx1	ADC_ OVFLx0
	page 59	0	0	0	0	0	0	0	0
17h	Interrupt Mask	DAC2_ AMUTELM	DAC2_ AMUTERM	DAC1_ AMUTELM	DAC1_ AMUTERM	SP2_ CLKERRM	SP1_ CLKERRM	ADC_ OVFLPM	ADC_ OVFLNM
	page 59	0	0	0	0	0	0	0	0
18h	Interrupt Status	DAC2_ AMUTEL	DAC2_ AMUTER	DAC1_ AMUTEL	DAC1_ AMUTER	SP2_ CLKERR	SP1_ CLKERR	ADC_ OVFLP	ADC_ OVFLN
	page 61	0	0	0	0	0	0	0	0

6. REGISTER DESCRIPTION

All registers are read/write except where otherwise noted. See the following bit definition tables for bit assignment information. The default state of each bit after release of reset is listed in the shaded row of each bit description table. When writing to registers containing “Reserved” bits, all bits marked as “Reserved” must maintain their default values.

6.1 Device I.D. and Revision Register (Address 00h) *(Read Only)*

7	6	5	4	3	2	1	0
DEVICE3	DEVICE2	DEVICE1	DEVICE0	REV3	REV2	REV1	REV0

6.1.1 Device I.D. (Read Only)

I.D. code for the CS42324.

DEVICE[3:0]	Device
0110	CS42324

6.1.2 Chip Revision (Read Only)

CS42324 revision level.

REV[3:0]	Revision Level
000	A1
001	B0

6.2 Mute Control (Address 01h)

7	6	5	4	3	2	1	0
Reserved	SYS_MCLK	DAC2_ MuteL	DAC2_ MuteR	DAC1_ MuteL	DAC1_ MuteR	ADC_ MuteL	ADC_ MuteR

6.2.1 System MCLK Source

This bit selects which MCLK pin provides the clock for internal state machines. It must always be set to whichever clock is currently active.

SYS_MCLK	System MCLK source
0	MCLK1
1	MCLK2

6.2.2 Mute DAC2 Left-Channel

When set, this bit engages internal mute circuit on DAC2 output.

DAC2_MuteL	Mute status of DAC2 Left-channel
0	Un-muted
1	Muted

6.2.3 Mute DAC2 Right-Channel

When set, this bit engages internal mute circuit on DAC2 output.

DAC2_MuteR	Mute status of DAC2 Right-channel
0	Un-muted
1	Muted

6.2.4 Mute DAC1 Left-Channel

When set, this bit engages internal mute circuit on DAC1 output.

DAC1_MuteL	Mute status of DAC1 Left-channel
0	Unmuted
1	Muted

6.2.5 Mute DAC1 Right-Channel

When set, this bit engages internal mute circuit on DAC1 output.

DAC1_MuteR	Mute Status of DAC1 Right-Channel
0	Un-muted
1	Muted

6.2.6 Mute ADC Left-Channel

When set, this bit engages internal mute circuit on ADC output.

ADC_MuteL	Mute Status of ADC Left-Channel
0	Un-muted
1	Muted

6.2.7 Mute ADC Right-Channel

When set, this bit engages internal mute circuit on ADC output.

ADC_MuteR	Mute Status of ADC Right-Channel
0	Un-muted
1	Muted

6.3 Operational Control (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN	INT_H/$\overline{L}$	FREEZE	Reserved	TRI-SDOUT	TRI-SP1	TRI-SP2

6.3.1 Global Power-Down

When set, this bit places the device in power-down mode.

PDN	Device Power-Down State
0	Device is running
1	Device is in power-down mode

6.3.2 INT Pin High/Low Active (INT_H/L)

When this bit is set, the INT pin will function as an active high CMOS driver. When this bit is cleared, the INT pin will function as an active low open drain driver and will require an external pull-up resistor for proper operation.

INT_H/L	INT Pin Polarity
0	Active low, open drain driver
1	Active high, CMOS driver

6.3.3 Freeze

This function allows modifications to be made to certain bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed in Table 10.

FREEZE	FREEZE Status
0	Changes to registers take effect immediately
1	Changes to registers are held until FREEZE is released

Name	Register	Bit(s)
Mute Control	01h	7:0
ADC Ch A Vol. Control	0Fh	7:0
ADC Ch B Vol. Control	10h	7:0
DAC1 Ch A Vol. Control	11h	7:0
DAC1 Ch B Vol. Control	12h	7:0
DAC2 Ch A Vol. Control	13h	7:0
DAC2 Ch B Vol. Control	14h	7:0

Table 10. Freeze-able Bits

6.3.4 Tri-State SDOUT

When this bit is set, SDOUT will be placed in a high-impedance state.

TRI-SDOUT	SDOUT state
0	Output
1	High-impedance

6.3.5 Tri-State Serial Port 1

When enabled, and the device is configured as a master, then SCLK1 and LRCK1 of Serial Port 1 (SP1) will be placed in a high-impedance output state. If Serial Port 1 is configured as a slave, SCLK1 and LRCK1 will remain as inputs.

TRI-SP1	SCLK1 and LRCK1 State
0	SCLK1 and LRCK1 operate as inputs if Serial Port 1 is configured as a slave; SCLK1 and LRCK1 operate as outputs if Serial Port 1 is configured as a master
1	SCLK1 and LRCK1 operate as inputs if Serial Port 1 is configured as a slave; SCLK1 and LRCK1 become high-impedance outputs if Serial Port 1 is configured as a master

6.3.6 Tri-State Serial Port 2

When enabled, and the device is configured as a master, then SCLK2 and LRCK2 of Serial Port 2 (SP2) will be placed in a high-impedance output state. If Serial Port 2 is configured as a slave, SCLK2 and LRCK2 will remain as inputs. SDIN1 and SDIN2 are always configured as inputs.

TRI-SP2	SCLK2 and LRCK2 State
0	SCLK2 and LRCK2 operate as inputs if Serial Port 2 is configured as a slave; SCLK2 and LRCK2 operate as outputs if Serial Port 2 is configured as a master
1	SCLK2 and LRCK2 operate as inputs if Serial Port 2 is configured as a slave; SCLK2 and LRCK2 become high-impedance outputs if Serial Port 2 is configured as a master

6.4 Serial Port 1 Control (Address 03h)

7	6	5	4	3	2	1	0
SP1_M/$\overline{S}$	Reserved	Reserved	SP1_SPEED	MCLK1 FREQ1	MCLK1 FREQ0	Reserved	SP1_MCLK

6.4.1 Serial Port 1 Master/Slave Select

This bit configures Serial Port 1 to operate as either a clock master or clock slave.

SP1_M/$\overline{S}$	Serial Port 1 Master/Slave Select
0	Slave Mode
1	Master Mode

6.4.2 Serial Port 1 Speed Mode

In Master Mode this bit configures the speed mode of Serial Port 1.

SP1_SPEED	Serial Port 1 Speed Mode
0	Single-Speed Mode (SSM)
1	Double-Speed Mode (DSM)

6.4.3 MCLK1 Divider

These bits configure the internal MCLK1 dividers.

MCLK1 FREQ[1:0]	MCLK Divider
00	÷1
01	÷1.5
10	÷2
11	÷3

6.4.4 Serial Port 1 MCLK source

This bit selects which MCLK pin provides the clock for deriving Master Mode sub-clocks for Serial Port 1.

SP1_MCLK	Serial Port 1 MCLK source
0	MCLK1
1	MCLK2

6.5 Serial Port 2 Control (Address 04h)

7	6	5	4	3	2	1	0
SP2_M/$\overline{S}$	Reserved	Reserved0	SP2_SPEED	MCLK2 FREQ1	MCLK2 FREQ0	Reserved	SP2_MCLK

6.5.1 Serial Port 2 Master/Slave Select

This bit configures Serial Port 2 to operate as either a clock master or clock slave.

SP2_M/$\overline{S}$	Serial Port 2 Master/Slave Select
0	Slave Mode
1	Master Mode

6.5.2 Serial Port 2 Speed Mode

In Master Mode this bit configures the speed mode of Serial Port 2.

SP2_SPEED	Serial Port 2 Speed Mode
0	Single-Speed Mode (SSM)
1	Double-Speed Mode (DSM)

6.5.3 MCLK2 Divider

These bits configure the internal MCLK2 dividers.

MCLK2 FREQ[1:0]	MCLK Divider
00	÷1
01	÷1.5
10	÷2
11	÷3

6.5.4 Serial Port 2 MCLK Source

This bit selects which MCLK pin provides the clock for deriving Master Mode sub-clocks for Serial Port 2.

SP2_MCLK	Serial Port 2 MCLK source
0	MCLK1
1	MCLK2

6.6 ADC Clocking (Address 06h)

7	6	5	4	3	2	1	0
Reserved	ADC_MCLK	Reserved	ADC_SP	Reserved	Reserved	ADC_DIF1	ADC_DIF0

6.6.1 ADC MCLK source

This bit selects which MCLK pin provides the clock for the ADC.

ADC_MCLK	ADC MCLK source
0	MCLK1
1	MCLK2

6.6.2 ADC Serial Port source

This bit selects which serial port provides the sub clocks for the ADC.

ADC_SP	ADC sub clock source
0	Serial Port 1 (SCLK1/LRCK1)
1	Serial Port 2 (SCLK2/LRCK2)

6.6.3 ADC Digital Interface Format (ADC_DIF)

These bits configure the serial audio interface format for transmitting digital audio data on SDOUT

ADC_DIF[1:0]	ADC Serial Audio Interface Format
00	Left-Justified, 24-bit data
01	I²S, 24-bit data
10	Reserved
11	Reserved

6.7 DAC1 Clocking (Address 07h)

7	6	5	4	3	2	1	0
Reserved	DAC1_MCLK	Reserved	DAC1_SP	Reserved	Reserved	DAC1_DIF1	DAC1_DIF0

6.7.1 DAC1 MCLK Source

This bit selects which MCLK pin provides the clock for DAC1.

DAC1_MCLK	DAC1 MCLK source
0	MCLK1
1	MCLK2

6.7.2 DAC1 Serial Port Source

This bit selects which serial port provides the sub clocks for the DAC1.

DAC1_SP	DAC1 sub clock source
0	Serial Port 1 (SCLK1/LRCK1)
1	Serial Port 2 (SCLK2/LRCK2)

6.7.3 DAC1 Digital Interface Format (DAC1_DIF)

These bits configure the serial audio interface format for incoming digital audio data on SDIN1.

DAC1_DIF[1:0]	DAC1 Serial Audio Interface Format
00	Left-Justified, up to 24-bit data
01	I²S, up to 24-bit data
10	Right Justified, 16-bit data
11	Right Justified, 24-bit data

6.8 DAC2 Clocking (Address 08h)

7	6	5	4	3	2	1	0
Reserved	DAC2_MCLK	Reserved	DAC2_SP	Reserved	Reserved	DAC2_DIF1	DAC2_DIF0

6.8.1 DAC2 MCLK Source

This bit selects which MCLK pin provides the clock for DAC2.

DAC2_MCLK	DAC2 MCLK source
0	MCLK1
1	MCLK2

6.8.2 DAC2 Serial Port Source

This bit selects which serial port provides the sub clocks for the DAC2.

DAC2_SP	DAC2 sub clock source
0	Serial Port 1 (SCLK1/LRCK1)
1	Serial Port 2 (SCLK2/LRCK2)

6.8.3 DAC2 Digital Interface Format (DAC2_DIF)

These bits configure the serial audio interface format for incoming digital audio data on SDIN2.

DAC2_DIF[1:0]	DAC2 Serial Audio Interface Format
00	Left-Justified, up to 24-bit data
01	I²S, up to 24-bit data
10	Right Justified, 16-bit data
11	Right Justified, 24-bit data

6.9 ADC Control (Address 0Ah)

7	6	5	4	3	2	1	0
Reserved	ADC_HPFRZ	ADC_SOFT	Reserved	Reserved	AIN_SEL2	AIN_SEL1	AIN_SEL0

6.9.1 ADC High-Pass Filter Freeze

The high-pass filter works by continuously subtracting a measure of the DC offset from the output of the decimation filter. If the ADC_HPFRZ bit is taken high during normal operation, the current value of the DC offset is frozen and this DC offset will continue to be subtracted from the conversion result. For DC measurements, this bit must be set to ‘1’.

ADC_HPFRZ	ADC High-Pass Filter Freeze
0	Continuous DC Subtraction
1	Fixed DC Subtraction

6.9.2 ADC Soft Ramp Control

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

ADC_SOFT	ADC Soft Ramp Control
0	Off
1	On

6.9.3 Analog Input Selection

These bits are used to select the input source for the ADC.

AIN_SEL[2:0]	ADC Soft Ramp Control
000	Reserved
001	Line-Level Input Pair 1
010	Line-Level Input Pair 2
011	Line-Level Input Pair 3
100	Line-Level Input Pair 4
101	Line-Level Input Pair 5
110	Reserved
111	Reserved

6.10 DAC1 Control (Address 0Bh)

7	6	5	4	3	2	1	0
DAC1_DEPH	DAC1_SNGVOL	DAC1_SOFT	DAC1_ZC	DAC1_LOOPBACK	DAC1_INV	DAC1_MIX1	DAC1_MIX0

6.10.1 DAC1 De-Emphasis Control

This bit enables the digital filter to apply the standard 15µs/50µs digital de-emphasis filter response for a sample rate (Fs) of 44.1 kHz. De-emphasis is available only in Single-Speed Mode.

DAC1_DEPH	DAC1 De-Emphasis Control
0	Off
1	On (valid for Fs = 44.1 kHz)

6.10.2 DAC1 Single Volume Control

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on DAC1 channels is determined by the DAC1A Volume Control register and the DAC1B Volume Control register is ignored.

DAC1_SNGVOL	DAC1 Single Volume Control
0	Off
1	On

6.10.3 DAC1 Soft Ramp Control

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

DAC1_SOFT	DAC1 Soft Ramp Control
0	Off
1	On

6.10.4 DAC1 Zero Cross Control

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

DAC1_SOFT	DAC1_ZC	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled

6.10.5 DAC1 Loop-Back

Loops ADC SDOUT, SCLK, and LRCK to DAC1 serial port pins.

DAC1_LOOP_BACK	DAC1 Loop-Back
0	Off
1	On

6.10.6 DAC1 Invert Signal Polarity

When enabled, this bit will effect a 180 degree phase shift in the DAC1 channels.

DAC1_INV	DAC1 Invert Signal Polarity
0	Off
1	On

6.10.7 DAC1 Channel Mixer

These bits implement mono mixes of the left and right channels as well as a left/right channel swap.

DAC1_MIX[1:0]	DAC1 OUTA	DAC1 OUTB
00	L	R
01	$\frac{L+R}{2}$	$\frac{L+R}{2}$
10		
11	R	L

6.11 DAC2 Control (Address 0Ch)

7	6	5	4	3	2	1	0
DAC2_DEPH	DAC2_ SNGVOL	DAC2_SOFT	DAC2_ZC	DAC2_ LOOP_BACK	DAC2_INV	DAC2_MIX1	DAC2_MIX0

6.11.1 DAC2 De-Emphasis Control

This bit enables the digital filter to apply the standard 15µs/50µs digital de-emphasis filter response for a sample rate (Fs) of 44.1 kHz. De-emphasis is available only in Single-Speed Mode.

DAC2_DEPH	DAC2 De-Emphasis Control
0	Off
1	On (valid for Fs = 44.1 kHz)

6.11.2 DAC2 Single Volume Control

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on DAC2 channels is determined by the DAC2A Volume Control register and the DAC2B Volume Control register is ignored.

DAC2_SNGVOL	DAC2 Single Volume Control
0	Off
1	On

6.11.3 DAC2 Soft Ramp Control

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

DAC2_SOFT	DAC2 Soft Ramp Control
0	Off
1	On

6.11.4 DAC2 Zero Cross Control

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

DAC2_SOFT	DAC2_ZC	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled

6.11.5 DAC2 Loop-Back

Loops ADC SDOUT, SCLK, and LRCK to DAC1 serial port pins.

DAC2_LOOP_BACK	DAC2 Loop-Back
0	Off
1	On

6.11.6 DAC2 Invert Signal Polarity

When enabled, this bit will effect a 180 degree phase shift in the DAC2 channels.

DAC2_INV	DAC2 Invert Signal Polarity
0	Off
1	On

6.11.7 DAC2 Channel Mixer

These bits implements mono mixes of the left and right channels as well as a left/right channel swap.

DAC2_MIX[1:0]	DAC2 OUTA	DAC2 OUTB
00	L	R
01	$\frac{L+R}{2}$	$\frac{L+R}{2}$
10		
11	R	L

6.12 AOUT1 Control (Address 0Dh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MUTEC1	AOUT1_SEL2	AOUT1_SEL1	AOUT1_SEL0

6.12.1 External Mute Control Pin

This bit controls the logic state of the corresponding $\overline{\text{MUTEC1}}$ pin. Though this bit is active high, it should be noted that the $\overline{\text{MUTEC1}}$ pin is active low.

MUTEC1	Output on $\overline{\text{MUTEC1}}$ pin
0	High (Mute Disengaged)
1	Low (Mute Engaged)

6.12.2 AOUT1 Select

These bits are used to select the analog output source.

AOUT1_SEL[2:0]	AOUT1 Source
000	Reserved
001	AIN Pair 1
010	AIN Pair 2
011	AIN Pair 3
100	AIN Pair 4
101	AIN Pair 5
110	DAC1 Output Pair
111	DAC2 Output Pair

6.13 AOUT2 Control (Address 0Eh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MUTEC2	AOUT2_SEL2	AOUT2_SEL1	AOUT2_SEL0

6.13.1 External Mute Control Pin

This bit controls the logic state of the corresponding $\overline{\text{MUTEC2}}$ pin. Though this bit is active high, it should be noted that the $\overline{\text{MUTEC2}}$ pin is active low.

MUTEC2	Output on $\overline{\text{MUTEC2}}$ pin
0	High (Mute Disengaged)
1	Low (Mute Engaged)

6.13.2 AOUT2 Select

These bits are used to select the analog output source.

AOUT2_SEL[2:0]	AOUT2 Source
000	Reserved
001	AIN Pair 1
010	AIN Pair 2
011	AIN Pair 3
100	AIN Pair 4
101	AIN Pair 5
110	DAC1 Output Pair
111	DAC2 Output Pair

6.14 AOUT3 Control (Address 0Fh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MUTEC3	AOUT3_SEL2	AOUT3_SEL1	AOUT3_SEL0

6.14.1 External Mute Control Pin

This bit controls the logic state of the corresponding $\overline{\text{MUTEC3}}$ pin. Though this bit is active high, it should be noted that the $\overline{\text{MUTEC3}}$ pin is active low.

MUTEC3	Output on $\overline{\text{MUTEC3}}$ pin
0	High (Mute Disengaged)
1	Low (Mute Engaged)

6.14.2 AOUT3 Select

These bits are used to select the analog output source.

AOUT3_SEL[2:0]	AOUT3 Source
000	Reserved
001	AIN Pair 1
010	AIN Pair 2
011	AIN Pair 3
100	AIN Pair 4
101	AIN Pair 5
110	DAC1 Output Pair
111	DAC2 Output Pair

6.15 ADCx Volume Control: ADCA (Address 10h) & ADCB (Address 11h)

7	6	5	4	3	2	1	0
ADCx_VOL7	ADCx_VOL6	ADCx_VOL5	ADCx_VOL4	ADCx_VOL3	ADCx_VOL2	ADCx_VOL1	ADCx_VOL0

The level for each channel of the ADC can be adjusted in 0.5 dB increments as dictated by the ADC Soft and Zero Cross bits (ADC_SOFT) from +12 to -84 dB. Levels are decoded in two's complement, as shown in the table below.

Binary Code	Volume Setting
0001 1000	+12.0 dB
...	...
0000 0000	0.0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0101 1000	-84.0 dB
All other values	Reserved

6.16 DAC1x Volume Control: DAC1A (Address 12h) & DAC1B (Address 13h)

7	6	5	4	3	2	1	0
DAC1x_VOL7	DAC1x_VOL6	DAC1x_VOL5	DAC1x_VOL4	DAC1x_VOL3	DAC1x_VOL2	DAC1x_VOL1	DAC1x_VOL0

The level for each channel of DAC1 output can be adjusted in 0.5 dB increments as dictated by the DAC1 Soft and Zero Cross bits (DAC1_SOFT & DAC1_ZC) from 0 to -127.5 dB. Levels are decoded as unsigned, as shown in the table below.

Binary Code	Volume Setting
0000 0000	0 dB
0000 0001	-0.5 dB
0000 0010	-1.0 dB
...	...
1111 1111	-127.5 dB

6.17 DAC2x Volume Control: DAC1A (Address 14h) & DAC1B (Address 15h)

7	6	5	4	3	2	1	0
DAC2x_VOL7	DAC2x_VOL6	DAC2x_VOL5	DAC2x_VOL4	DAC2x_VOL3	DAC2x_VOL2	DAC2x_VOL1	DAC2x_VOL0

The level for each channel of DAC2 output can be adjusted in 0.5 dB increments as dictated by the DAC2 Soft and Zero Cross bits (DAC2_SOFT & DAC2_ZC) from 0 to -127.5 dB. Levels are decoded in unsigned, as shown in the table below.

Binary Code	Volume Setting
0000 0000	0 dB
0000 0001	-0.5 dB
0000 0010	-1.0 dB
...	...
1111 1111	-127.5 dB

6.18 Interrupt Mode (Address 16h)

7	6	5	4	3	2	1	0
SP2_ CLKERR1	SP2_ CLKERR0	SP1_ CLKERR1	SP1_ CLKERR0	DAC_AMUTE1	DAC_AMUTE0	ADC_ OVFLx1	ADC_ OVFLx0

The Interrupt Mode register contains four two-bit codes which correspond to either an Interrupt Status bit or group of bits as shown below. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising-edge Active Mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling-edge Active Mode, the INT pin becomes active on the removal of the interrupt condition. In Level Active Mode, the INT pin remains active during the interrupt condition .

Interrupt Mode	Associated Interrupt Status Bit(s)
SP2_CLKERR[1:0]	SP2_CLKERR
SP1_CLKERR[1:0]	SP1_CLKERR
DAC_AMUTE[1:0]	DAC2_AMUTEL, DAC2_AMUTER, DAC1_AMUTEL, DAC1_AMUTER
ADC_AVFLx[1:0]	ADC_OVFLP, ADC_OVFLN

Bit Settings	Interrupt Mode Setting
00	Rising-edge Active
01	Falling-edge Active
10	Level Active
11	Reserved

6.19 Interrupt Mask (Address 17h)

7	6	5	4	3	2	1	0
DAC2_ AMUTELM	DAC2_ AMUTERM	DAC1_ AMUTELM	DAC1_ AMUTERM	SP2_ CLKERRM	SP1_ CLKERRM	ADC_ OVFLPM	ADC_ OVFLNM

These bits are mask bits for the corresponding bits in the “Interrupt Status (Address 18h) (Read Only)” register on page 61.

Bit Settings	Bit in Interrupt Register
0	Not Masked
1	Masked

6.19.1 DAC2 Auto Mute Left Mask (DAC2_AMUTELM)

This bit serves as a mask for the DAC2 Auto Mute Left interrupt source. If this bit is cleared, the DAC2_AMUTEL interrupt is unmasked, meaning that if the DAC2_AMUTEL condition occurs, the INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the DAC2_AMUTELM bit is set, the DAC2_AMUTEL condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.2 DAC2 Auto Mute Right Mask (DAC2_AMUTERM)

This bit serves as a mask for the DAC2 Auto Mute Left interrupt source. If this bit is cleared, the DAC2_AMUTER interrupt is unmasked, meaning that if the DAC2_AMUTER condition occurs, the INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the DAC2_AMUTERM bit is set, the DAC2_AMUTER condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.3 DAC1 Auto Mute Left Mask (DAC1_AMUTELM)

This bit serves as a mask for the DAC1 Auto Mute Left interrupt source. If this bit is cleared, the DAC1_AMUTEL interrupt is unmasked, meaning that if the DAC1_AMUTEL condition occurs, the INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the DAC1_AMUTELM bit is set, the DAC1_AMUTEL condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.4 DAC1 Auto Mute Right Mask (DAC1_AMUTELM)

This bit serves as a mask for the DAC1 Auto Mute Left interrupt source. If this bit is cleared, the DAC1_AMUTER interrupt is unmasked, meaning that if the DAC1_AMUTER condition occurs, the INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the DAC1_AMUTERM bit is set, the DAC1_AMUTER condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.5 Serial Port 2 Clock Error Mask (SP2_CLKERRM)

This bit serves as a mask for the serial port 2 clock error interrupt source. If this bit is cleared, the SP2_CLKERR interrupt is unmasked, meaning that if the SP2_CLKERR bit is set, the INT pin will go active according to the SP2_CLKERR[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the SP2_CLKERRM bit is set, the SP2_CLKERR condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.6 Serial Port 1 Clock Error Mask (SP1_CLKERRM)

This bit serves as a mask for the serial port 1 clock error interrupt source. If this bit is cleared, the SP1_CLKERR interrupt is unmasked, meaning that if the SP1_CLKERR bit is set, the INT pin will go active according to the SP1_CLKERR[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the SP1_CLKERRM bit is set, the SP1_CLKERR condition is masked, meaning that its occurrence will not affect the INT pin.

6.19.7 ADC Positive Overflow Mask (ADC_OVFLPM)

This bit serves as a mask for the ADC positive overflow interrupt source. If this bit is cleared, the ADC_OVFLP interrupt is unmasked, meaning that if the ADC_OVFLP conditions are met in the interrupt status register, the INT pin will go active according to the ADC_OVFLx[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the ADC_OVFLPM bit is set, the ADC_OVFLP condition is masked, meaning that its occurrence will not affect the INT pin. However, the OVFL pin will continue to reflect the overflow state of the ADC.

6.19.8 ADC Negative Overflow Mask (ADC_OVFLNM)

This bit serves as a mask for the ADC negative overflow interrupt source. If this bit is cleared, the ADC_OVFLN interrupt is unmasked, meaning that if the ADC_OVFLN conditions are met in the interrupt status register, the INT pin will go active according to the ADC_OVFLx[1:0] bits in the "Interrupt Mode (Address 16h)" register on page 59. If the ADC_OVFLNM bit is set, the ADC_OVFLN condition is masked, meaning that its occurrence will not affect the INT pin. However, the OVFL pin will continue to reflect the overflow state of the ADC.

6.20 Interrupt Status (Address 18h) *(Read Only)*

7	6	5	4	3	2	1	0
DAC2_ AMUTEL	DAC2_ AMUTER	DAC1_ AMUTEL	DAC1_ AMUTER	SP2_ CLKERR	SP1_ CLKERR	ADC_ OVFLP	ADC_ OVFLN

This register defaults to 00h and is read only. If the INT pin is active, reading this register clears the interrupt condition.

Bit Settings	Bit in Interrupt Register
0	Interrupt has not occurred since the last read of this register.
1	Interrupt has occurred since the last read of this register.

6.20.1 DAC2 Auto Mute Left Interrupt Status (DAC2_AMUTEL)

This bit is read only. When set, indicates that DAC2 left channel has had an auto-mute condition since the last read of this register. Conditions which cause an auto-mute, such as receiving 4096 consecutive samples of zeroes or ones on the left channel of SDIN2, will cause this bit to be set. This interrupt status bit is an edge-triggered event and will be cleared following a read of this register.

The INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if DAC2_AMUTELM bit is cleared.

6.20.2 DAC2 Auto Mute Right Interrupt Status (DAC2_AMUTER)

This bit is read only. When set, indicates that DAC2 right channel has had an auto-mute condition since the last read of this register. Conditions which cause an auto-mute, such as receiving 4096 consecutive samples of zeroes or ones on the right channel of SDIN2, will cause this bit to be set. This interrupt status bit is an edge-triggered event and will be cleared following a read of this register.

The INT pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if DAC2_AMUTERM bit is cleared.

6.20.3 DAC1 Auto Mute Left Interrupt Status (DAC1_AMUTEL)

This bit is read only. When set, indicates that DAC1 left channel has had an auto-mute condition since the last read of this register. Conditions which cause an auto-mute, such as receiving 4096 consecutive samples of zeroes or ones on the left channel of SDIN1, will cause this bit to be set. This interrupt status bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if DAC1_AMUTELM bit is cleared.

6.20.4 DAC1 Auto Mute Right Interrupt Status (DAC1_AMUTEL)

This bit is read only. When set, indicates that DAC1 right channel has had an auto-mute condition since the last read of this register. Conditions which cause an auto-mute, such as receiving 4096 consecutive samples of zeroes or ones on the right channel of SDIN1, will cause this bit to be set. This interrupt status bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the DAC_AMUTE[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if DAC1_AMUTERM bit is cleared.

6.20.5 Serial Port 2 Clock Error Interrupt Status (SP2_CLKERR)

This bit is read only. When set, indicates that Serial Port 2 has had a clock error since the last read of this register. Conditions which cause a clock error in the serial port, such as loss of LRCK2, SCLK2, an MCLKx/LRCK2 ratio change, or speed mode change, will cause this bit to be set. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the SP2_CLKERR[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if SP2_CLKERRM bit is cleared.

6.20.6 Serial Port 1 Clock Error Interrupt Status (SP1_CLKERR)

This bit is read only. When set, indicates that Serial Port 1 has had a clock error since the last read of this register. Conditions which cause a clock error in the serial port, such as loss of LRCK1, SCLK1, an MCLKx/LRCK1 ratio change, or speed mode change, will cause this bit to be set. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the SP1_CLKERR[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if SP1_CLKERRM bit is cleared.

6.20.7 ADC Positive Overflow Interrupt Bit (ADC_OVFLP)

This bit is read only. When set, indicates that a positive over-range condition occurred anywhere in the CS42324 ADC signal path and has ADC data has been clipped to positive full scale since the last read of this register. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the ADC_OVFLx[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if ADC_OVFLPM bit is cleared. To determine the current overflow state of the ADC use the $\overline{\text{OVFL}}$ pin.

6.20.8 ADC Negative Overflow Interrupt Bit (ADC_OVFLN)

This bit is read only. When set, indicates that a negative over-range condition occurred anywhere in the CS42324 ADC signal path and has ADC data has been clipped to negative full scale since the last read of this register. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

The $\overline{\text{INT}}$ pin will go active according to the ADC_OVFLx[1:0] bits in the "Interrupt Mode (Address 16h)" on page 59 and the status of this bit if ADC_OVFLNM bit is cleared. To determine the current overflow state of the ADC use the $\overline{\text{OVFL}}$ pin.

7. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-resolution converter, the CS42324 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 7 on page 26 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply (VL) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD.

Power supply decoupling capacitors should be as near to the CS42324 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+, VCM_ADC, VBIAS, VCMBUF, and VCMDAC pins in order to avoid unwanted coupling into the modulators. The FILT+, VCM_ADC, VBIAS, VCMBUF, and VCMDAC decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from each pin to GND. The CS42324 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS42324 digital outputs only to CMOS inputs.

8. ADC FILTER PLOTS

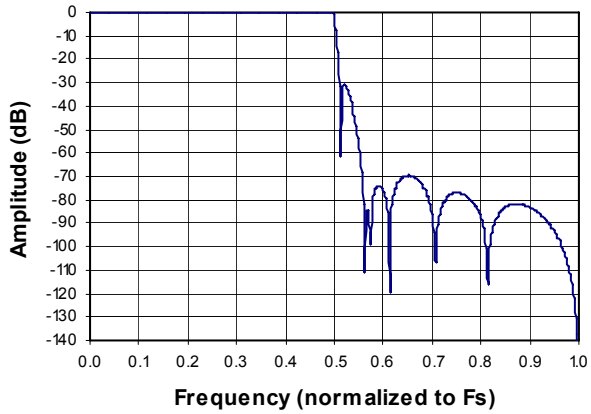


Figure 23. Single-Speed Mode Stopband Rejection

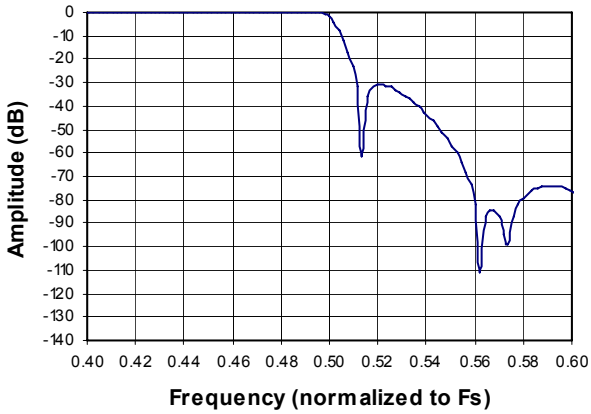


Figure 24. Single-Speed Mode Transition Band

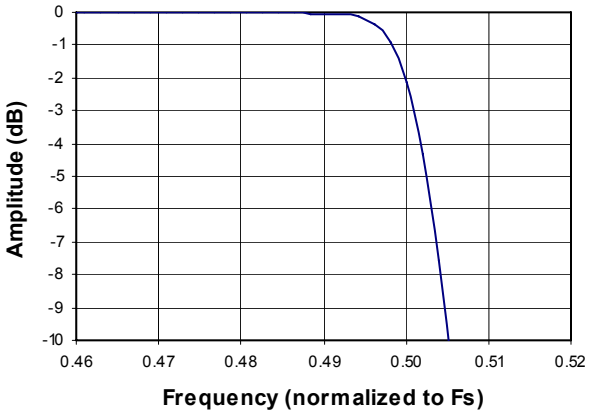


Figure 25. Single-Speed Mode Transition Band (Detail)

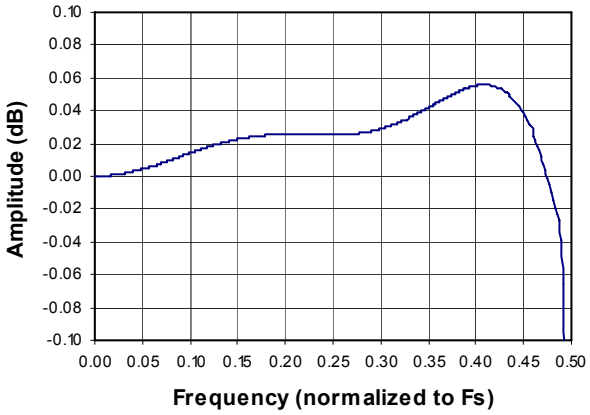


Figure 26. Single-Speed Mode Passband Ripple

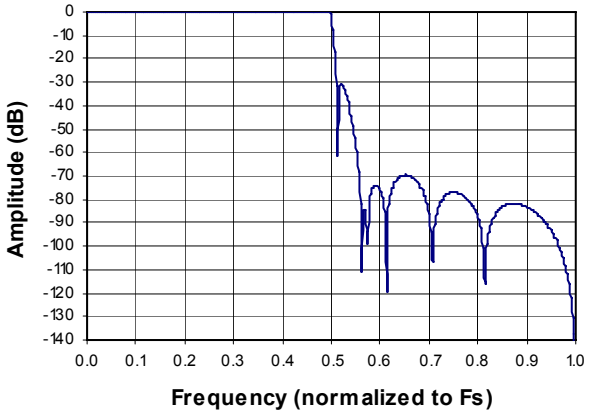


Figure 27. Double-Speed Mode Stopband Rejection

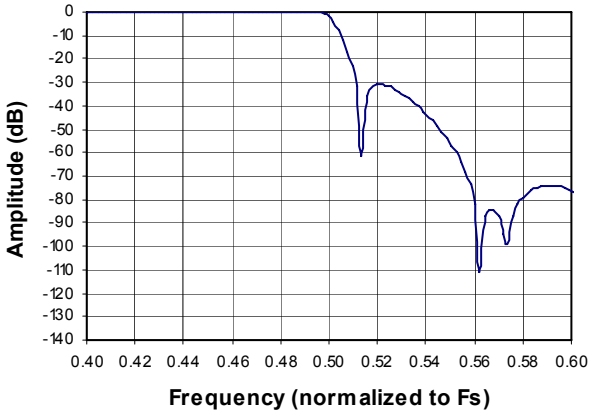


Figure 28. Double-Speed Mode Transition Band

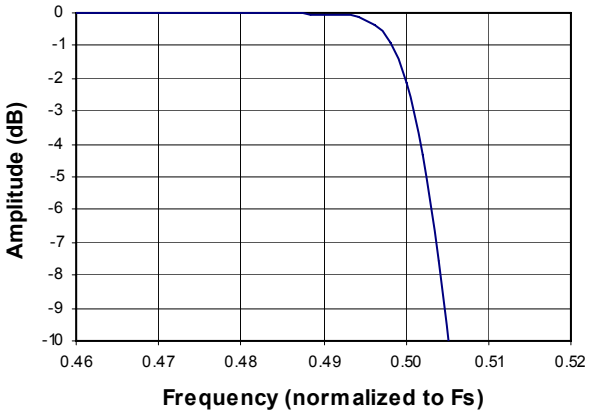


Figure 29. Double-Speed Mode Transition Band (Detail)

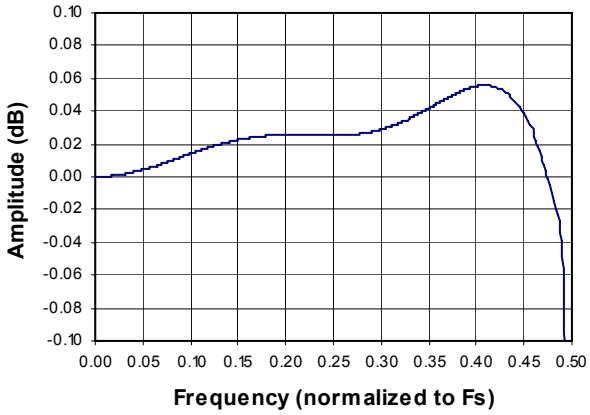


Figure 30. Double-Speed Mode Passband Ripple

9. DAC DIGITAL FILTER RESPONSE PLOTS

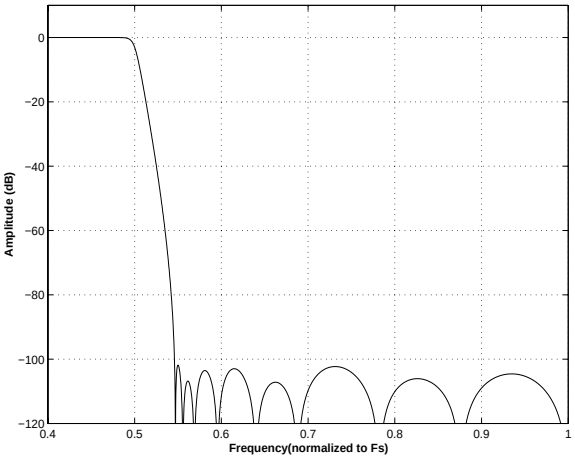


Figure 31. Single-Speed Stopband Rejection

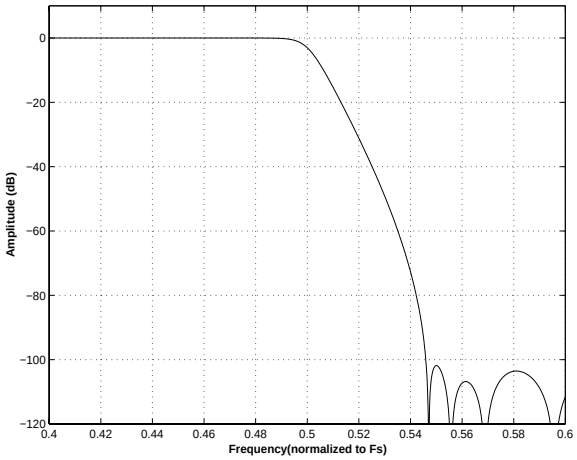


Figure 32. Single-Speed Transition Band

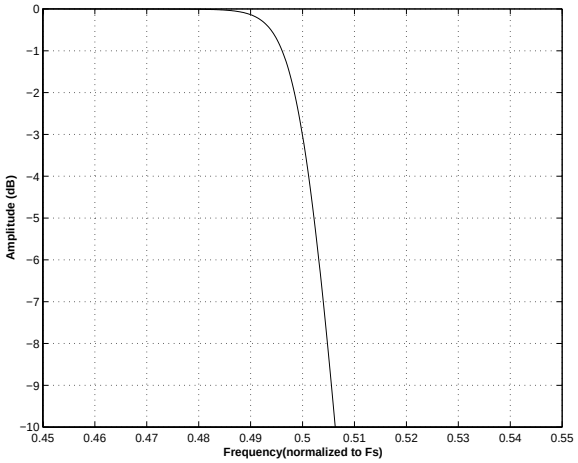


Figure 33. Single-Speed Transition Band (detail)

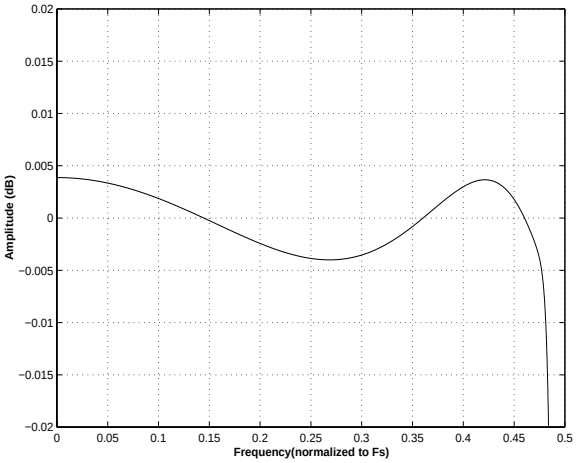


Figure 34. Single-Speed Passband Ripple

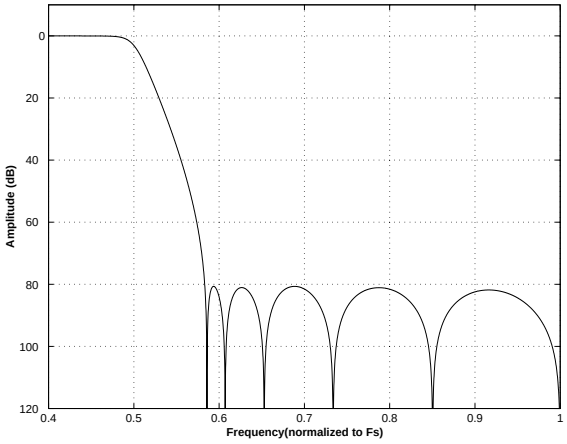


Figure 35. Double-Speed Stopband Rejection

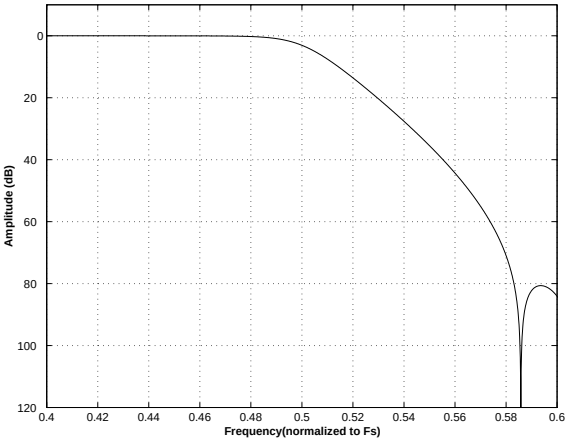


Figure 36. Double-Speed Transition Band

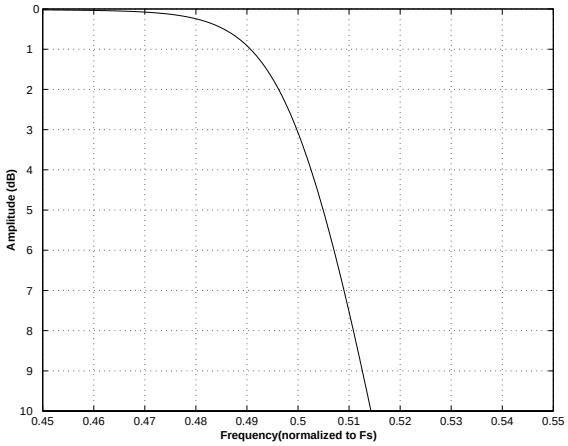


Figure 37. Double-Speed Transition Band (detail)

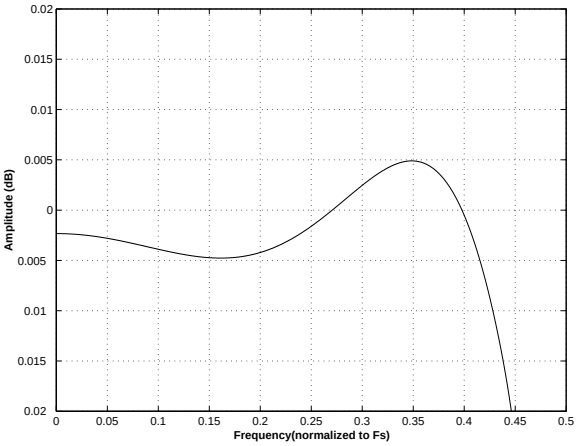


Figure 38. Double-Speed Passband Ripple

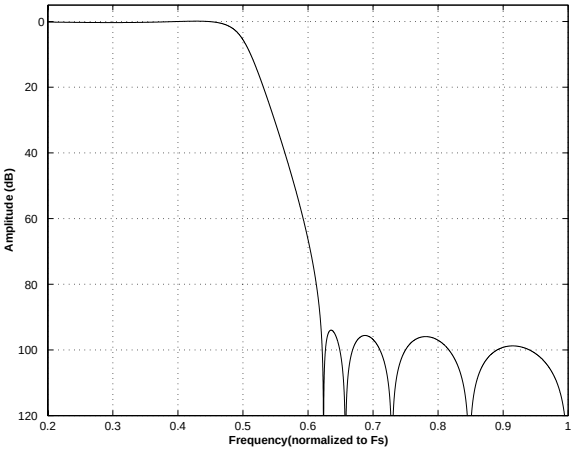


Figure 39. Quad-Speed Stopband Rejection

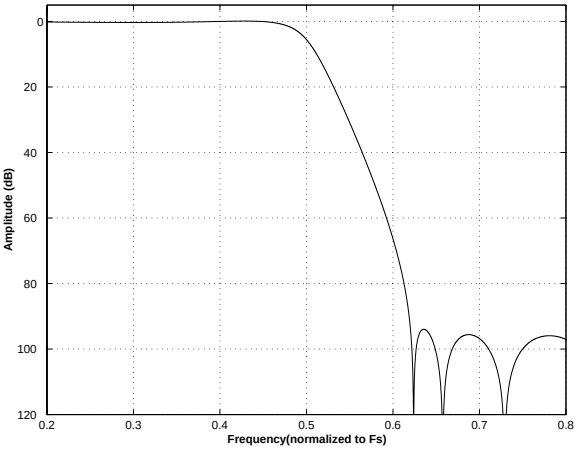


Figure 40. Quad-Speed Transition Band

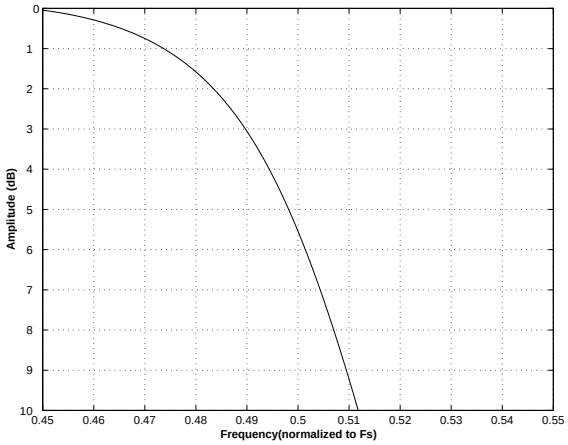


Figure 41. Quad-Speed Transition Band (detail)

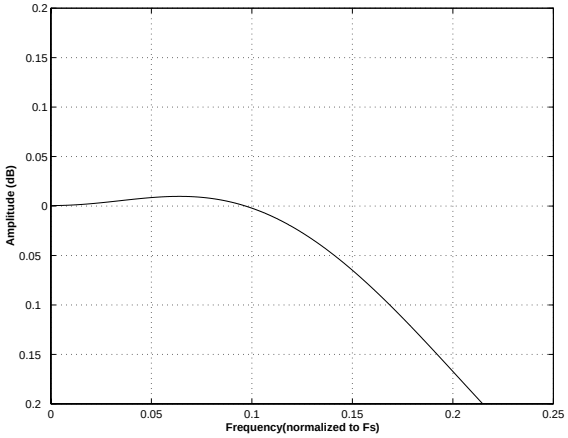


Figure 42. Quad-Speed Passband Ripple

10.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

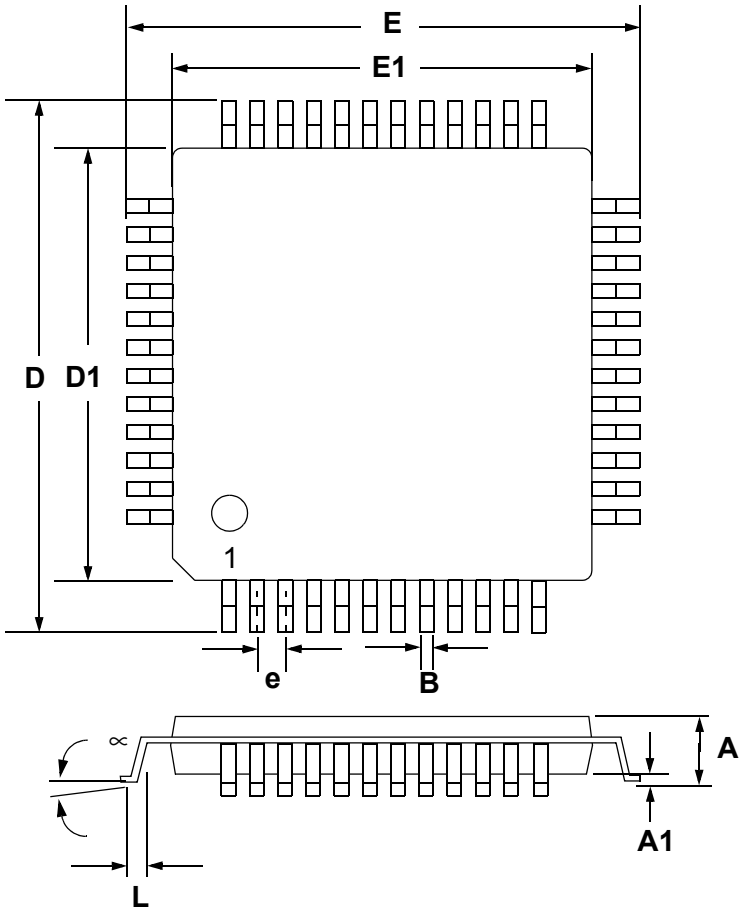
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

11.PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
µ	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm *Controlling dimension is mm. *JEDEC Designation: MS022

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance	multi-layer	θ_{JA}	-	48	-	°C/Watt
	dual-layer	θ_{JA}	-	65	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42324	2-In, 4-Out Audio CODEC with 2Vrms Analog I/O	LQFP	Yes	Commercial	-40° to +85° C	Tray	CS42324-CQZ
CS42324	2-In, 4-Out Audio CODEC with 2Vrms Analog I/O	LQFP	Yes	Automotive	-40° to +105° C	Tray	CS42324-DQZ
CDB42324	Evaluation Board		-	-	-	-	CDB42324

13.REVISION HISTORY

Release	Changes
A3	Added documentation for new clocking functionality for the CS42324 rev B Changed naming convention for pins and registers Added Automotive ordering option
A4	Corrected default bit values for registers 01h, 02h, 06h, 07h, and 08h.
A5	Changed Title

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.