

### FEATURES

- High dynamic range, dual DAC parts
- Low noise and intermodulation distortion
- Single carrier WCDMA ACLR = 80 dBc @ 61.44 MHz IF
- Innovative switching output stage permits useable outputs beyond Nyquist frequency
- LVC MOS inputs with dual-port or optional interleaved single-port operation
- Differential analog current outputs are programmable from 8.6 mA to 31.7 mA full scale
- Auxiliary 10-bit current DACs with source/sink capability for external offset nulling
- Internal 1.2 V precision reference voltage source
- Operates from 1.8 V and 3.3 V supplies
- 315 mW power dissipation
- Small footprint, RoHS compliant, 72-lead LFCSP

### APPLICATIONS

- Wireless infrastructure
- WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Wideband communications
- LMDS/MMDS, point-to-point
- RF signal generators, arbitrary waveform generators

### GENERAL DESCRIPTION

The AD9780/AD9781/AD9783 include pin-compatible, high dynamic range, dual digital-to-analog converters (DACs) with 12-/14-/16-bit resolutions, and sample rates of up to 600 MSPS. The devices include specific features for direct conversion transmit applications, including gain and offset compensation, and they interface seamlessly with analog quadrature modulators such as the [ADL5370](#).

A proprietary, dynamic output architecture permits synthesis of analog outputs even above Nyquist by shifting energy away from the fundamental and into the image frequency.

Full programmability is provided through a serial peripheral interface (SPI) port. Some pin-programmable features are also offered for those applications without a controller.

### PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) enables high quality synthesis of wideband signals.
2. Proprietary switching output for enhanced dynamic performance.
3. Programmable current outputs and dual auxiliary DACs provide flexibility and system enhancements.

### FUNCTIONAL BLOCK DIAGRAM

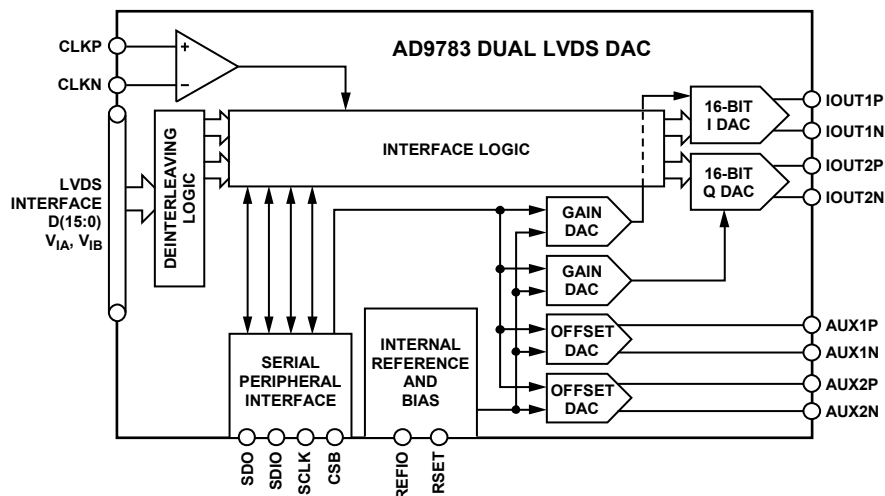


Figure 1

### Rev. PrG

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## TABLE OF CONTENTS

Features .....	1	General Operation of the Serial Interface .....	18
Applications .....	1	Instruction Byte .....	18
General Description .....	1	MSB/LSB Transfers .....	19
Product Highlights .....	1	Serial Interface Port Pin Descriptions .....	19
Functional Block Diagram .....	1	SPI Register Map .....	20
Specifications .....	3	SPI Register Descriptions .....	21
DC Specifications .....	3	SPI Port, RESET, and Pin Mode .....	23
Digital Specifications .....	4	Parallel Data Port Interface .....	23
AC Specifications .....	4	Optimizing the Parallel Port Timing .....	23
Absolute Maximum Ratings .....	5	Driving the CLK Input .....	25
Thermal Resistance .....	5	Full-Scale Current Generation .....	25
ESD Caution .....	5	DAC Transfer Function .....	26
Pin Configuration and Function Descriptions .....	6	Analog Modes of Operation .....	26
Typical Performance Characteristics .....	9	Power Dissipation .....	27
Terminology .....	17	Outline Dimensions .....	29
Theory of Operation .....	18	Ordering Guide .....	29
Serial Peripheral Interface .....	18		

## SPECIFICATIONS

### DC SPECIFICATIONS

$T_{\text{MIN}}$  to  $T_{\text{MAX}}$ ,  $AVDD33 = 3.3 \text{ V}$ ,  $DVDD33 = 3.3 \text{ V}$ ,  $DVDD18 = 1.8 \text{ V}$ ,  $CVDD18 = 1.8 \text{ V}$ ,  $I_{\text{OUTFS}} = 20 \text{ mA}$  maximum sample rate, unless otherwise noted.

Table 1.

Parameter	AD9780			AD9781			AD9783			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		$\pm 0.13$			$\pm 0.5$			$\pm 2$		LSB
Integral Nonlinearity (INL)		$\pm 0.25$			$\pm 1$			$\pm 4$		LSB
MAIN DAC OUTPUTS										
Offset Error	-0.001	0	+0.001	-0.001	0	+0.001	-0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		$\pm 2$			$\pm 2$			$\pm 2$		% FSR
Full-Scale Output Current <sup>1</sup>	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	V
Output Resistance		10			10			10		M $\Omega$
Gain DAC Monotonicity Guaranteed										
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/ $^{\circ}\text{C}$
Gain		100			100			100		ppm/ $^{\circ}\text{C}$
Reference Voltage		30			30			30		ppm/ $^{\circ}\text{C}$
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current	-2		+2	-2		+2	-2		+2	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		M $\Omega$
AUX DAC Monotonicity Guaranteed										
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		k $\Omega$
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION										
$f_{\text{DAC}} = 500 \text{ MSPS}$ , $I_{\text{F}} = 20 \text{ MHz}$		$V \times I$	$V \times I$		$V \times I$	$V \times I$		$V \times I$	$V \times I$	mW
$f_{\text{DAC}} = 600 \text{ MSPS}$ , $I_{\text{F}} = 10 \text{ MHz}$		440			440			440		mW
Power-Down Mode		3	5		3	5		3	35	mW
SUPPLY CURRENTS <sup>2</sup>										
AVDD33		55	58		55	58		55	58	mA
CVDD18		34	38		34	38		34	38	mA
DVDD33		13	15		13	15		13	15	mA
DVDD18		68	85		68	85		68	85	mA

<sup>1</sup> Based on a 10 k $\Omega$  external resistor.

<sup>2</sup>  $F_{\text{DAC}} = 500 \text{ MSPS}$ ,  $F_{\text{OUT}} = 20 \text{ MHz}$ .

**DIGITAL SPECIFICATIONS**

$T_{MIN}$  to  $T_{MAX}$ ,  $AVDD33 = 3.3$  V,  $DVDD33 = 3.3$  V,  $DVDD18 = 1.8$  V,  $CVDD18 = 1.8$  V,  $I_{OUTFS} = 20$  mA, maximum sample rate, unless otherwise noted.

**Table 2.**

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKP, CLKN)				
Peak-to-Peak Voltage at CLKP and CLKN	400	800	1600	mV
Common-Mode Voltage	300	400	500	mV
Maximum Clock Rate	600			MSPS
SERIAL PERIPHERAL INTERFACE (CMOS Interface)				
Maximum Clock Rate (SCLK)			40	MHz
Minimum Pulse Width High			12.5	ns
Minimum Pulse Width Low			12.5	ns
DIGITAL INPUT DATA (LVDS Interface)				
Input Voltage Range, $V_{IA}$ or $V_{IB}$	800		1600	mV
Input Differential Threshold, $V_{IDTH}$	-100		+100	mV
Input Differential Hysteresis, $V_{IDTHL}$ to $V_{IDTHH}$		20		mV
Input Differential Input Impedance,	80		120	$\Omega$
Maximum LVDS Input Rate (Per DAC)	600			MSPS

**AC SPECIFICATIONS**

$T_{MIN}$  to  $T_{MAX}$ ,  $AVDD33 = 3.3$  V,  $DVDD33 = 3.3$  V,  $DVDD18 = 1.8$  V,  $CVDD18 = 1.8$  V,  $I_{OUTFS} = 20$  mA, maximum sample rate, unless otherwise noted.

**Table 3.**

Parameter	AD9780			AD9781			AD9783			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
$f_{DAC} = 600$ MSPS, $f_{OUT} = 20$ MHz		79			78			80		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 120$ MHz		67			66			68		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 480$ MHz (Mix Mode)		58			62			59		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 580$ MHz (Mix Mode)		58			56			60		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
$f_{DAC} = 600$ MSPS, $f_{OUT} = 20$ MHz		91			93			86		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 120$ MHz		80			75			79		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 480$ MHz (Mix Mode)		60.5			61.5			66		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 580$ MHz (Mix Mode)		58			59			59		dBc
NOISE SPECTRAL DENSITY (NSD) One-Tone										
$f_{DAC} = 600$ MSPS, $f_{OUT} = 40$ MHz		-157			-162			-165		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 120$ MHz		-154.5			-156.5			-157		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 480$ MHz (Mix Mode)		-152			-152			-153		dBc
$f_{DAC} = 600$ MSPS, $f_{OUT} = 580$ MHz (Mix Mode)		-152			-151			-152		dBc
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
$f_{DAC} = 491.52$ MSPS, $f_{OUT} = 20$ MHz		-81			-82.5			-82		dBc
$f_{DAC} = 491.52$ MSPS, $f_{OUT} = 80$ MHz		-80			-82.5			-81		dBc
$f_{DAC} = 491.52$ MSPS, $f_{OUT} = 411.52$ MHz		-71			-68			-69		dBc
$f_{DAC} = 491.52$ MSPS, $f_{OUT} = 471.52$ MHz		-69			-69			-70		dBc

## ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect to	Rating
AVDD33, DVDD33	AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD18, CVDD18	AGND, DGND, CGND	−0.3 V to +1.98 V
AGND	DGND, CGND	−0.3 V to +0.3 V
DGND	AGND, CGND	−0.3 V to +0.3 V
CGND	AGND, DGND	−0.3 V to +0.3 V
REFIO	AGND	−0.3 V to AVDD33 + 0.3 V
IOUT1P, IOUT1N, IOUT2P, IOUT2N, AUX1P, AUX1N, AUX2P, AUX2N	AGND	−1.0 V to AVDD33 + 0.3 V
D15 to D0	DGND	−0.3 V to DVDD33 + 0.3 V
CLKP, CLKN	CGND	−0.3 V to CVDD18 + 0.3 V
CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature		−65°C to +150°C

## THERMAL RESISTANCE

Thermal resistance tested using JEDEC standard 4-layer thermal test board with no airflow.

Table 5.

Package Type	$\theta_{JA}$	Unit
CP-72-1 (Exposed Pad Soldered to PCB)	25	°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

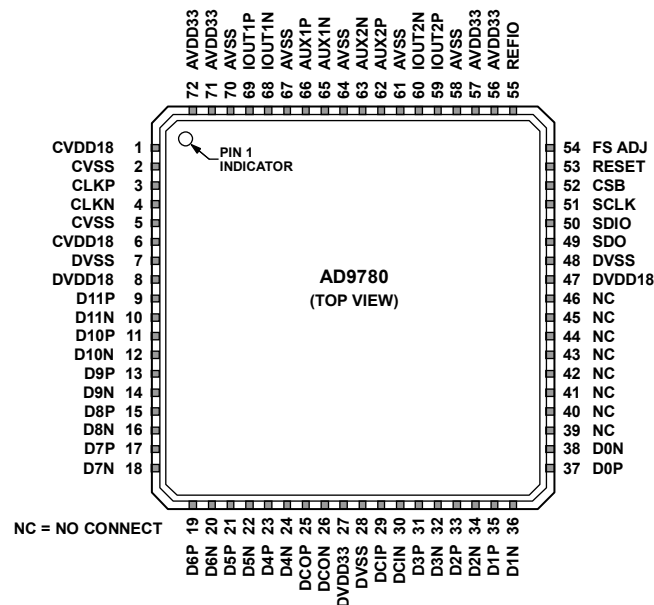


Figure 2. AD9780 Pin Configuration

Table 6. AD9780 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Return.
3, 4	CLKP, CLKN	Differential DAC Sampling Clock Input.
7, 28, 48	DVSS	Digital Common.
8, 47	DVDD18	Digital Supply Voltage (1.8 V).
9, 10	D11P, D11N	LVDS Data Input (MSB)
11 to 24, 31 to 36	D10P to D1P, D10N to D1N	LVDS Data Inputs.
25, 26	DCOP, DCON	Differential Data Clock Output. LVDS clock at the DAC sample rate.
27	DVDD33	Digital Input and Output Pad Ring Supply Voltage (3.3 V).
29, 30	DCIP, DCIN	Differential Data Clock Input. LVDS clock aligned with input data.
37, 38	D0P, D0N	LVDS Data Input (LSB).
39 to 46	NC	No Connection. Leave these pins floating.
49	SDO	Serial Port Data Output.
50	SDIO	Serial Port Data Input (4-Wire Mode). Bidirectional serial data line (3-wire mode).
51	SCLK	Serial Port Clock Input.
52	CSB	Serial Port Chip Select (Active Low).
53	RESET	Chip Reset (Active High).
54	FS ADJ	Full-Scale Current Output Adjust.
55	REFIO	Analog Reference Input/Output (1.2 V Nominal).
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Common.
59	IOUT2P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
60	IOUT2N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
62, 63	AUX2P, AUX2N	Differential Auxiliary DAC current output (Channel 2).
65, 66	AUX1N, AUX1P	Differential Auxiliary DAC current output (Channel 1).
68	IOUT1N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
69	IOUT1P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.

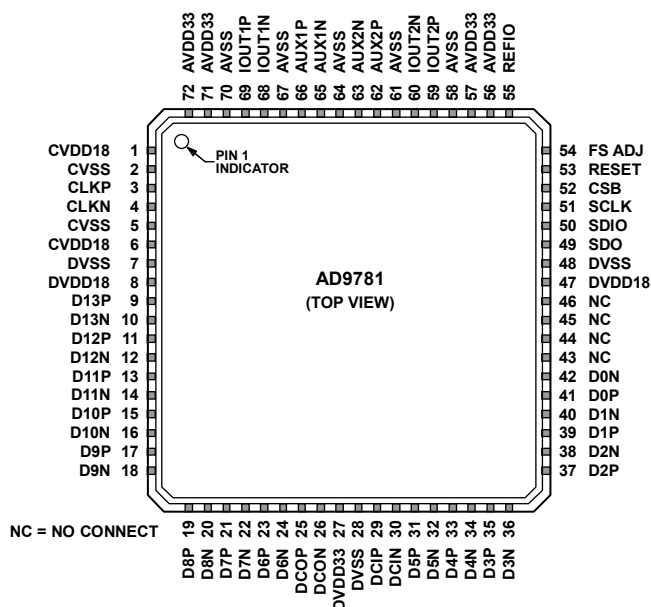


Figure 3. AD9781 Pin Configuration

Table 7. AD9781 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Return.
3, 4	CLKP, CLKN	Differential DAC Sampling Clock Input.
7, 28, 48	DVSS	Digital Common.
8, 47	DVDD18	Digital Supply Voltage (1.8 V).
9, 10	D13P, D13N	LVDS Data Input (MSB).
11 to 24, 31 to 40	D12P, D12N to D1P, D1N	LVDS Data Inputs.
25, 26	DCOP, DCON	Differential Data Clock Output. LVDS clock at the DAC sample rate.
27	DVDD33	Digital Input and Output pad ring supply voltage (3.3 V).
29, 30	DCIP, DCIN	Differential Data Clock Input. LVDS clock aligned with input data.
41, 42	D0P, D0N	LVDS Data Input (LSB).
43 to 46	NC	No connection. Leave these pins floating.
49	SDO	Serial Port Data Output.
50	SDIO	Serial Port Data Input (4-Wire Mode). Bidirectional serial data line (3-wire mode).
51	SCLK	Serial Port Clock Input.
52	CSB	Serial Port Chip Select (Active Low).
53	RESET	Chip Reset (Active High).
54	FS ADJ	Full-Scale Current Output Adjust.
55	REFIO	Analog Reference Input/Output (1.2 V nominal).
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Common.
59	IOUT2P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
60	IOUT2N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
62, 63	AUX2P, AUX2N	Differential Auxiliary DAC current output (Channel 2).
65, 66	AUX1N, AUX1P	Differential Auxiliary DAC current output (Channel 1).
68	IOUT1N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
69	IOUT1P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.

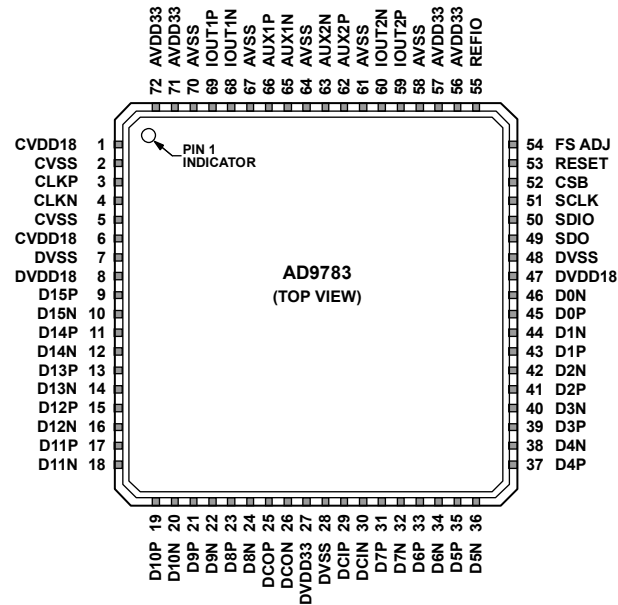


Figure 4. AD9783 Pin Configuration

Table 8. AD9783 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Return.
3, 4	CLKP, CLKN	Differential DAC Sampling Clock Input.
7, 28, 48	DVSS	Digital Common.
8, 47	DVDD18	Digital Supply Voltage (1.8 V).
9, 10	D15P, D15N	LVDS Data Input (MSB).
11 to 24, 31 to 44	D14P, D14N to D1P, D1N	LVDS Data Inputs.
25, 26	DCOP, DCON	Differential Data Clock Output. LVDS clock at the DAC sample rate.
27	DVDD33	Digital Input and Output Pad Ring Supply Voltage (3.3 V).
29, 30	DCIP, DCIN	Differential Data Clock Input. LVDS clock aligned with input data.
45, 46	D0P, D0N	LVDS Data Input (LSB).
49	SDO	Serial Port Data Output.
50	SDIO	Serial Port Data Input (4-Wire Mode). Bidirectional serial data line (3-wire mode).
51	SCLK	Serial Port Clock Input.
52	CSB	Serial Port Chip Select (Active Low).
53	RESET	Chip RESET (active High).
54	FS ADJ	Full-Scale Current Output Adjust.
55	REFIO	Analog Reference Input/Output (1.2 V nominal).
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Common.
59	IOUT2P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
60	IOUT2N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
62, 63	AUX2P, AUX2N	Differential Auxiliary DAC Current Output (Channel 2).
65, 66	AUX1N, AUX1P	Differential Auxiliary DAC Current Output (Channel 1).
68	IOUT1N	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
69	IOUT1P	DAC Current Output. Full-scale current is sourced when all data bits are 1s.

# TYPICAL PERFORMANCE CHARACTERISTICS

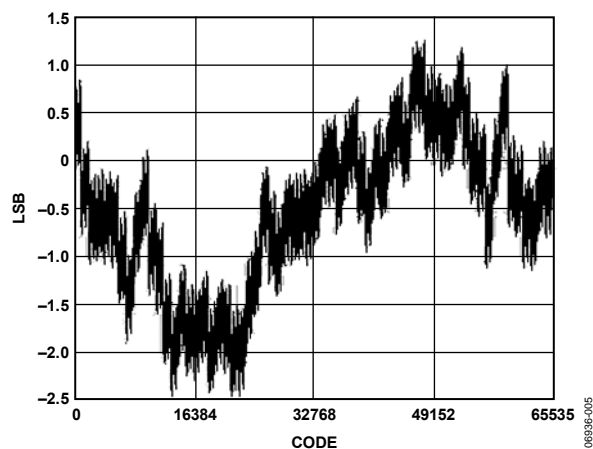


Figure 5. AD9783 INL 85°C

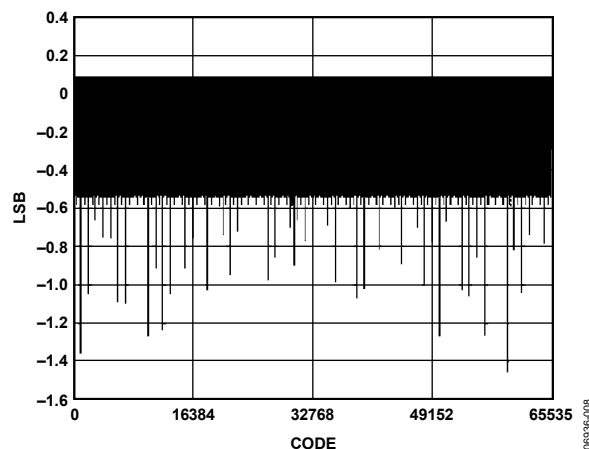


Figure 8. AD9783 DNL 85°C

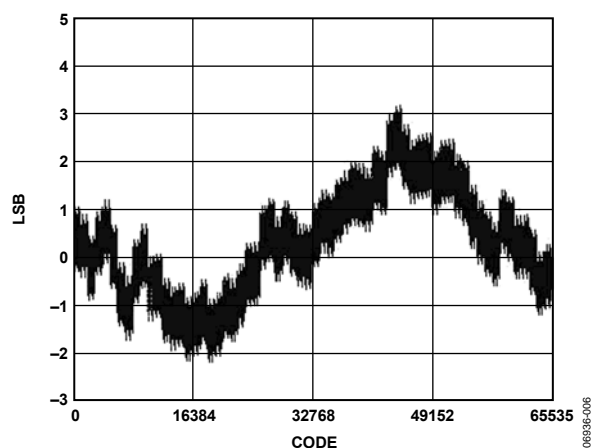


Figure 6. AD9783 INL 25°C

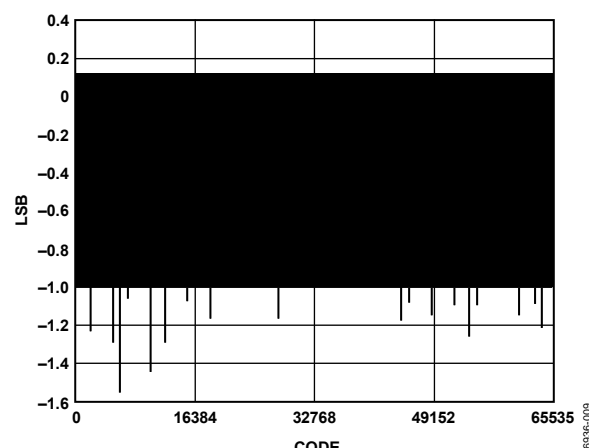


Figure 9. AD9783 DNL 25°C

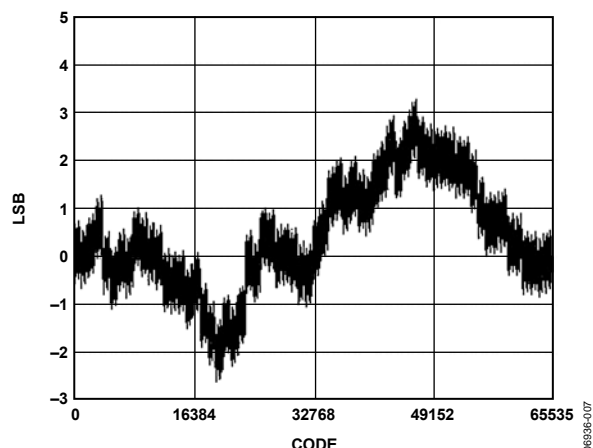


Figure 7. AD9783 INL -40°C

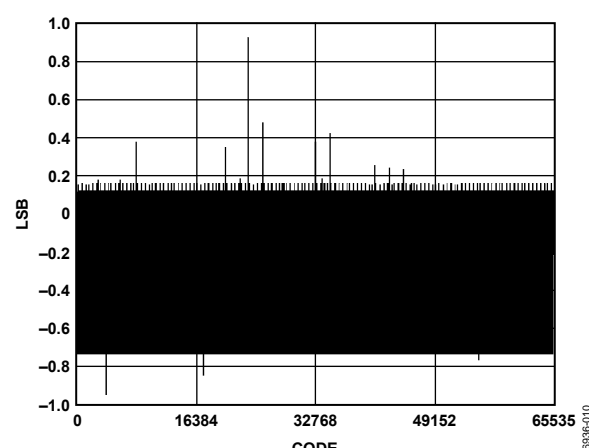


Figure 10. AD9783 DNL -40°C

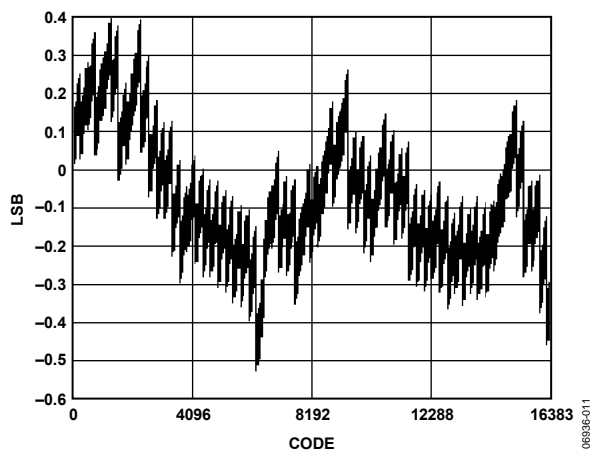


Figure 11. AD9781 INL 85°C

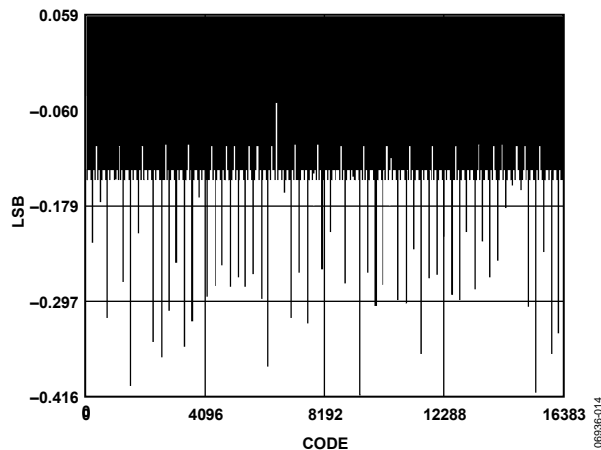
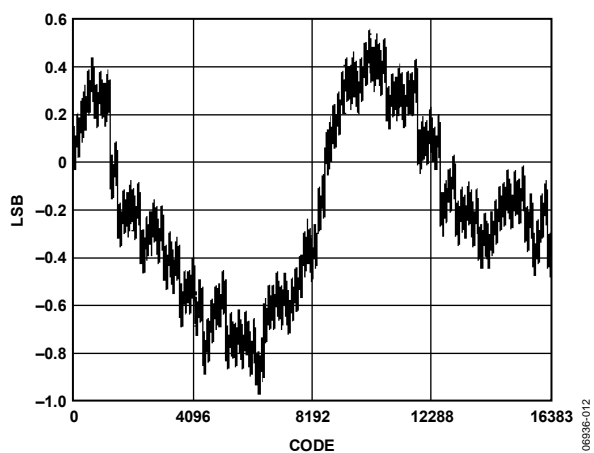
Figure 14. AD9781 DNL 20mA  $F_S$  85°C

Figure 12. AD9781 INL -40°C

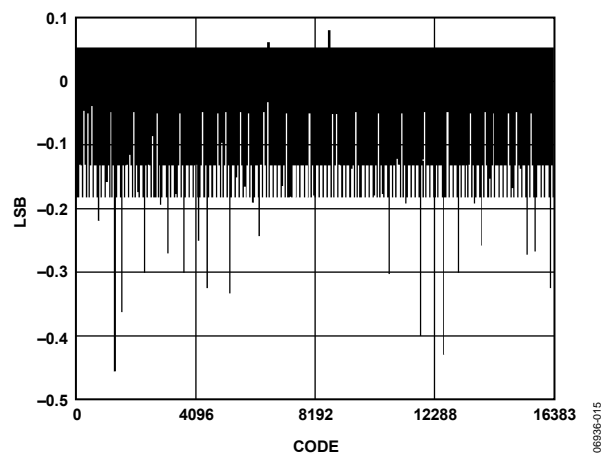


Figure 15. AD9781 DNL -40°C

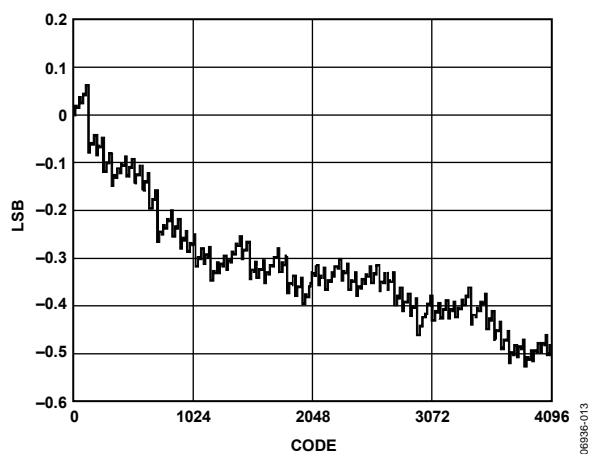


Figure 13. AD9780 INL -40°C

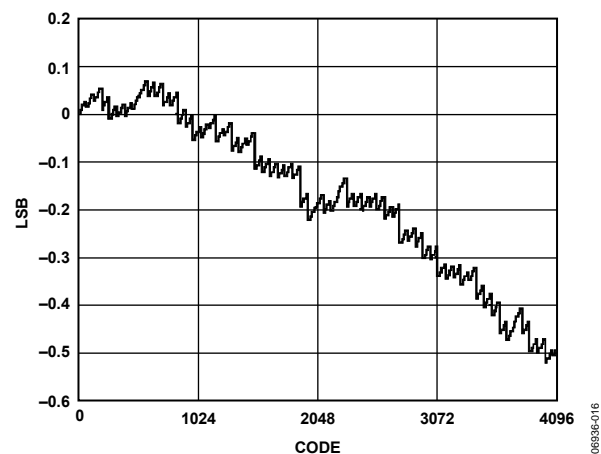


Figure 16. AD9780 INL 85°C

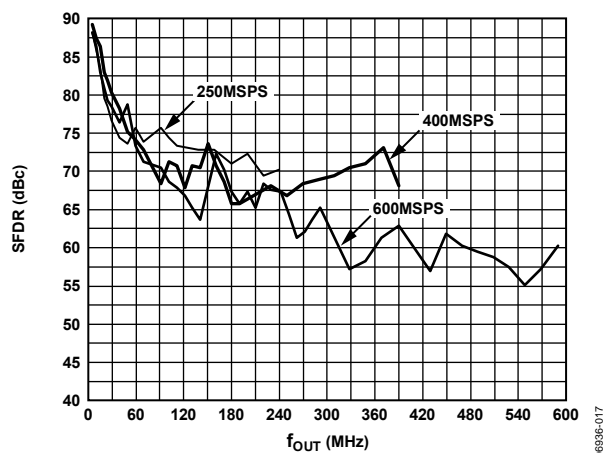


Figure 17. AD9783 SFDR vs.  $f_{OUT}$  Over  $F_{DAC}$  in Baseband and Mix Modes

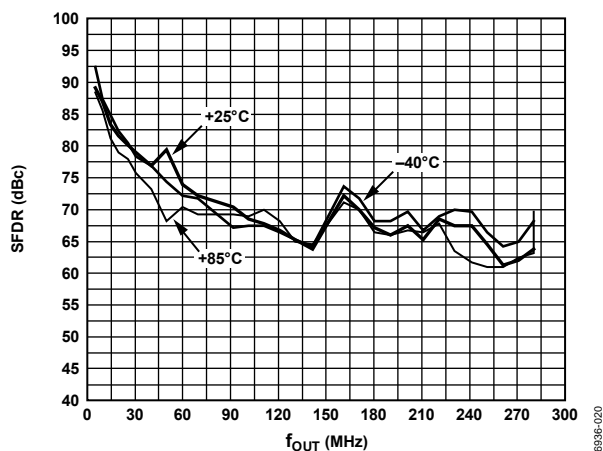


Figure 20. AD9783 SFDR vs.  $f_{OUT}$  Over Temperature, 600 MSPS

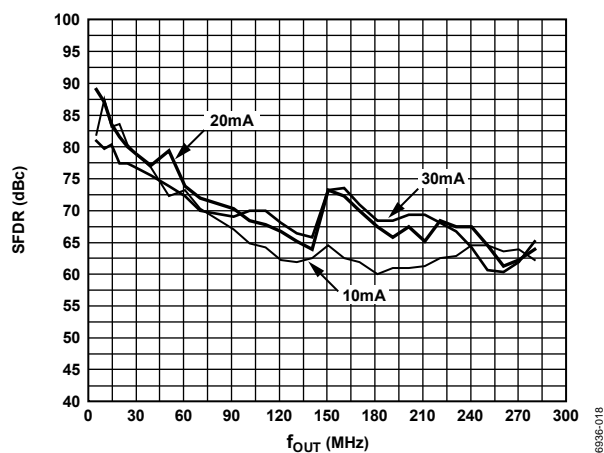


Figure 18. AD9783 SFDR vs.  $f_{OUT}$  Over Analog Output, 25°C, 600 MSPS

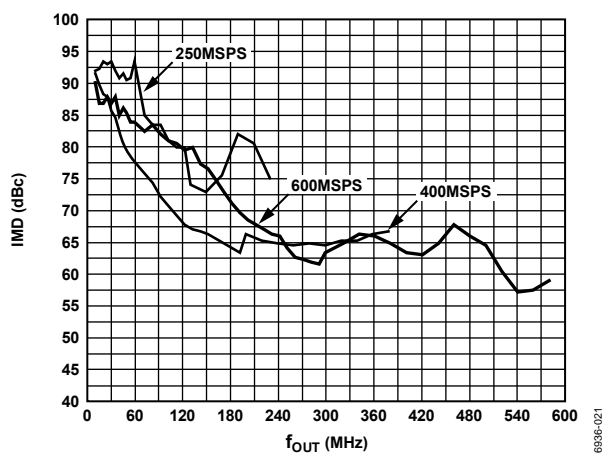


Figure 21. AD9783 IMD vs.  $f_{OUT}$  Over  $F_{DAC}$  in Baseband and Mix Modes

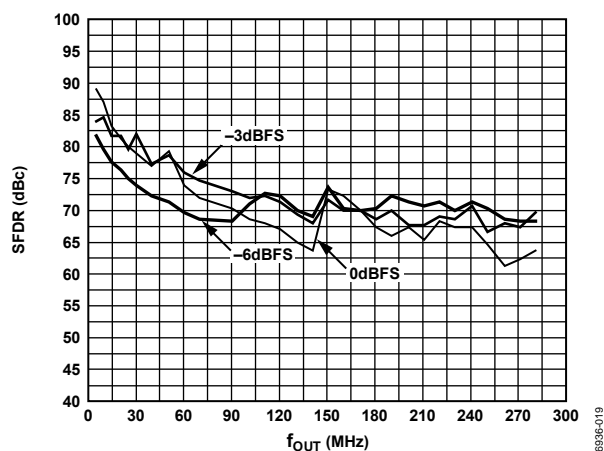


Figure 19. AD9783 SFDR vs.  $f_{OUT}$  Over Digital Input Level, 25°C, 600 MSPS

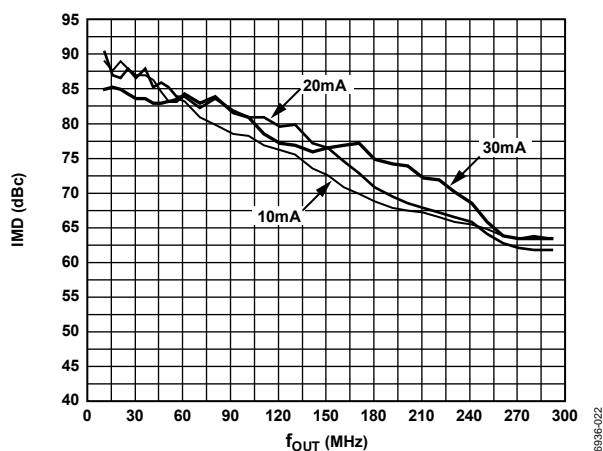


Figure 22. AD9783 IMD vs.  $f_{OUT}$  Over Analog Output, 25°C, 600 MSPS

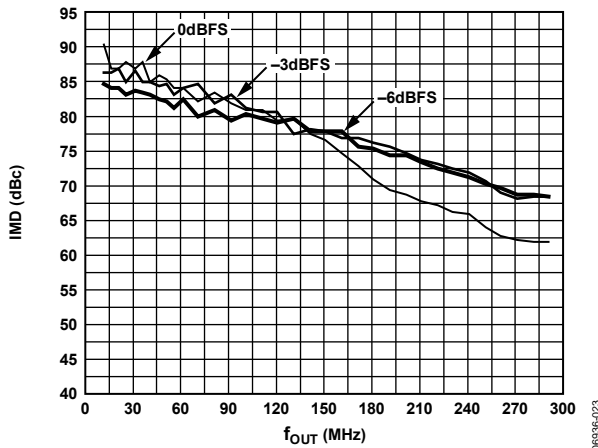


Figure 23. AD9783 IMD vs.  $f_{OUT}$  Over Digital Input Level, 25C, 600MSPS

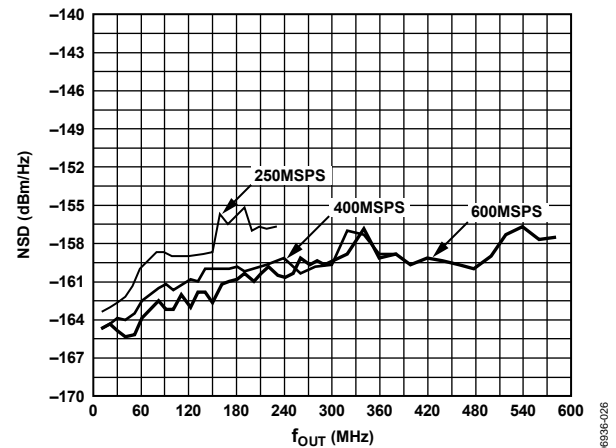


Figure 26. AD9783 8-Tone NSD vs.  $f_{OUT}$  Over  $F_{DAC}$  Baseband and Mix Modes

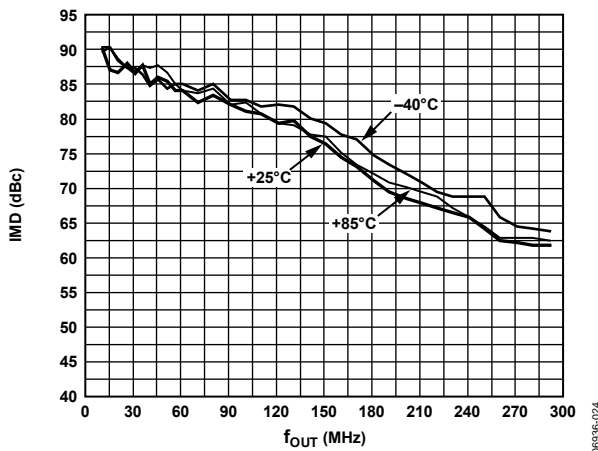


Figure 24. AD9783 IMD vs.  $f_{OUT}$  Over Temperature, 600MSPS

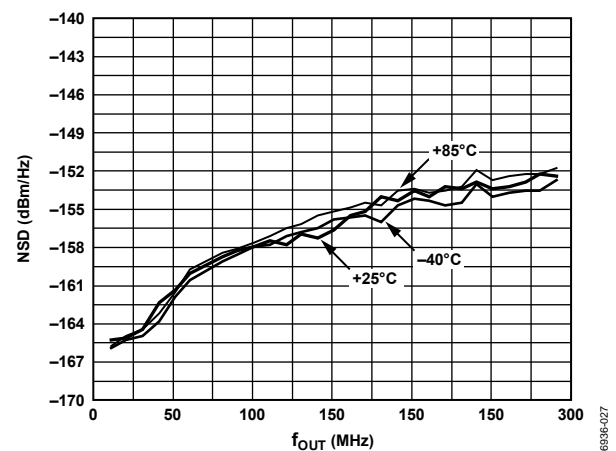


Figure 27. AD9783 1-Tone NSD vs.  $f_{OUT}$  Over Temperature, 600MSPS

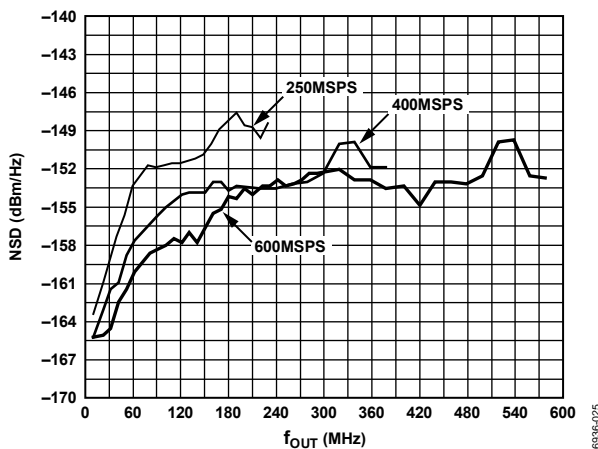


Figure 25. AD9783 1-Tone NSD vs.  $f_{OUT}$  Over  $F_{DAC}$  Baseband and Mix Modes

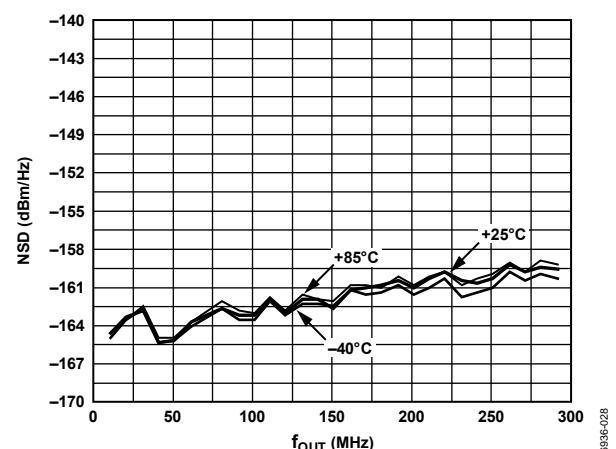


Figure 28. AD9783 8-Tone NSD vs.  $f_{OUT}$  Over Temperature, 600MSPS

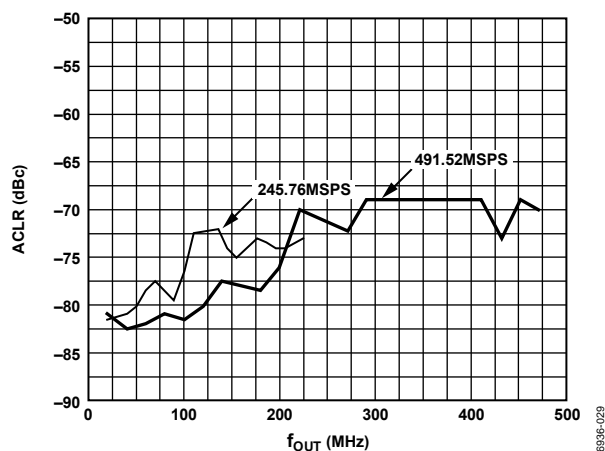


Figure 29. AD9783 ACLR For First Adjacent Band 1-Carrier WCDMA Baseband and Mix Modes

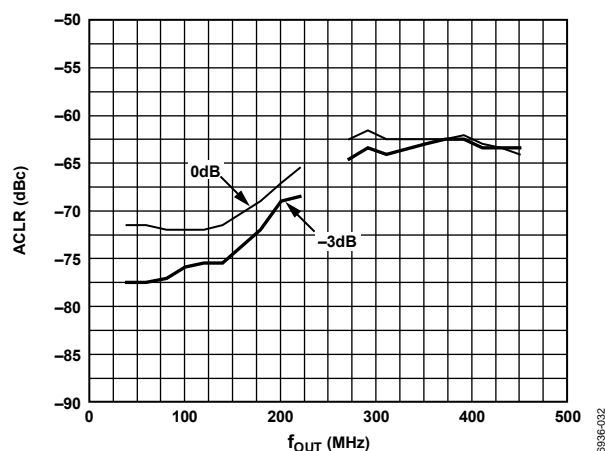


Figure 32. AD9783 ACLR for First Adjacent Channel 2-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

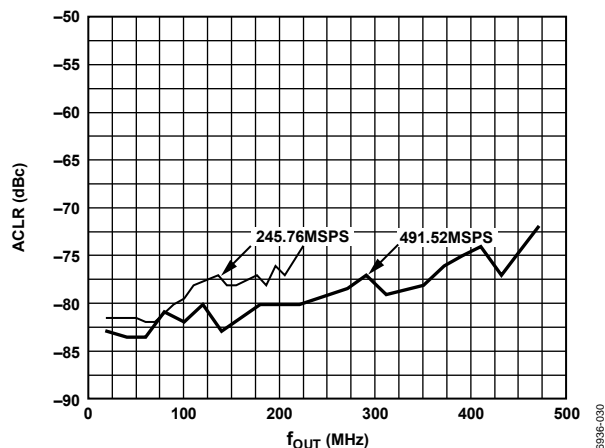


Figure 30. AD9783 ACLR For Second Adjacent Band 1-Carrier WCDMA Baseband and Mix Modes

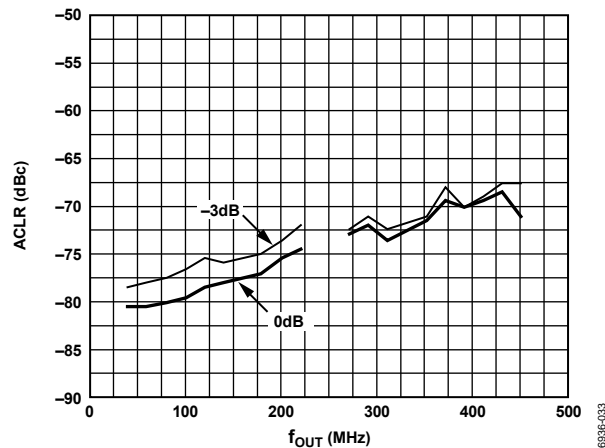


Figure 33. AD9783 ACLR for Second Adjacent Channel 2-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

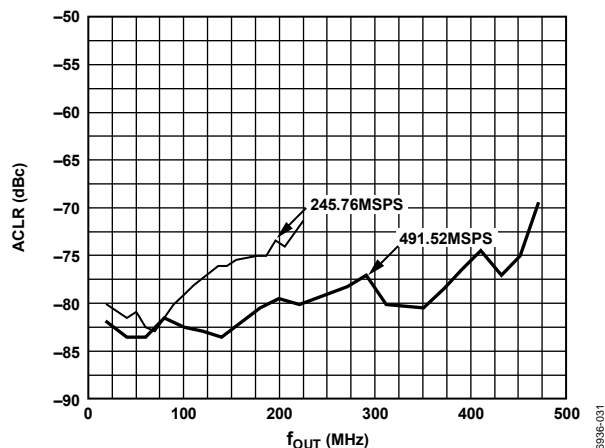


Figure 31. AD9783 ACLR For Third Adjacent Band 1-Carrier WCDMA Baseband and Mix Modes

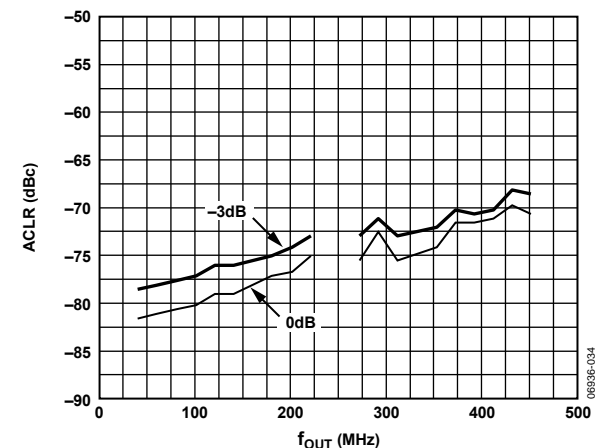


Figure 34. AD9783 ACLR for Third Adjacent Channel 2-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

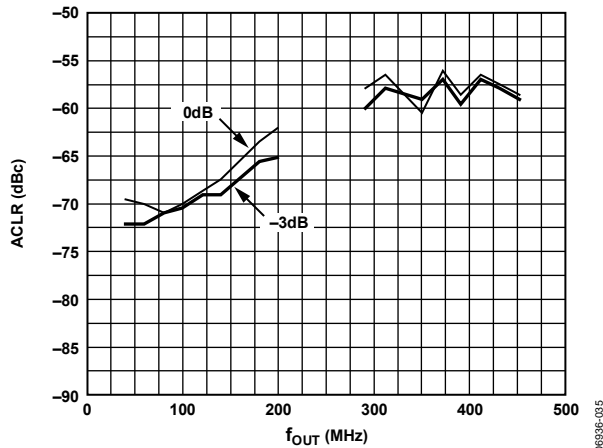


Figure 35. AD9783 ACLR for First Adjacent Channel 4-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

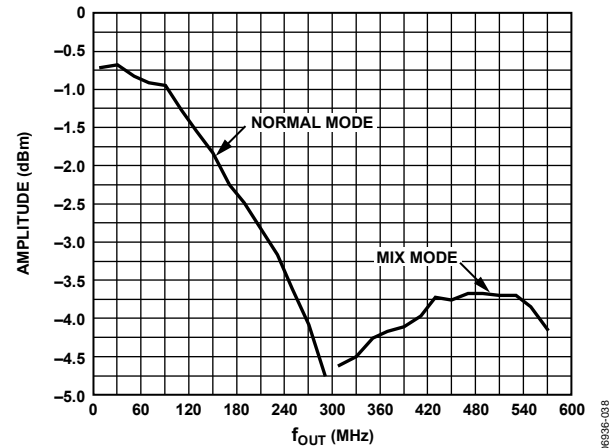


Figure 38. Nominal Power In The Fundamental, 20 mA  $F_s$  600 MSPS

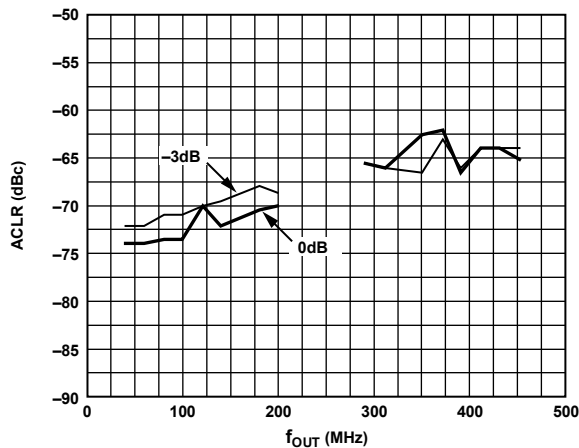


Figure 36. AD9783 ACLR for Second Adjacent Channel 4-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

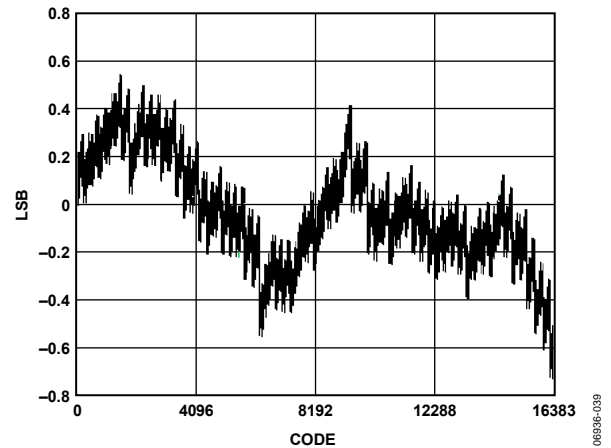


Figure 39. AD9781 INL 20 mA  $F_s$

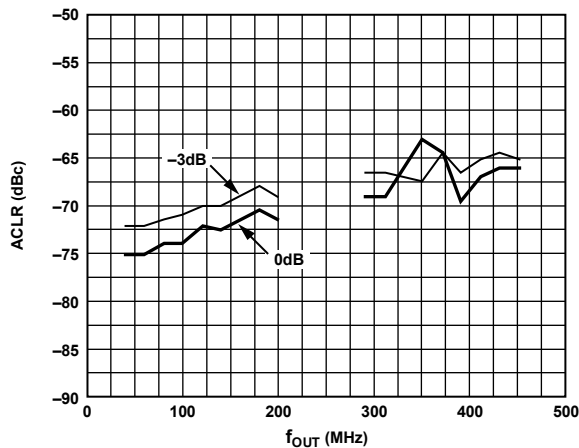


Figure 37. AD9783 ACLR for Third Adjacent Channel 4-Carrier WCDMA Over Digital Input Level Baseband and Mix Modes, 491.52 MSPS

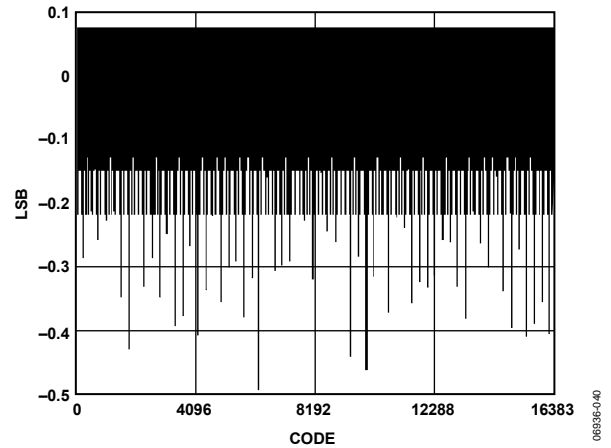


Figure 40. AD9781 DNL 20 mA  $F_s$

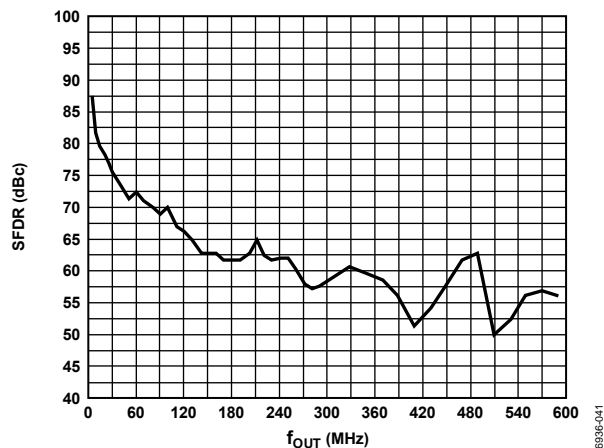


Figure 41. AD9781 SFDR vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

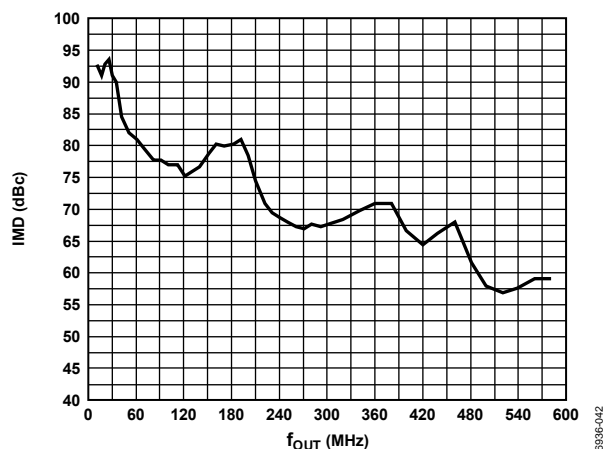


Figure 42. AD9781 IMD vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

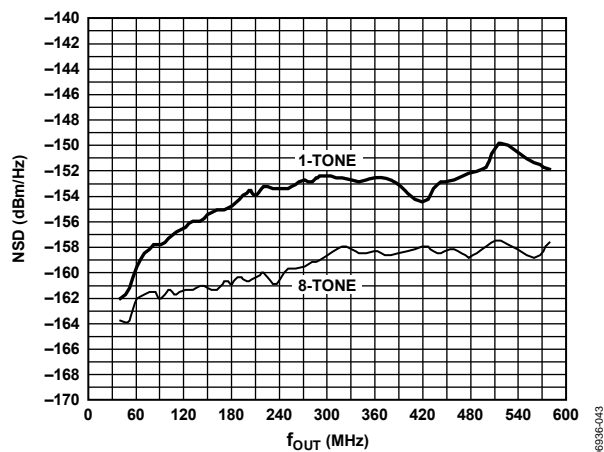


Figure 43. AD9781 1-Tone, 8-Tone NSD vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

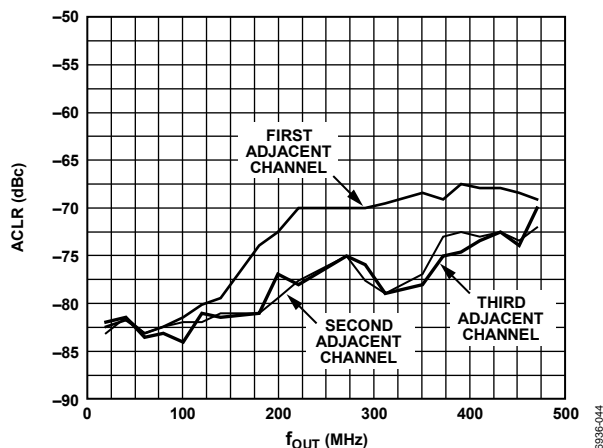


Figure 44. AD9781 ACLR for 1-Carrier WCDMA Baseband and Mix Modes, 491.52 MSPS

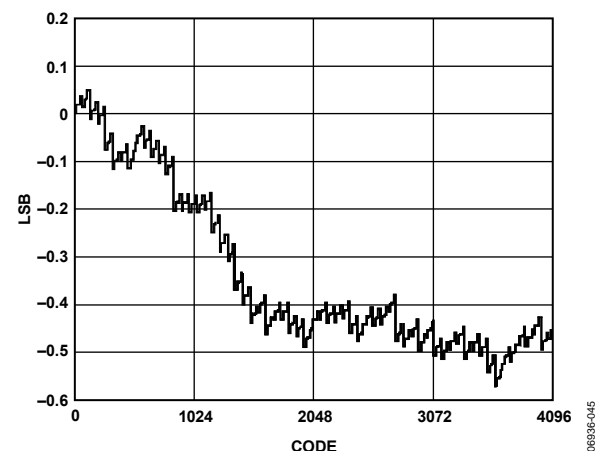


Figure 45. AD9780 INL 20 mA  $F_S$

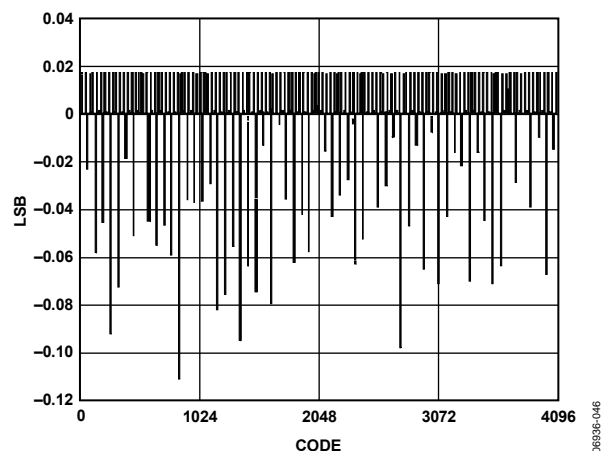


Figure 46. AD9780 DNL, 20 mA  $F_S$

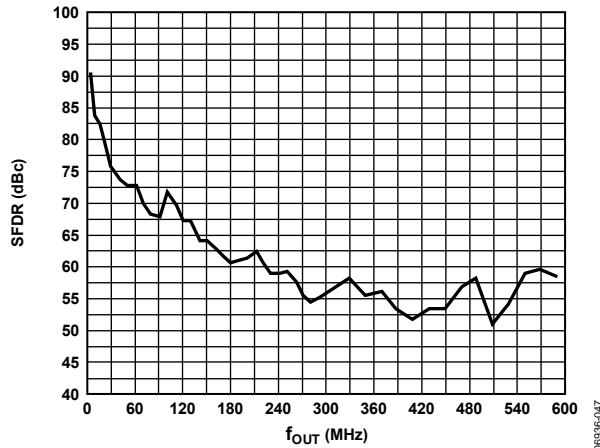


Figure 47. AD9780 SFDR vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

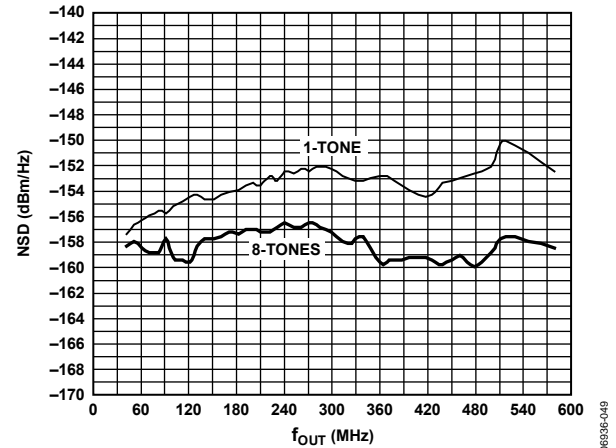


Figure 49. AD9780 1-Tone, 8-Tone NSD vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

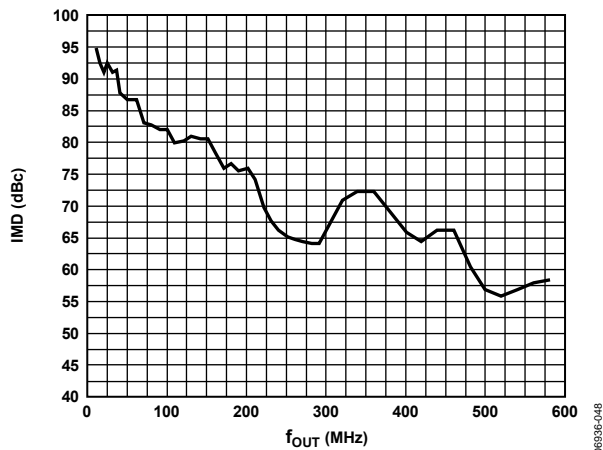


Figure 48. AD9780 IMD vs.  $f_{OUT}$  in Baseband and Mix Modes, 600 MSPS

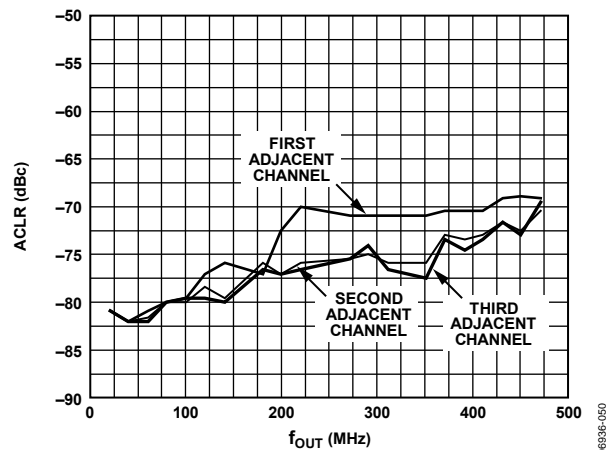


Figure 50. AD9780 ACLR For 1-Carrier WCDMA Baseband and Mix Modes, 491.52 MSPS

## TERMINOLOGY

### Linearity Error (Integral Nonlinearity or INL)

Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

### Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

### Monotonicity

A DAC is monotonic if the output either increases or remains constant as the digital input increases.

### Offset Error

The deviation of the output current from the ideal of zero is called offset error. For  $I_{OUTA}$ , 0 mA output is expected when the inputs are all 0s. For  $I_{OUTB}$ , 0 mA output is expected when all inputs are set to 1.

### Gain Error

The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

### Output Compliance Range

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

### Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either  $T_{MIN}$  or  $T_{MAX}$ . For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

### Power Supply Rejection

The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

### Settling Time

The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

### Spurious Free Dynamic Range (SFDR)

The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

### Adjacent Channel Leakage Ratio (ACLR)

The ratio in dBc between the measured power within a channel relative to its adjacent channel.

### Complex Image Rejection

In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

## THEORY OF OPERATION

The AD9780/AD9781/AD9783 combine many features to make them very attractive for wired and wireless communications systems. The dual DAC architecture facilitates easy interface to common quadrature modulators when designing single sideband transmitters. In addition, the speed and performance of the devices allows wider bandwidths and more carriers to be synthesized than in previously available products.

All features and options are software programmable through the SPI port.

### SERIAL PERIPHERAL INTERFACE

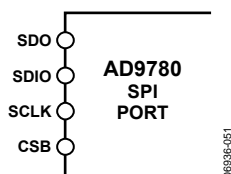


Figure 51. SPI Port

The serial peripheral interface (SPI) port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The port is compatible with most synchronous transfer formats including both the Motorola SPI® and Intel® SSR protocols.

The interface allows read and write access to all registers that configure the AD9780/AD9781/AD9783. Single or multiple byte transfers are supported as well as MSB-first or LSB-first transfer formats. Serial data input/output can be accomplished through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

The serial port configuration is controlled by Register 0x00, Bits<7:6>. It is important to note that any change made to the serial port configuration occurs immediately upon writing to the last bit of this byte. Therefore, it is possible with a multibyte transfer to write to this register and change the configuration in the middle of a communication cycle. Care must be taken to compensate for the new configuration within the remaining bytes of the current communication cycle.

Use of a single-byte transfer when changing the serial port configuration is recommended to prevent unexpected device behavior.

### GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to any communication cycle with the AD9780/AD9781/AD9783: Phase 1 and Phase 2. Phase 1 is the instruction cycle, which writes an instruction byte into the device. This byte provides the serial port controller with information regarding Phase 2 of the communication cycle: the data transfer cycle.

The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and a reference register address for the first byte of the data transfer. A logic high on the CSB pin followed by a logic low resets the SPI port to its initial state and defines the start of the instruction cycle. From this point, the next eight rising SCLK edges define the eight bits of the instruction byte for the current communication cycle.

The remaining SCLK edges are for Phase 2 of the communication cycle, which is the data transfer between the serial port controller and the system controller. Phase 2 can be a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using multibyte transfers is usually preferred although single-byte data transfers are useful to reduce CPU overhead or when only a single register access is required.

All serial port data is transferred to and from the device in synchronization with the SCLK pin. Input data is always latched on the rising edge of SCLK whereas output data is always valid after the falling edge of SCLK. Register contents change immediately upon writing to the last bit of each transfer byte.

Anytime synchronization is lost, the device has the ability to asynchronously terminate an I/O operation whenever the CSB pin is taken to logic high. Any unwritten register content data is lost if the I/O operation is aborted. Taking CSB low then resets the serial port controller and restarts the communication cycle.

### INSTRUCTION BYTE

The instruction byte contains the information shown in Table 9.

Table 9.

MSB						LSB	
B7	B6	B5	B4	B3	B2	B1	B0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit 7, R/W, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

Bits<6:5>, N1 and N0, determine the number of bytes to be transferred during the data transfer cycle. The bits decode as shown in Table 10.

Table 10. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Bits<4:0>, A4, A3, A2, A1, and A0, determine which register is accessed during the data transfer of the communications cycle. For multibyte transfers, this address is a starting or ending address depending on the current data transfer mode. For MSB-first format, the specified address is an ending address or the most significant address in the current cycle. Remaining register addresses for multiple byte data transfers are generated internally by the serial port controller by decrementing from the specified address. For LSB-first format, the specified address is a beginning address or the least significant address in the current cycle. Remaining register addresses for multiple byte data transfers are generated internally by the serial port controller by incrementing from the specified address.

### MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register 0x00, Bit 6. The default is Logic 0, which is MSB-first format.

When using MSB-first format (LSBFIRST = 0), the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes are loaded into sequentially lower address locations. In MSB-first mode, the serial port internal address generator decrements for each byte of the multibyte data transfer.

When using LSB-first format (LSBFIRST = 1), the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes are loaded into sequentially higher address locations. In LSB-first mode, the serial port internal address generator increments for each byte of the multibyte data transfer.

Use of a single-byte transfer when changing the serial port data format is recommended to prevent unexpected device behavior.

### SERIAL INTERFACE PORT PIN DESCRIPTIONS

#### Chip Select Bar (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communication lines. CSB must stay low during the entire communication cycle. Incomplete data transfers are aborted anytime the CSB pin goes high. SDO and SDIO pins go to a high impedance state when this input is high.

#### Serial Clock (SCLK)

The serial clock pin is used to synchronize data to and from the device and to run the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

#### Serial Port Data I/O (SDIO)

Data is always written into the device on this pin. However, SDIO can also function as a bidirectional data output line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

#### Serial Port Data Output (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. The configuration of this pin is controlled by Register 0x00, Bit 7. If this bit is set to a Logic 1, the SDO pin does not output data and is set to a high impedance state.

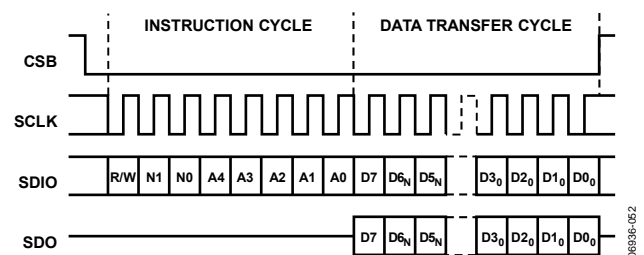


Figure 52. Serial Register Interface, MSB First

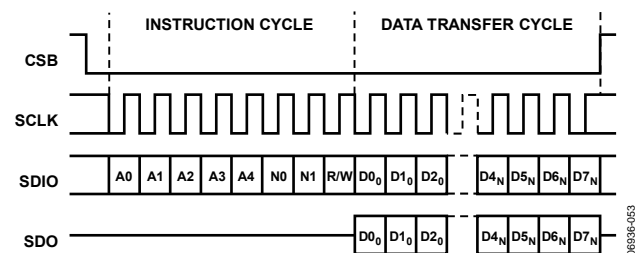


Figure 53. Serial Register Interface Timing LSB First

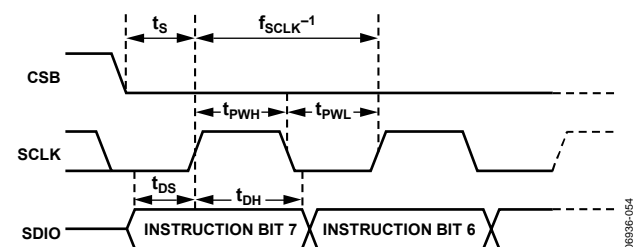


Figure 54. Timing Diagram for SPI Write Register

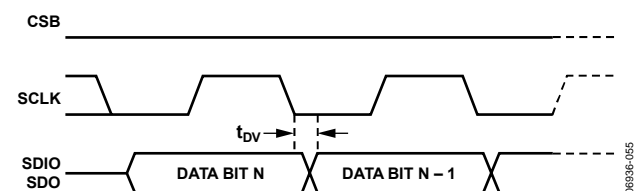


Figure 55. Timing Diagram for SPI Read Register

## SPI REGISTER MAP

Table 11.

Register Name	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00	SDIO_DIR	LSBFIRST	RESET					
Data Control	0x02	0x00	DATA	ONEPORT		INVDCO				
Power Down	0x03	0x00	PD_DCO	PD_INPT	PD_AUX2	PD_AUX1	PD_BIAS	PD_CLK	PD_DAC2	PD_DAC1
Setup and Hold	0x04	0x00	SET<3:0>				HLD<3:0>			
Timing Adjust	0x05	0x00				SAMP_DLY<4:0>				
Seek	0x06	0x00						LVDS Low	LVDS High	SEEK
Mix Mode	0x0A	0x00					DAC1MIX<1:0>		DAC2MIX<1:0>	
DAC1 FSC	0x0B	0xF9	DAC1FSC<7:0>							
DAC1 FSC MSBs	0x0C	0x01							DAC1FSC<9:8>	
AUXDAC1	0x0D	0x00	AUXDAC1<7:0>							
AUXDAC1 MSB	0x0E	0x00	AUX1SGN	AUX1DIR					AUXDAC1<9:8>	
DAC2 FSC	0x0F	0xF9	DAC2FSC<7:0>							
DAC2 FSC MSBs	0x10	0x01							DAC2FSC<9:8>	
AUXDAC2	0x11	0x00	AUXDAC2<7:0>							
AUXDAC2 MSB	0x12	0x00	AUX2SGN	AUX2DIR					AUXDAC2<9:8>	
BIST Control	0x1A	0x00	BISTEN	BISTRD	BISTCLR					
BIST Result 1 Low	0x1B	0x00	BISTRES1<7:0>							
BIST Result 1 High	0x1C	0x00	BISTRES1<15:8>							
BIST Result 2 Low	0x1D	0x00	BISTRES2<7:0>							
BIST Result 2 High	0x1E	0x00	BISTRES2<15:8>							
Hardware Version	0x1F	N/A	VERSION<3:0>				DEVICE<2:0>			

## SPI REGISTER DESCRIPTIONS

Reading these registers returns previously written values for all defined register bits, unless otherwise noted.

Table 12.

Register	Address	Bit	Name	Function
SPI Control	0x00	7	SDIO_DIR	0, Operate SPI in 4-wire mode. The SDI pin operates as an input only pin. 1, Operate SPI in 3-wire mode. The SDI pin operates as a bidirectional data line.
		6	LSBFIRST	0, MSB first per SPI Standard 1, LSB first per SPI Standard Note: Only Change LSB/MSB order in single-byte instructions to avoid erratic behavior due to bit order errors.
		5	RESET	0, Execute Software reset of SPI and controllers, reload default register values except register 0x00. 1, Set Software reset, write 0 on the next (or any following) cycle to release the reset.
Data Control	0x02	7	DATA	0, DAC input data is two's compliment binary format. 1, DAC input data is unsigned binary format.
		4	INVDCO	1, Inverts the Data Clock Output. Used for adjusting timing of input data.
Power Down	0x03	7	PD_DCO	1, Power down Data Clock Output driver circuit.
		6	PD_INPT	1, Power Down Input..
		5	PD_AUX2	1, Power down AUX2 DAC
		4	PD_AUX1	1, Power down AUX1 DAC.
		3	PD_BIAS	1, Power down Voltage Reference Bias circuit.
		2	PD_CLK	1, Power down DAC Clock input circuit..
		1	PD_DAC2	1, Power down DAC2
		0	PD_DAC1	1, Power down DAC1.
Setup and Hold	0x04	7:4	SET<3:0>	4-bit value used to determine input data setup timing.
		3:0	HLD<3:0>	4-bit value used to determine input data hold timing.
Timing Adjust	0x05	4:0	SAMP_DLY<4:0>	5-bit values used to optimally position input data relative to internal sampling clock.
Seek	0x06	2	LVDS High	One of the LVDS inputs is above the input voltage limits of the IEEE reduced link specification
		1	LVDS Low	One of the LVDS inputs is below the input voltage limits of the IEEE reduced link specification
		0	SEEK	Indicator bit used with LVDS_SET and LVDS_HLD to determine input data timing margin.
Mix Mode	0x0A	3:2	DAC1MIX<1:0>	00 – Selects Normal Mode, DAC2. 01 – Selects Return to Zero mode, DAC2. 10 – Selects Return to Zero mode, DAC2. 11 – Selects Mix mode, DAC2.
		1:0	DAC2MIX<1:0>	00 – Selects Normal Mode, DAC1. 01 – Selects Return to Zero mode, DAC1. 10 – Selects Return to Zero mode, DAC1. 11 – Selects Mix mode, DAC1.
DAC1 FSC	0x0B 0x0C		DAC1FSC<9:0>	DAC1 Full-Scale 10 bit adjustment word. 0x3FF, Sets DAC Full-Scale Output Current to the maximum value of 31.68mA . 0x200, Sets DAC Full-Scale Output Current to the nominal value of 20.0mA. 0x000, Sets DAC Full-Scale Output Current to the minimum value of 8.64mA.

Register	Address	Bit	Name	Function
AUXDAC1	0x0D 0x0E	7:0	AUXDAC1<9:0>	AUXDAC1 output current adjustment word.
		1:0	AUXDAC1<9:8>	0x3FF, Sets AUXDAC1 Output Current to 2.0 mA. 0x200, Sets AUXDAC1 Output Current to 1.0 mA. 0x000, Sets AUXDAC1 Output Current to 0.0 mA.
		7	AUX1SGN	0, AUX1_P output pin is active. 1, AUX1_N output pin is active.
		6	AUX1DIR	0, Configures AUX1 DAC output to source current. 1, Configures AUX1 DAC output to sink current.
DAC2 FSC	0x0F 0x10		DAC2FSC<9:0>	DAC2 Full-Scale 10 bit adjustment word. 0x3FF, Sets DAC Full-Scale Output Current to the maximum value of 31.68mA . 0x200, Sets DAC Full-Scale Output Current to the nominal value of 20.0mA. 0x000, Sets DAC Full-Scale Output Current to the minimum value of 8.64mA.
AUXDAC2	0x11 0x12	7:0	AUXDAC2<9:0>	AUX DAC2 output current adjustment word.
		7	AUX2SGN	0, AUX2_P output pin is active. 1, AUX2_N output pin is active.
		6	AUX2DIR	0, Configures AUX2 DAC output to source current. 1, Configures AUX1 DAC output to sink current.
		1:0		0x3FF, Sets AUXDAC2 Output Current to 2.0 mA. 0x200, Sets AUXDAC2 Output Current to 1.0 mA. 0x000, Sets AUXDAC2 Output Current to 0.0 mA.
BIST Control	0x1A	7	BISTEN	1, Enables and starts Built In Self Test.
		6	BISTRD	1, Transfers BIST result registers to SPI for readback.
		5	BISTCLR	1, Reset BIST logic and clear BIST result registers.
BIST Result1	0x1B 0x1C	7:0 7:0	BISTRES1<15:0>	Sixteen bit result generated by BIST 1.
BIST Result2	0x1D 0x1E	7:0 7:0	BISTRES2<15:0>	Sixteen bit result generated by BIST 2.
Hardware Version	0x1F	7:4	VERSION<3:0>	Read only register. Indicates the version of the chip.
		3:0	DEVICE<3:0>	Read only register. Indicates the device type.

## SPI PORT, RESET, AND PIN MODE

In general, when the AD9780/AD9781/AD9783 are powered up, an active high pulse applied to the RESET pin should follow. This insures the default state of all control register bits. In addition, once the RESET pin goes low, the SPI port can be activated, so, CSB should be held high.

For applications without a controller, the AD9780/AD9781/AD9783 also supports pin mode operation, which allows some functional options to be pin, selected without the use of the SPI port. Pin mode is enabled anytime the RESET pin is held high. In pin mode, the four SPI port pins take on secondary functions as shown in Table 13.

**Table 13. SPI Pin Functions (Pin Mode)**

Pin Name	Pin Mode Function
SDIO	DATA (Register 0x02, Bit 7), bit value (1/0) equals pin state (high/low)
CSB	Enable Mix Mode, if CSB is high, Register 0x0A is set to 0x05 putting both DAC1 and DAC2 into mix mode
SDO	Enable full power-down, if SDO is high, Register 0x03 is set to 0xFF

## PARALLEL DATA PORT INTERFACE

The parallel port data interface consists of 18 differential LVDS signals, DCO, DCI, and the sixteen DATA lines (DATA[15:0]), as shown in Figure 56. DCO is the output clock generated by the AD9780/AD9781/AD9783 that is used to clock out the data from the digital data engine. The DATA lines transmit the multiplexed I and Q data words for the I and Q DACs respectively. The DCI provides timing information about the parallel data as well as signals the I/Q status of the data.

As shown in Figure 56, the incoming LVDS data is latched by an internally generated clock referred to as the data sampling signal (DSS). DSS is a delayed version of the main DAC clock signal CLKP/CLKN. Optimal positioning of the rising and falling edges of DSS with respect to the incoming DATA signals results in the most robust transmission of the DAC data. Positioning the edges of DSS with respect to the DATA signals is achieved by selecting the value of a programmable delay element, SMP. A procedure for determining optimal value of SMP is given in the Optimizing the Parallel Port Timing section.

In addition to properly positioning the DSS edges, maximizing the opening of the eye in the DCLK\_IN and DATA signals improves the reliability of the data port interface. The two sources of degradation that reduce the eye in the DCLK\_IN and DATA signals are the jitter on these signals and the skew between them. Therefore, it is recommended that the DCLK\_IN be generated in the same manner as the DATA signals with the same output driver and data line routing. In

other words, it should be implemented as a seventeenth DATA line with an alternating (010101...) bit sequence.

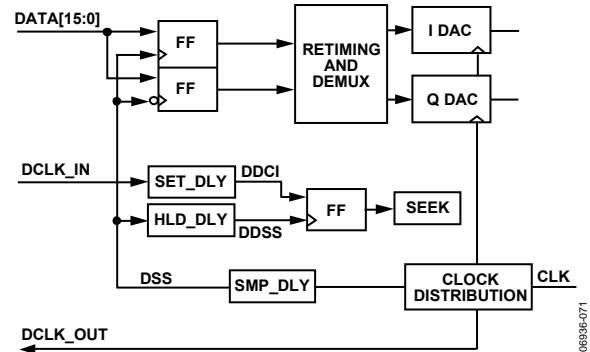


Figure 56. AD9783 Digital Data Port

## OPTIMIZING THE PARALLEL PORT TIMING

Before outlining the procedure for determining the delay for SMP (that is, the positioning of DSS with respect to the DATA signals), it is worthwhile describing the simplified block diagram of the digital data port. As can be seen in Figure 56, the DATA signals are latched-in on the rising and falling edges of DSS. From there, the data is demultiplexed and retimed before being sent to the DACs.

The DCLK\_IN signal provides timing information about the parallel data as well as indicating the destination (that is, I DAC or Q DAC) of the data. A delayed version of DCI is generated by a delay element, SET and is referred to as DDCL. DDCL is sampled by a delayed version of the DSS signal, labeled as DDSS in Figure 56. DDSS is simply DSS delayed by a period of time, HLD. The pair of delays, SET and HLD allow accurate timing information to be extracted from DCLK\_IN. Increasing the delay of the HLD block, results in DCLK\_IN being sampled later in its cycle. Increasing the delay of the SET block, results in DCLK\_IN being sampled earlier in its cycle. The result of this sampling is stored and can be queried by reading the SEEK bit. Since DSS and DCLK\_IN are the same frequency, the SEEK bit should be a constant value. By varying the SET and HLD delay blocks and seeing the effect on the SEEK bit, the setup and hold timing of DSS with respect to DCLK\_IN (and hence, DATA) can be measured.

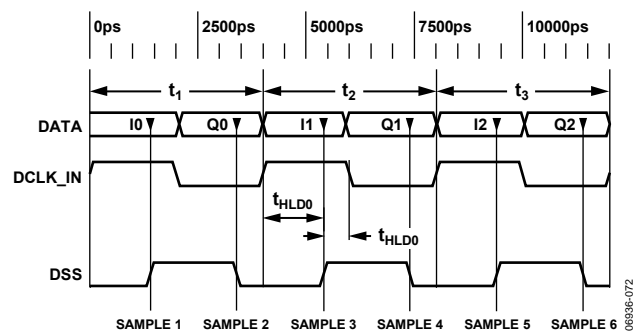


Figure 57. Digital Data Timing

The incremental units of SET, HLD, and SMP are in units of real time, not fractions of a clock cycle. The nominal step size

for SET and HLD is 80 psec. The nominal step size for SMP is 160 ps. Note that the value of SMP refers to Register 5, Bits[4:0], SET refers to Register 4, Bits[7:4], and HLD refers to Register 4, Bits[3:0].

Use the following steps to ensure the AD9780/AD9781/AD9783 is configured for a valid sampling time of the DATA signals. Generally speaking, the procedure begins by finding the point in its cycle that DCI is sampled by the rising edge of DSS. Based on this information, a value of SMP is programmed to establish a new and improved sampling point. This new sampling point is then double checked to make sure it is optimally set.

1. Set the values of SMP, SET, and HLD to zero. Read and record the value of the SEEK bit.
2. With SMP and SET set to 0, increment the HLD until the SEEK bit toggles and record the HLD value. This measures the hold time as shown in figure 2.
3. With SMP and HLD set to 0, increment the SET until the SEEK bit toggles and record the SET value. This measures the set-up time as shown in Figure 57.
4. Using the values of SMP, HLD, and SET, the value of SMP can now be determined.
5. If SEEK = 1, and HLD and SET are within 2 counts of each other, then the sampling edge is well positioned and it is unnecessary to increase the SMP delay. Also, if SEEK = 1 and HLD and SET are both greater than 12, then there is a sufficient timing margin and it is unnecessary to increase the SMP delay.
6. If SEEK = 1, and SET is more than two counts higher than HLD, then your timing resembles that shown in Figure 58. Program the value of SMP to be

$$SMP = \frac{PER - 40 \times (SET - HLD)}{160}$$

Where PER is the period of the DAC Clock (CLK) period in picoseconds. This moves the sampling edge of DSS from the position marked Orig, to the position marked New in the figure.

7. If SEEK = 1, and HLD is more than two counts higher than SET, then your timing resembles that shown in Figure 59. Program the value of SMP to be

$$SMP = \frac{(HLD - SET)}{4}$$

This moves the sampling edge of DSS from the position marked Orig to the position marked New in the figure.

8. If SEEK = 0, then your timing resembles that shown in Figure 60. Program the value of SMP to be

$$SMP = \frac{PER + 80 \times (HLD - SET)}{320}$$

Where PER is the period of the DAC Clock (CLK) period in picoseconds. This moves the sampling edge of DSS from

the position marked Orig, to the position marked New in the figure.

9. After programming the calculated value of SMP, verification that the sampling edge occurs in the middle of the valid data window can be done as follows. Set both SET and HLD to zero. Increment SET until the SEEK bit goes low and record that value. Reset SET to zero. Increment HLD until SEEK goes low and record that value. The recorded values of SET and HLD should be within two unit delays of each other if SMP was set correctly.

It should be noted that the values of SET and HLD should both be a minimum of 4. If either value is lower than this, then you should check for excessive jitter on your DCLK\_IN line, and that the frequency of DCLK\_IN does not exceed the datasheet maximum.

Another consideration in the timing of the digital data port is the propagation delay variation from DATACLK\_OUT to DATACLK\_IN. If this varies significantly (more than 25% of SET or HLD) over time due to temperature changes or other effects, then repeat this timing calibration procedure accordingly.

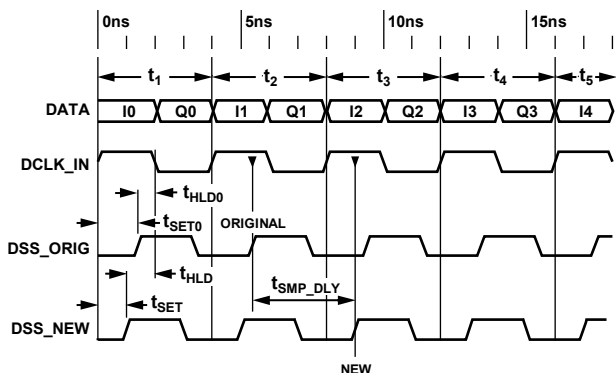


Figure 58. Digital Data Timing Calibration

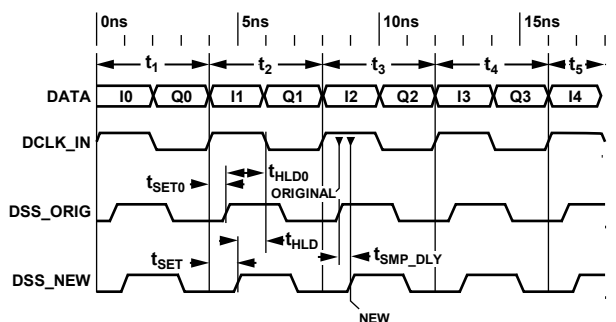


Figure 59. Digital Data Timing Calibration

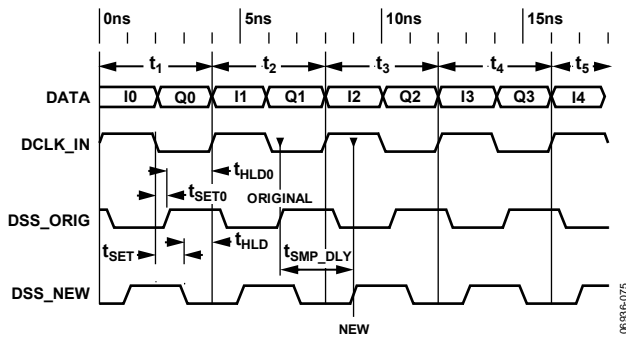


Figure 60. Digital Data Timing Calibration

## DRIVING THE CLK INPUT

The CLK input requires a low jitter differential drive signal. It is a PMOS input differential pair powered from the 1.8 V supply, therefore, it is important to maintain the specified 400 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p about the 400 mV common-mode voltage. While these input levels are not directly LVDS-compatible, CLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 61.

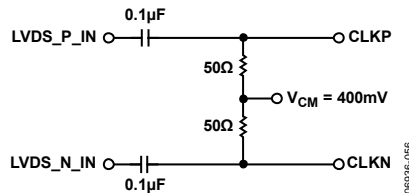


Figure 61. LVDS DACCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to CLK, as shown in Figure 61. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS to LVDS translator, then ac-coupled, as described in this section. Alternatively, it can be transformer-coupled and clamped, as shown in Figure 62.

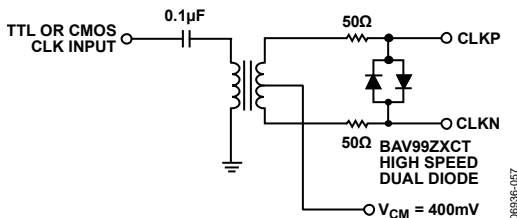


Figure 62. TTL or CMOS DACCLK Drive Circuit

A simple bias network for generating VCM is shown in Figure 63. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade the DAC's performance.

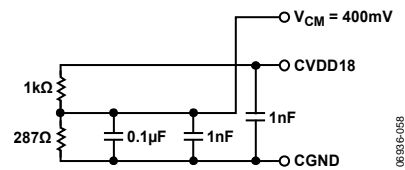


Figure 63. DACCLK VCM Generator Circuit

## FULL-SCALE CURRENT GENERATION

### Internal Reference

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to FSADJ (Pin54). A simplified block diagram of the reference circuitry is shown in Figure 64. The recommended value for the external resistor is 10 kΩ, which sets up an  $I_{\text{REFERENCE}}$  in the resistor of 120 µA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Internal current mirrors provide a current-gain scaling, where I DAC or Q DAC gain is a 10-bit word in the SPI port register. The default value for the DAC gain registers gives a full-scale current output ( $I_{\text{FS}}$ ) of approximately 20 mA, where  $I_{\text{FS}}$  is equal to:

$$I_{\text{FS}} = (86.6 + (0.220 \times \text{DAC gain})) \times 1000 / R$$

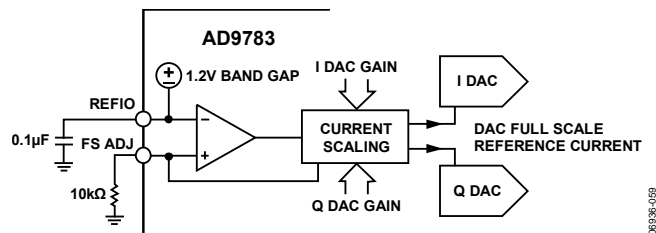


Figure 64. Reference Circuitry

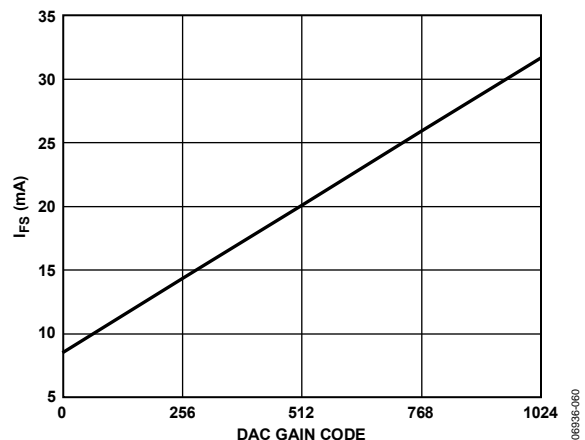


Figure 65.  $I_{\text{FS}}$  vs. DAC Gain Code

## DAC TRANSFER FUNCTION

Each DAC output of the AD9780/AD9781/AD9783 drives two complementary current outputs,  $I_{OUTP}$  and  $I_{OUTN}$ .  $I_{OUTP}$  provides a near  $I_{FS}$  when all bits are high. For example,

$$DAC\ CODE = 2^N - 1,$$

where:

$N = 12\text{-}/14\text{-}/16\text{-bits}$  for AD9780/AD9781/AD9783 respectively), while  $I_{OUTN}$  provides no current.

The current output appearing at  $I_{OUTP}$  and  $I_{OUTN}$  is a function of both the input code and  $I_{FS}$  and can be expressed as

$$I_{OUTP} = (DAC\ DATA / 2^N) \times I_{FS} \quad (1)$$

$$I_{OUTN} = ((2^N - 1) - DAC\ DATA) / 2^N \times I_{FS} \quad (2)$$

where  $DAC\ DATA = 0$  to  $2^N - 1$  (decimal representation).

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required,  $I_{OUTP}$  and  $I_{OUTN}$  should be connected to matching resistive loads ( $R_{LOAD}$ ) that are tied to analog common ( $AVSS$ ). The single-ended voltage output appearing at the  $I_{OUTP}$  and  $I_{OUTN}$  pins is

$$V_{OUTP} = I_{OUTP} \times R_{LOAD} \quad (3)$$

$$V_{OUTN} = I_{OUTN} \times R_{LOAD} \quad (4)$$

Note that to achieve the maximum output compliance of 1 V at the nominal 20 mA output current,  $R_{LOAD}$  must be set to 50  $\Omega$ . Also note that the full-scale value of  $V_{OUTP}$  and  $V_{OUTN}$  should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

There are two distinct advantages to operating the AD9780/AD9781/AD9783 differentially. First, differential operation helps cancel common-mode error sources associated with  $I_{OUTP}$  and  $I_{OUTN}$ , such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent output voltage ( $V_{DIFF}$ ) is twice the value of the single-ended voltage output ( $V_{OUTP}$  or  $V_{OUTN}$ ), providing  $2\times$  signal power to the load.

$$V_{DIFF} = (I_{OUTP} - I_{OUTN}) \times R_{LOAD} \quad (5)$$

## ANALOG MODES OF OPERATION

The AD9780/AD9781/AD9783 utilizes a proprietary quad-switch architecture that lowers the distortion of the DAC by eliminating a code dependent glitch that occurs with conventional dual-switch architectures. This architecture eliminates the code dependent glitches, but creates a constant glitch at a rate of  $2 \times f_{DAC}$ . For communications systems and other applications requiring good frequency domain performance from the DAC, this is seldom problematic.

The quad-switch architecture also supports two additional modes of operation; mix mode and return-to-zero mode. The waveforms of these two modes are shown in Figure 66. In the mix mode, the output is inverted every other half clock cycle. This effectively chops the DAC output at the sample rate. This chopping has the effect of frequency shifting the sinc roll-off

from dc to  $f_{DAC}$ . Additionally, there is a second subtle effect on the output spectrum. The shifted spectrum is also shaped by a second Sinc function with a first null at  $2 \times f_{DAC}$ . The reason for this shaping is that the data is not continuously varying at twice the clock rate, but is simply repeated.

In the return-to-zero mode, the output is set to mid-scale every other half clock cycle. The output is similar to the DAC output in normal mode except that the output pulses are half the width and half the area. Because the output pulses have half the width, the sinc function is scaled in frequency by two and has a first null at  $2 \times f_{DAC}$ . Because the area of the pulses is half that of the pulses in normal mode, the output power is half the normal mode output power.

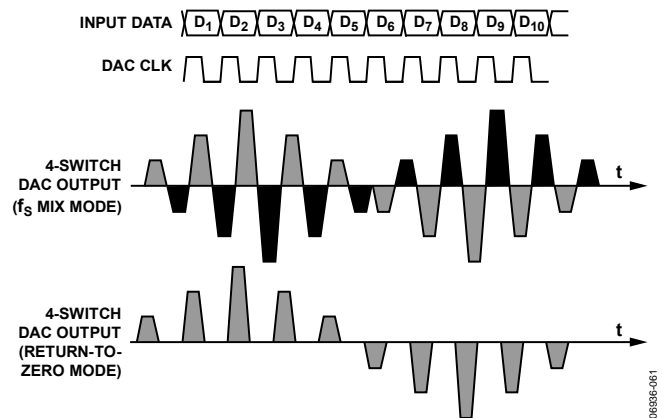


Figure 66. Mix Mode and RZ DAC Waveforms

The functions that shape the output spectrums for the three modes of operation; normal mode, mix mode and return-to-zero mode, are shown in Figure 67. Switching between the analog modes reshapes the sinc roll off inherent at the DAC output. This ability to change modes in the AD9780/AD9781/AD9783 make the parts suitable for direct IF applications. The user can place a carrier anywhere in the first three nyquist zones depending on the operating mode selected. The performance and maximum amplitude in all three nyquist zones is impacted by this sinc roll off depending on where the carrier is placed, as shown in Figure 67.

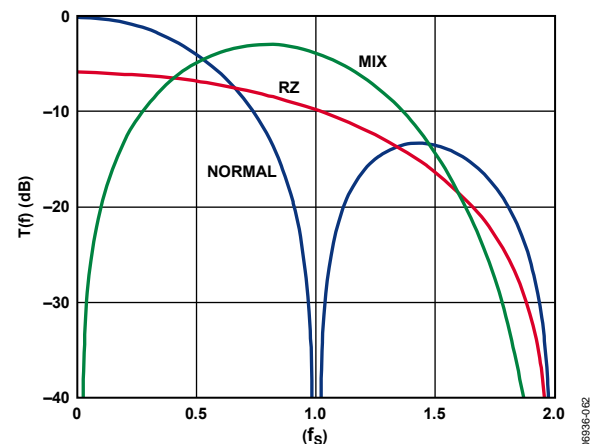


Figure 67. Transfer Function for Each Analog Operating Mode

### Auxiliary DACs

Two auxiliary DACs are provided on the AD9780/AD9781/AD9783. A functional diagram is shown in Figure 68. The auxiliary DACs are current output devices with two output pins, AUXP and AUXN. The active pin can be programmed to either source or sink current. When either sinking or sourcing, the full-scale current magnitude is 2 mA. The available compliance range at the auxiliary DAC outputs depends on whether the output is configured to a sink or source current. When sourcing current, the compliance voltage is 0 V to 1.6 V but when sinking current the output compliance voltage is reduced to 0.8 V to 1.6 V. Either output can be used, but only one output of the AUX DAC (P or N) is active at any time. The inactive pin is always in a high impedance state ( $>100\text{ k}\Omega$ ).

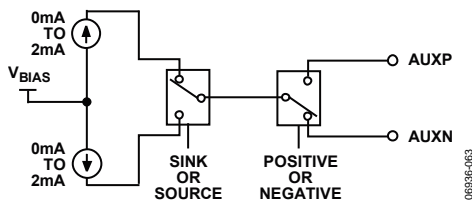


Figure 68. Auxiliary DAC Functional Diagram

In a single sideband transmitter application, the combination of the input referred dc offset voltage of the quadrature modulator and the DAC output offset voltage can result in local oscillator (LO) feedthrough at the modulator output, which degrades system performance. The auxiliary DACs can be used to remove the dc offset and the resulting LO feedthrough. The circuit configuration for using the auxiliary DACs for performing dc offset correction depends on the details of the DAC and modulator interface. An example of a dc-coupled configuration with low-pass filtering is outlined in the Figure 69.

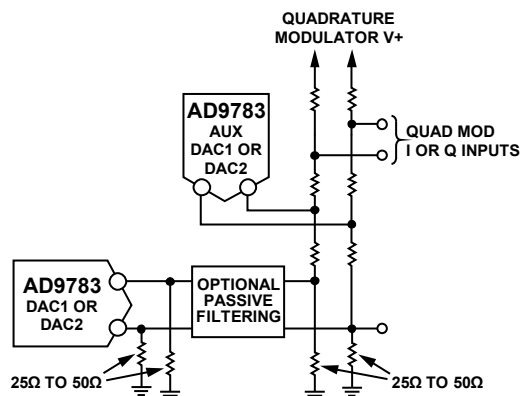


Figure 69. DAC DC Coupled to Quadrature Modulator with Passive DC Shift

### POWER DISSIPATION

Figure 70 through Figure 75 show the power dissipation of the part in single DAC and dual DAC modes.

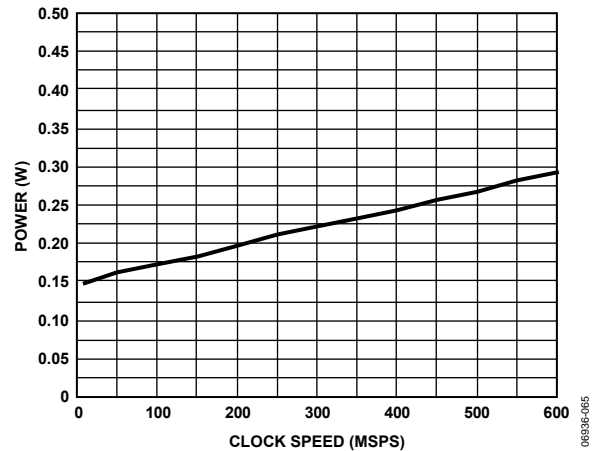


Figure 70. Power Dissipation, I Data Only, Single DAC Mode

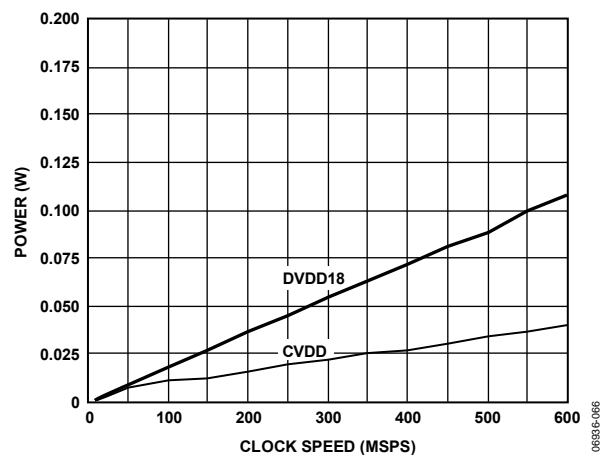


Figure 71. Power Dissipation, Digital 1.8 V Supply, Clock 1.8 V Supply I Data Only

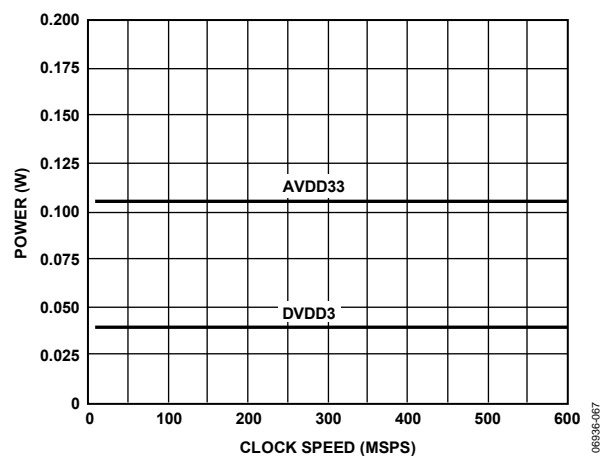


Figure 72. Power Dissipation, Digital 3.3 V Supply, Analog 3.3 V Supply, I Data Only

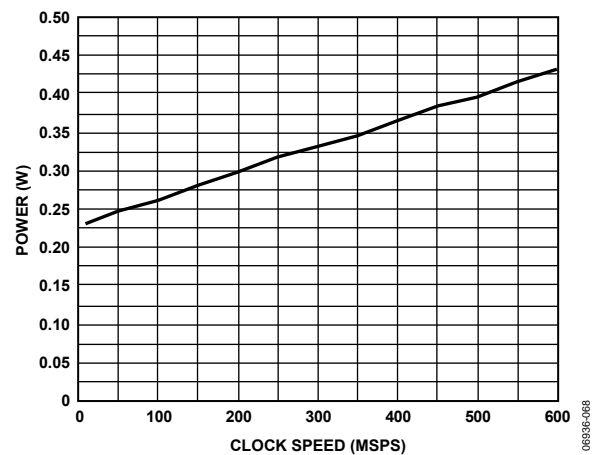


Figure 73. . Power Dissipation, I and Q Data Only, Dual DAC Mode

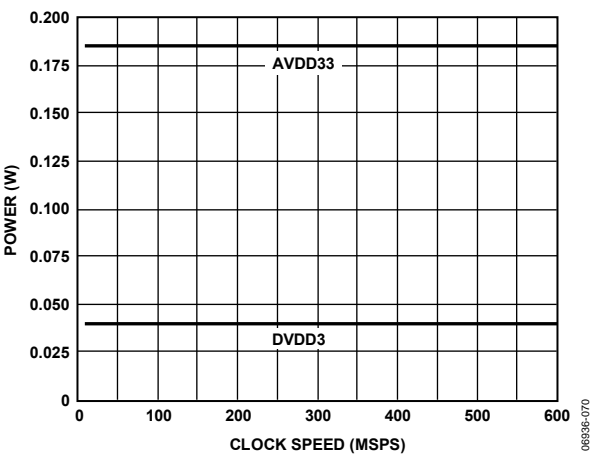


Figure 75. Power Dissipation, Digital 3.3 V Supply, Analog 3.3 V Supply I and Q Data Dual DAC Mode

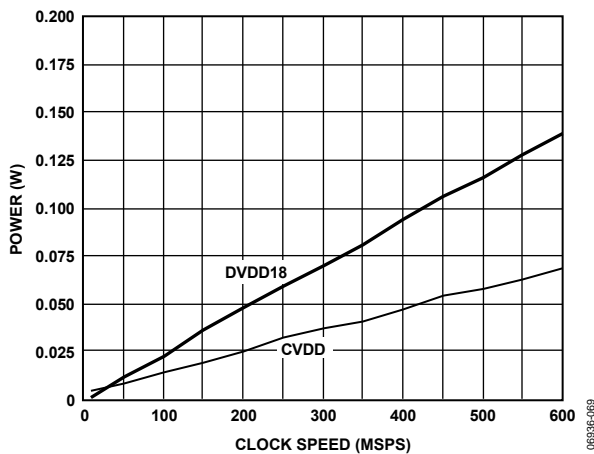
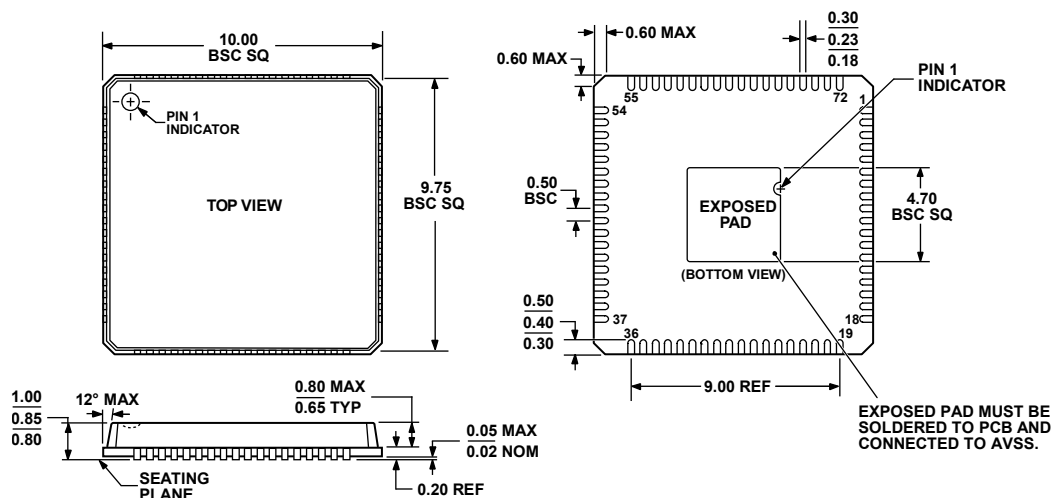


Figure 74. Power Dissipation, Digital 1.8 V Supply, Clock 1.8 V Supply I and Q Data Dual DAC Mode

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-3

Figure 76. 72-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]

10 mm × 10 mm, Very Thin Quad

(CP-72-1)

Dimensions shown in millimeters

042407-0

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9780BCPZ <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9780BCPZRL7 <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9781BCPZ <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9781BCPZRL7 <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9783BCPZ <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9783BCPZRL7 <sup>1</sup>	−40°C to +85°C	72-Lead LFCSP	CP-72-1
AD9780-EB <sup>1</sup>		Evaluation Board	
AD9781-EB <sup>1</sup>		Evaluation Board	
AD9783-EB <sup>1</sup>		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

## **NOTES**

## NOTES

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