Low Noise, Precision, 16 V, CMOS, Rail-to-Rail Operational Amplifiers

AD8663

FEATURES

- Low offset voltage: 175 µV maximum @ V_S = 5 V
- Low supply current: 275 µA maximum per amplifier
- Single-supply operation: 5 V to 16 V
- Low noise: 23 nV/√Hz
- Wide bandwidth: 520 kHz
- Unity-gain stable
- Small package options
  - 3 mm × 3 mm 8-lead LFCSP
  - 8-lead narrow SOIC

APPLICATIONS

- Sensors
- Medical equipment
- Consumer audio
- Photodiode amplification
- ADC drivers

PIN CONFIGURATIONS

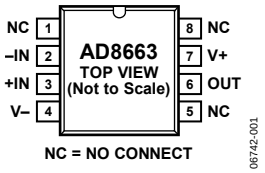

Figure 1. AD8663, 8-Lead SOIC (R-8)

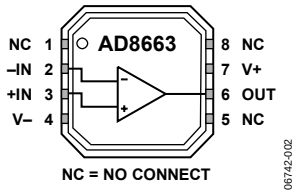

Figure 2. AD8663, 8-Lead LFCSP (CP-8-2)

GENERAL DESCRIPTION

The AD8663 is a rail-to-rail output, single-supply amplifier that uses the Analog Devices, Inc., patented DigiTrim® trimming technique to achieve low offset voltage. The AD8663 features an extended operating range, with supply voltages up to 16 V. It also features low input bias current, wide signal bandwidth, and low input voltage and current noise.

The combination of low offset, very low input bias current, and a wide supply range makes these amplifiers useful in a wide variety of applications usually associated with higher priced JFET amplifiers. Systems using high impedance sensors, such as photodiodes, benefit from the combination of low input bias current, low noise, low offset, and wide bandwidth. The wide operating voltage range meets the demands of high performance ADCs and DACs. Audio applications and medical monitoring equipment can take advantage of the high input impedance, low voltage and current noise, and wide bandwidth.

The single AD8663 is available in a narrow 8-lead SOIC package and a very thin, dual lead, 8-lead LFCSP. The AD8663 SOIC package is specified over the extended industrial temperature range of −40°C to +125°C. The AD8663 LFCSP is specified over the industrial temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

7/07—Revision 0: Initial Version

SPECIFICATIONS

AD8663 ELECTRICAL CHARACTERISTICS

V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		30	175	µV
		−40°C < T_A < +85°C			300	µV
		−40°C < T_A < +125°C			450	µV
Input Bias Current	I_B			0.3		pA
		−40°C < T_A < +85°C			45	pA
		−40°C < T_A < +125°C			105	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C			35	pA
		−40°C < T_A < +125°C			35	pA
Input Voltage Range			0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.2 V to 3.0 V	76	100		dB
		−40°C < T_A < +125°C	76	100		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	106	114		dB
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		1.5	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.65	4.80		V
		−40°C < T_A < +125°C	4.60			V
Output Voltage Low	V_{OL}	I_L = 1 mA		150	200	mV
		−40°C < T_A < +125°C			250	mV
Short-Circuit Current	I_{SC}			±7		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		965		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 16 V	95	105		dB
		−40°C < T_A < +125°C	95			dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		210	275	µA
		−40°C < T_A < +125°C			325	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.26		V/µs
Gain Bandwidth Product	GBP	C_L = 20 pF		520		kHz
Phase Margin	Φ_O	C_L = 20 pF		60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		23		nV/√Hz
		f = 10 kHz		21		nV/√Hz

V_S = 16.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		40	300	µV
		−40°C < T_A < +85°C			450	µV
		−40°C < T_A < +125°C			450	µV
Input Bias Current	I_B			0.3		pA
		−40°C < T_A < +85°C		19	45	pA
		−40°C < T_A < +125°C		70	120	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C		11	35	pA
		−40°C < T_A < +125°C		21	65	pA
Input Voltage Range			0.2		14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.2 V to +14.5 V	87	109		dB
		−40°C < T_A < +125°C	87	109		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 15.5 V	106	111		dB
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		1.5	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	15.80	15.92		V
		I_L = 10 mA	14.80	15.12		V
		I_L = 10 mA, −40°C < T_A < +125°C	14.55			V
Output Voltage Low	V_{OL}	I_L = 1 mA		57	100	mV
		I_L = 10 mA		575	720	mV
		−40°C < T_A < +125°C			980	mV
Short-Circuit Current	I_{SC}			±42		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		720		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 16 V	95	105		dB
		−40°C < T_A < +125°C	95			dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		230	285	µA
		−40°C < T_A < +125°C			355	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.3		V/µs
Gain Bandwidth Product	GBP	C_L = 20 pF		540		kHz
Phase Margin	Φ_O	C_L = 20 pF		64		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		23		nV/√Hz
		f = 10 kHz		21		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	−0.1 V to V_S
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	
R-8	−40°C to +125°C
CP-8-2	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead LFCSP	75[1]	18[1]	°C/W

[1] Exposed pad soldered to application board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

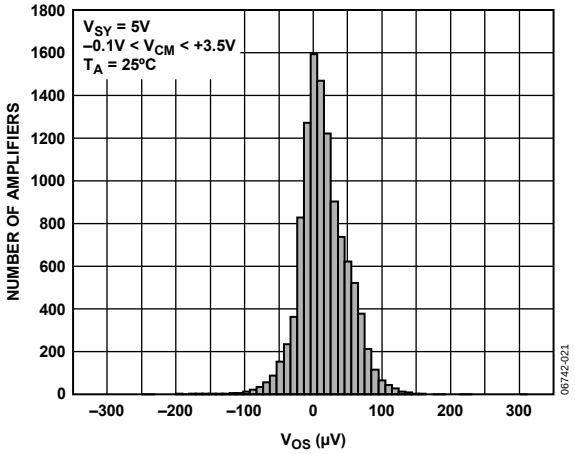

Figure 3. Input Offset Voltage Distribution

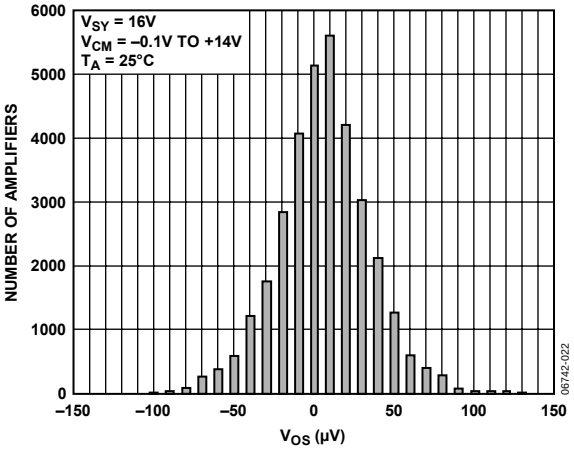

Figure 6. Input Offset Voltage Distribution

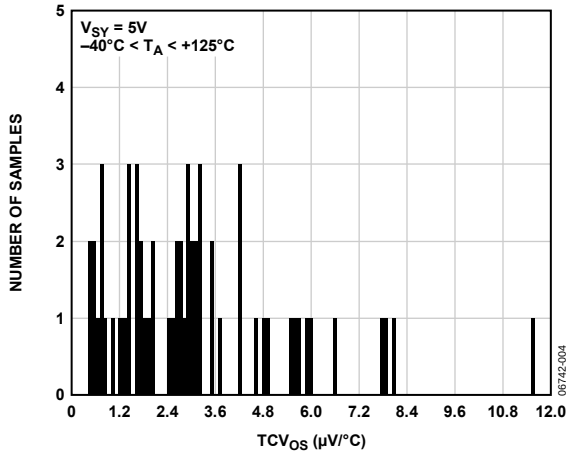

Figure 4. Offset Voltage Drift Distribution

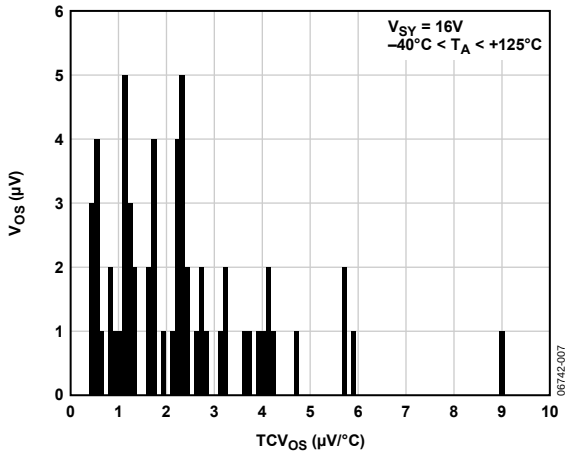

Figure 7. Offset Voltage Drift Distribution

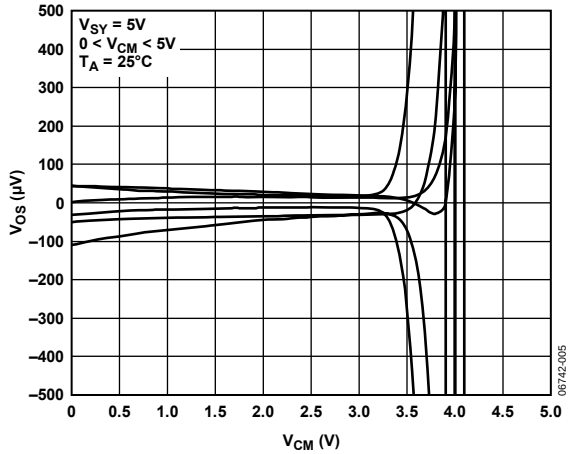

Figure 5. Input Offset Voltage vs. Common-Mode Voltage

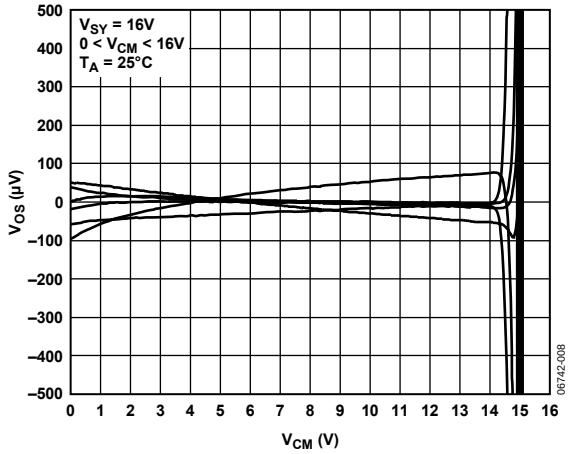

Figure 8. Input Offset Voltage vs. Common-Mode Voltage

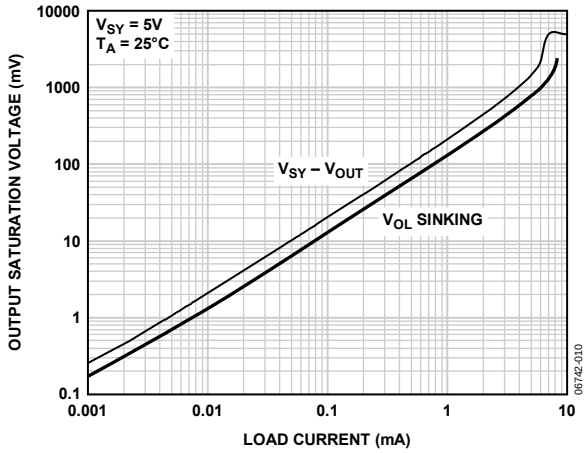

Figure 9. Output Swing Saturation Voltage vs. Load Current

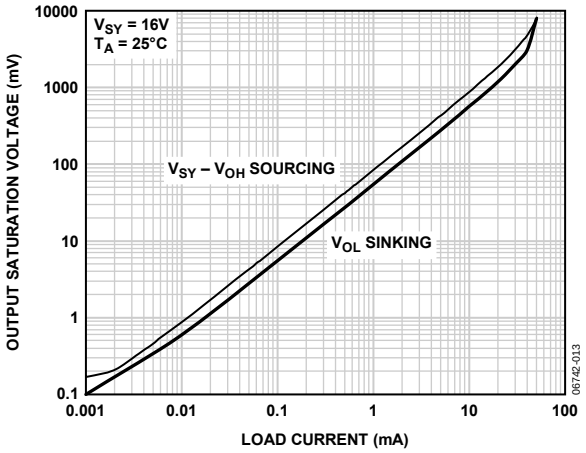

Figure 12. Output Swing Saturation Voltage vs. Load Current

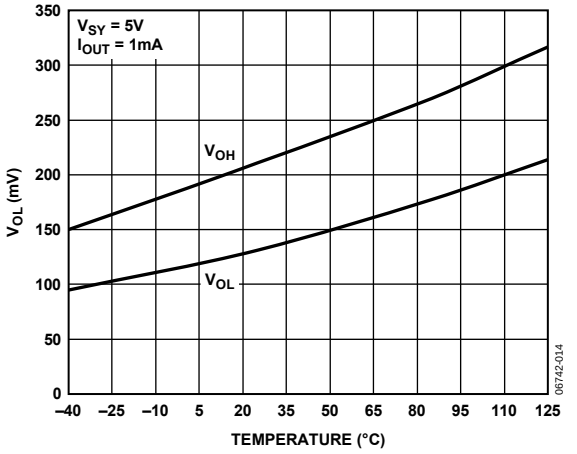

Figure 10. Output Voltage Saturation vs. Temperature

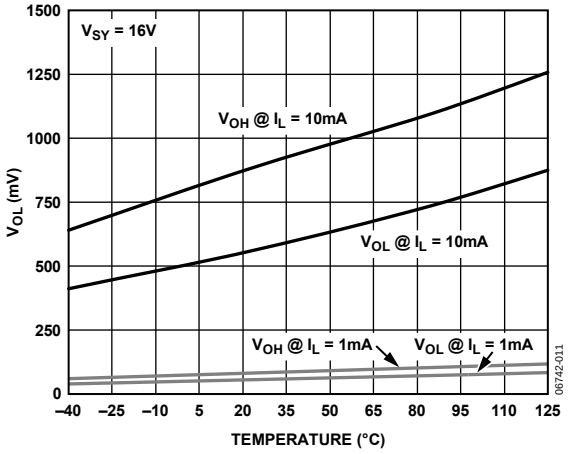

Figure 13. Output Voltage Saturation vs. Temperature

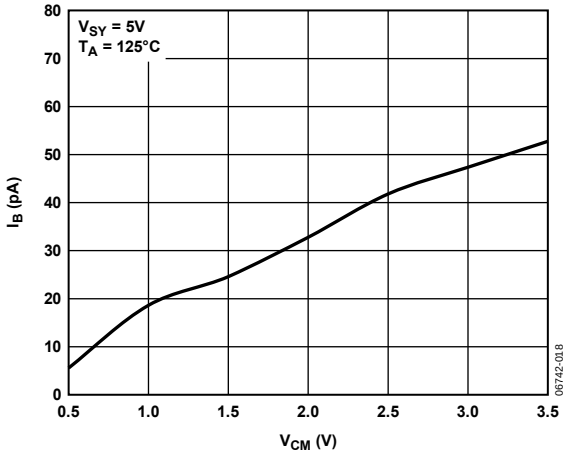

Figure 11. Input Bias Current vs. Common-Mode Voltage at 125°C

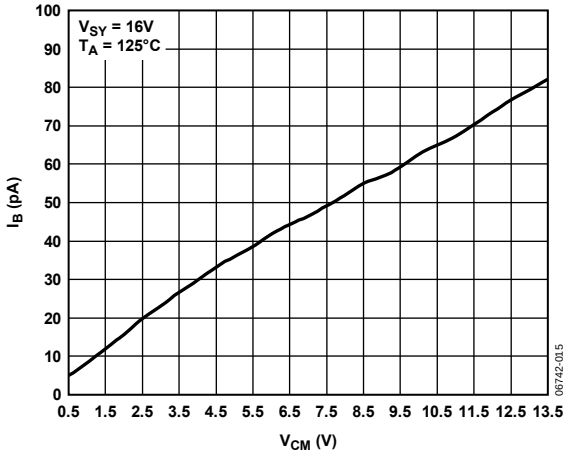

Figure 14. Input Bias Current vs. Common-Mode Voltage at 125°C

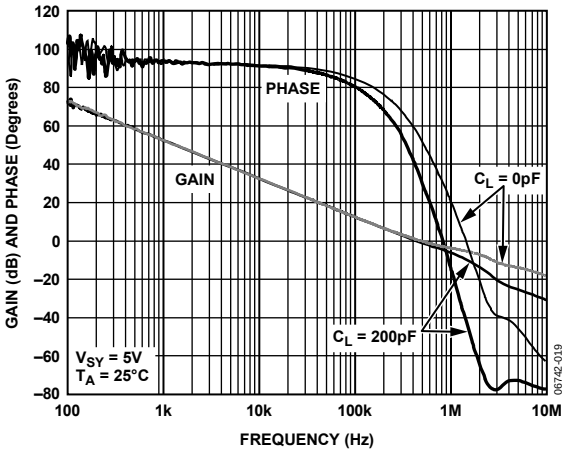

Figure 15. Open-Loop Gain and Phase Shift vs. Frequency

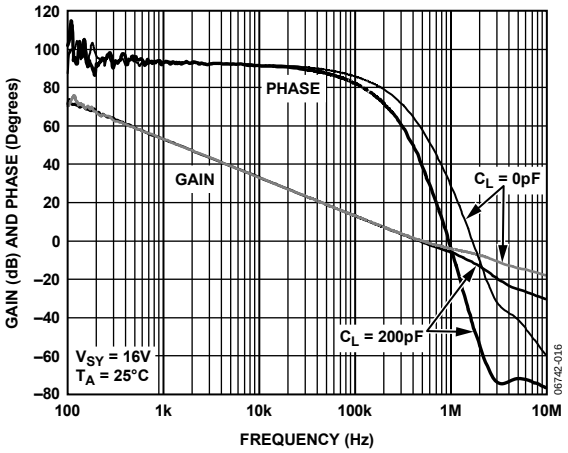

Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

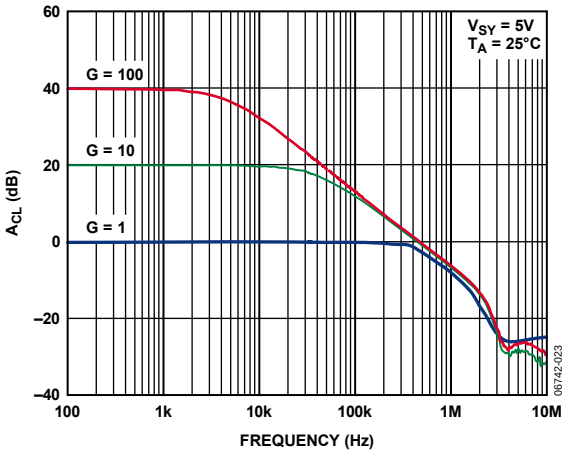

Figure 16. Closed-Loop Gain vs. Frequency

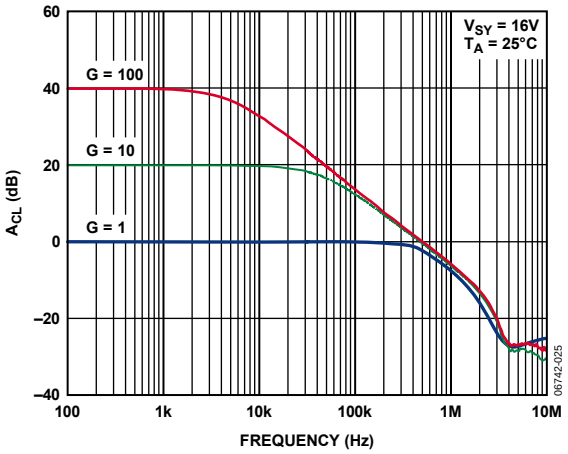

Figure 19. Closed-Loop Gain vs. Frequency

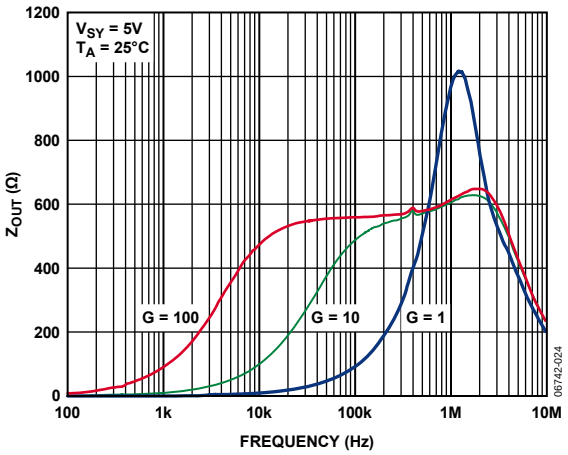

Figure 17. Closed-Loop Output Impedance vs. Frequency

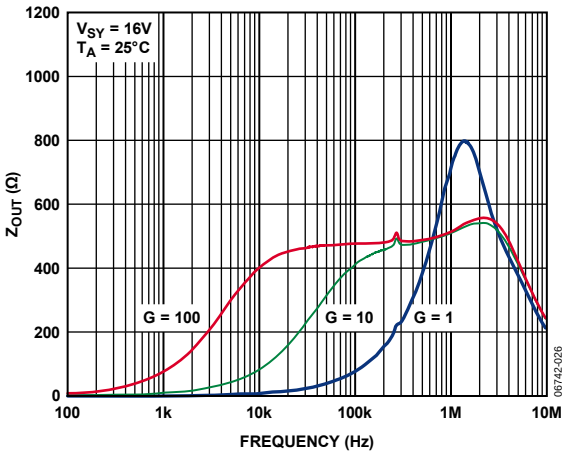

Figure 20. Closed-Loop Output Impedance vs. Frequency

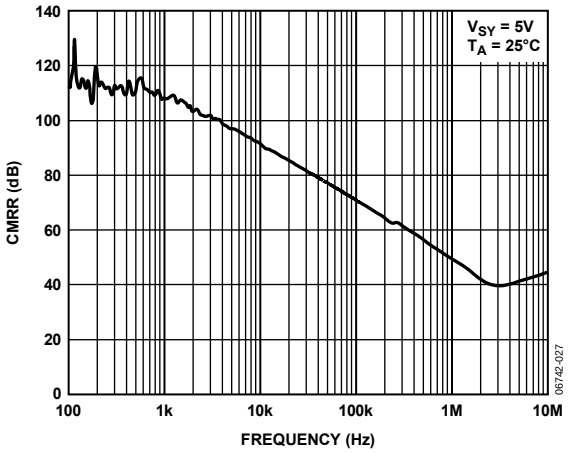

Figure 21. CMRR vs. Frequency

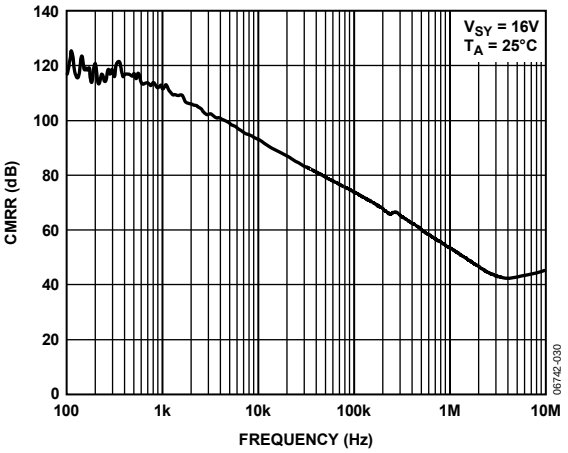

Figure 24. CMRR vs. Frequency

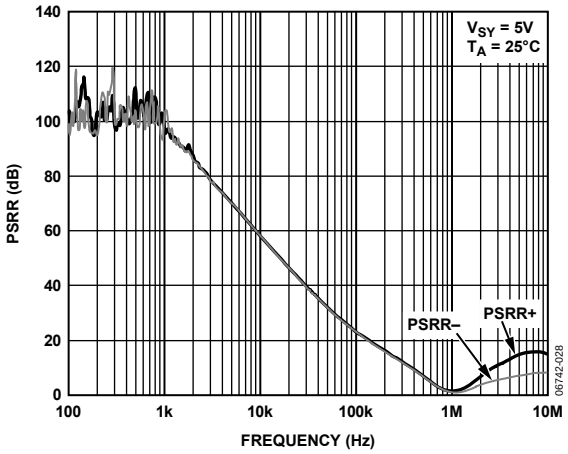

Figure 22. PSRR vs. Frequency

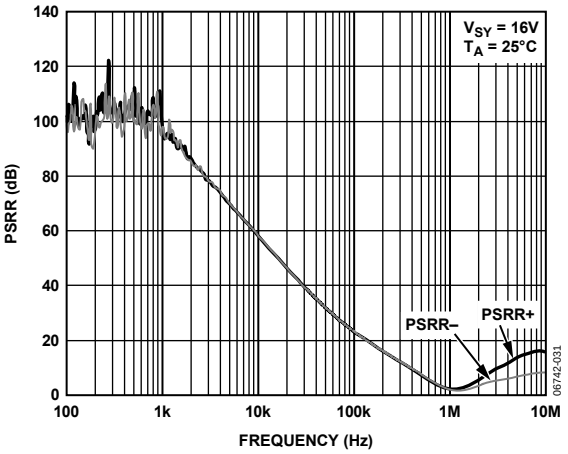

Figure 25. PSRR vs. Frequency

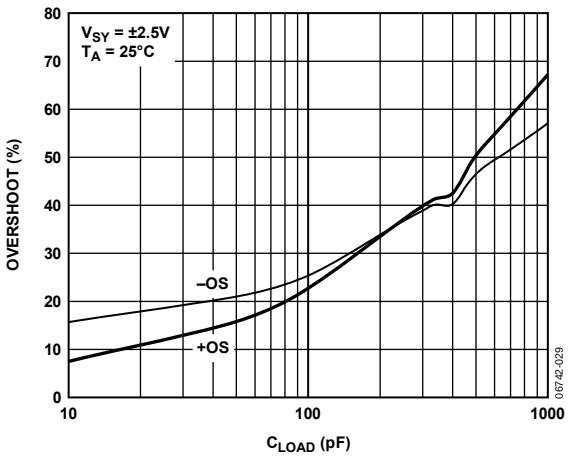

Figure 23. Small-Signal Overshoot vs. Load Capacitance

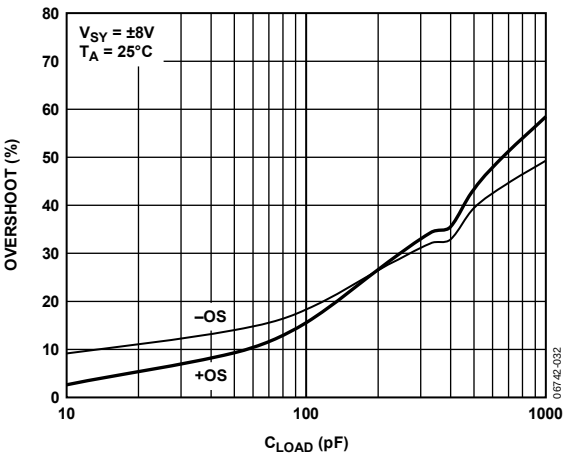

Figure 26. Small-Signal Overshoot vs. Load Capacitance

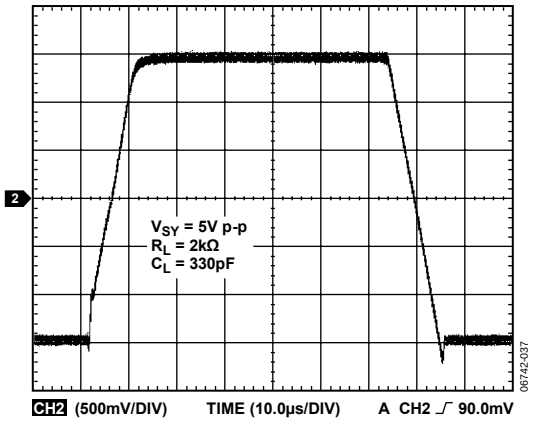

Figure 27. Large-Signal Transient Response

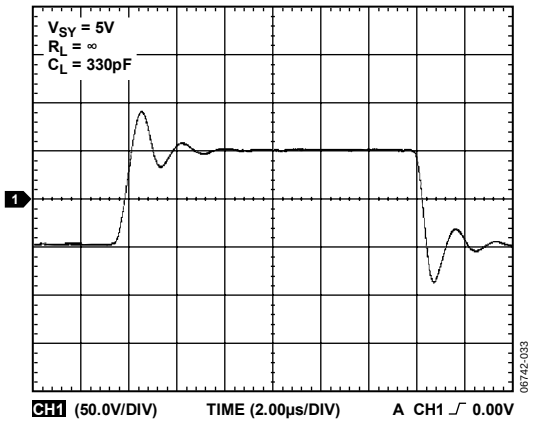

Figure 28. Small-Signal Transient Response

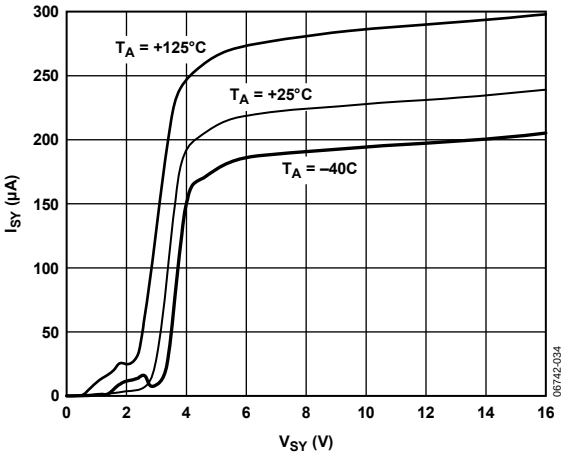

Figure 29. Supply Current vs. Supply Voltage

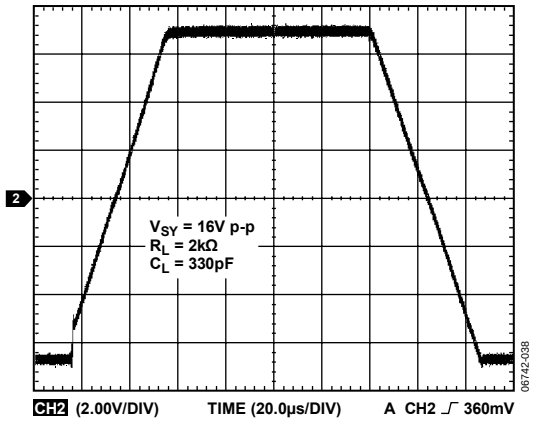

Figure 30. Large-Signal Transient Response

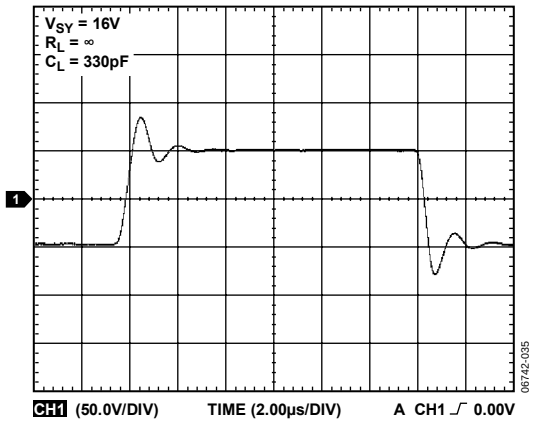

Figure 31. Small-Signal Transient Response

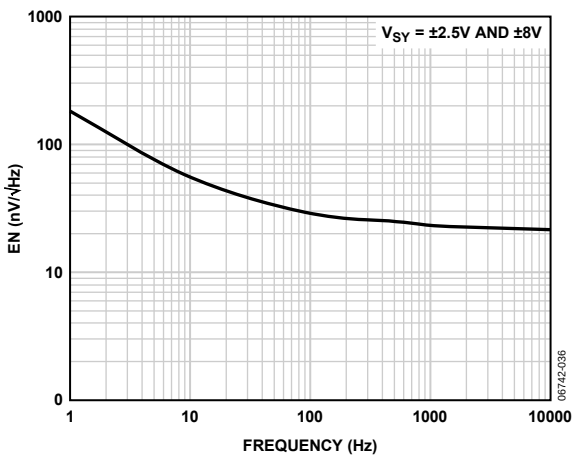

Figure 32. Voltage Noise Density

OUTLINE DIMENSIONS

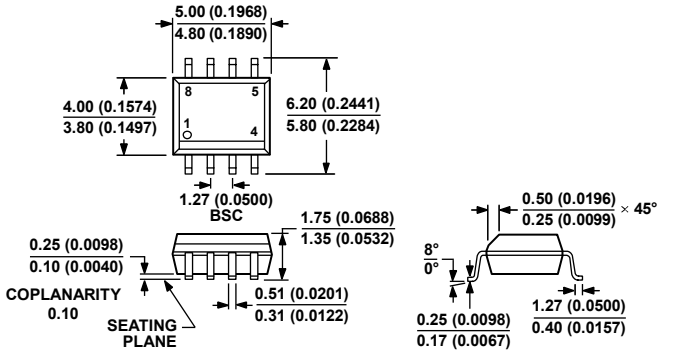

Figure 33. 8-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

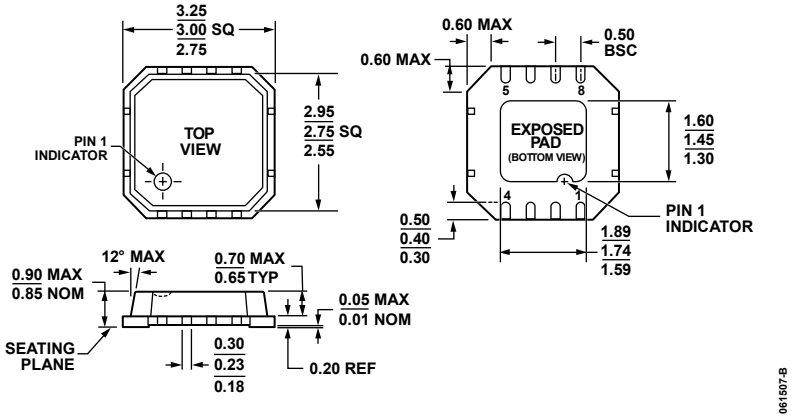

Figure 34. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8663ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8663ARZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8663ARZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8663ACPZ-R2[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A1U
AD8663ACPZ-REEL[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A1U
AD8663ACPZ-REEL7[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A1U

[1] Z = RoHS Compliant Part.

NOTES

D06742-0-7/07(0)