AAT2158
1.5A Low Noise Step-Down Converter

SwitchReg™

General Description

The AAT2158 SwitchReg is a 1.5A step-down converter with an input voltage range of 2.4V to 5.5V and an adjustable output voltage from 0.6V to V_{IN}. The 1.4MHz switching frequency enables the use of small external components. The small footprint and high efficiency make the AAT2158 an ideal choice for portable applications.

The AAT2158 delivers 1.5A maximum output current while consuming only 42µA of no-load quiescent current. Ultra-low $R_{DS(ON)}$ integrated MOSFETs and 100% duty cycle operation make the AAT2158 an ideal choice for high output voltage, high current applications which require a low dropout threshold.

The AAT2158 provides excellent transient response and high output accuracy across the operating range. No external compensation components are required.

The AAT2158 maintains high efficiency throughout the load range. The AAT2158's unique architecture produces reduced ripple and spectral noise. Over-temperature and short-circuit protection safeguard the AAT2158 and system components from damage.

The AAT2158 is available in a Pb-free, space-saving 16-pin 3x3mm QFN package. The product is rated over an operating temperature range of -40°C to +85°C.

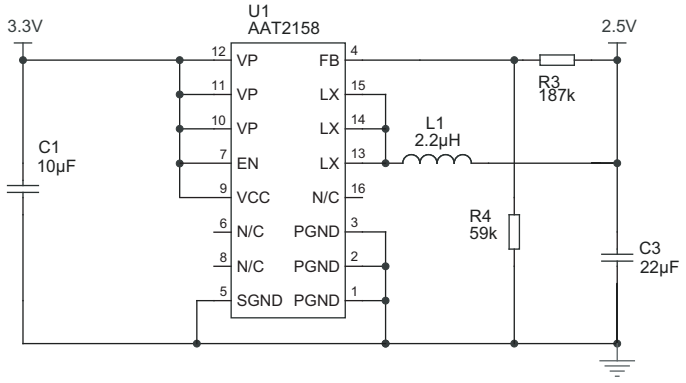
Features

- 1.5A Maximum Output Current
- Input Voltage: 2.4V to 5.5V
- Output Voltage: 0.6V to V_{IN}
- Up to 95% Efficiency
- Low Noise Light Load Mode
- 42µA No Load Quiescent Current
- No External Compensation Required
- 1.4MHz Switching Frequency
- 100% Duty Cycle Low-Dropout Operation
- Internal Soft Start
- Over-Temperature and Current Limit Protection
- <1µA Shutdown Current
- 16-Pin 3x3mm QFN Package
- Temperature Range: -40°C to +85°C

Applications

- Cellular Phones
- Digital Cameras
- Hard Disk Drives
- MP3 Players
- PDAs and Handheld Computers
- Portable Media Players
- USB Devices

Typical Application

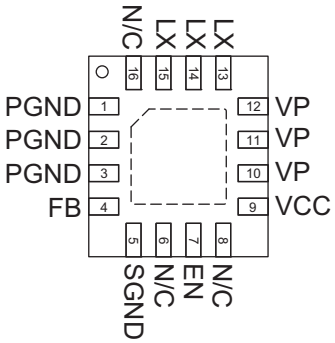


Pin Descriptions

Pin #	Symbol	Function
1, 2, 3	PGND	Main power ground return pin. Connect to the output and input capacitor return. (See board layout rules.)
4	FB	Feedback input pin. For an adjustable output, connect an external resistive divider to this pin. For fixed output voltage versions, FB is the output pin of the converter.
5	SGND	Signal ground. Connect the return of all small signal components to this pin. (See board layout rules.)
7	EN	Enable input pin. A logic high enables the converter; a logic low forces the AAT1158 into shutdown mode reducing the supply current to less than 1µA. The pin should not be left floating.
6, 8, 16	N/C	Not internally connected.
9	VCC	Bias supply. Supplies power for the internal circuitry. Connect to input power.
10, 11, 12	VP	Input supply voltage for the converter power stage. Must be closely decoupled to PGND.
13, 14, 15	LX	Connect inductor to these pins. Switching node internally connected to the drain of both high- and low-side MOSFETs.
EP		Exposed paddle (bottom); connect to PGND directly beneath package.

Pin Configuration

QFN33-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{CC}, V_P	V_{CC}, V_P to GND	6	V
V_{LX}	LX to GND	-0.3 to V_P + 0.3	V
V_{FB}	FB to GND	-0.3 to V_{CC} + 0.3	V
V_{EN}	EN to GND	-0.3 to -6	V
T_J	Operating Junction Temperature Range	-40 to150	°C

Thermal Characteristics

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance	50	°C/W
θ_{JC}	Maximum Thermal Resistance	4.2	°C/W
P_D	Maximum Power Dissipation (T_A = 25°C)[2, 3]	2.0	W

Recommended Operating Conditions

Symbol	Description	Value	Units
T_A	Ambient Temperature Range	-40 to 85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a demo board (FR4, in still air). Exposed pad must be mounted to PCB.
3. Derate 20mW/°C above 25°C.

Electrical Characteristics[1]

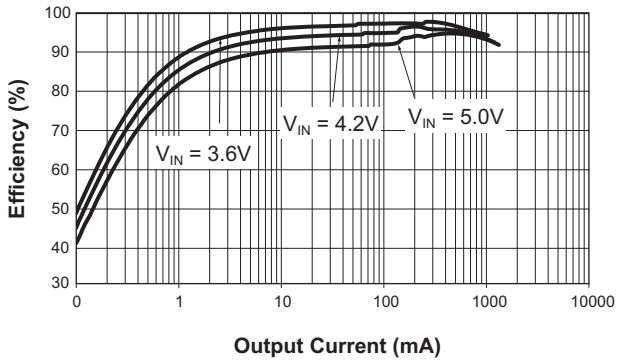
V_{IN} = 3.6V; T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.4		5.5	V
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.4	V
		Hysteresis		250		mV
		V_{IN} Falling	1.8			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0A to 1.5A, V_{IN} = 2.4V to 5.5V	-3.0		3.0	%
I_Q	Quiescent Current	No Load		42	90	µA
I_{SHDN}	Shutdown Current	V_{EN} = GND			1.0	µA
I_{LIM}	Current Limit		1.8			A
$R_{DS(ON)H}$	High Side Switch On-Resistance			0.120		Ω
$R_{DS(ON)L}$	Low Side Switch On-Resistance			0.085		Ω
$\Delta V_{LOADREG}$	Load Regulation	I_{LOAD} = 0A to 1.5A		0.5		%
$\Delta V_{LINEREG}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.4V to 5.5V		0.2		%/V
V_{FB}	Feedback Threshold Voltage Accuracy (Adjustable Version)	No Load, T_A = 25°C	0.591	0.60	0.609	V
I_{FB}	FB Leakage Current	V_{OUT} = 1.0V			0.2	µA
F_{OSC}	Internal Oscillator Frequency		1.12	1.4	1.68	MHz
T_S	Start-Up Time	From Enable to Output Regulation		150		µs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
EN						
V_{IL}	Enable Threshold Low				0.6	V
V_{IH}	Enable Threshold High		1.4			V
I_{EN}	Enable Leakage Current	V_{IN} = V_{EN} = 5.5V	-1.0		1.0	µA

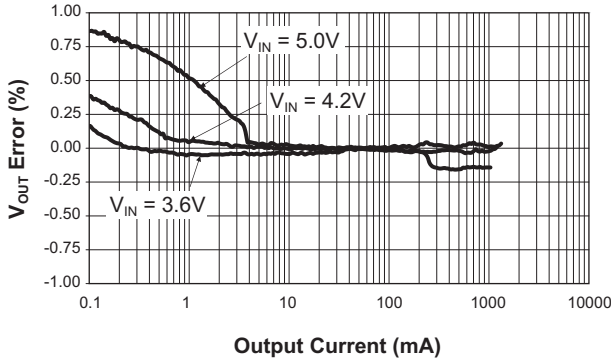
1. The AAT2158 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

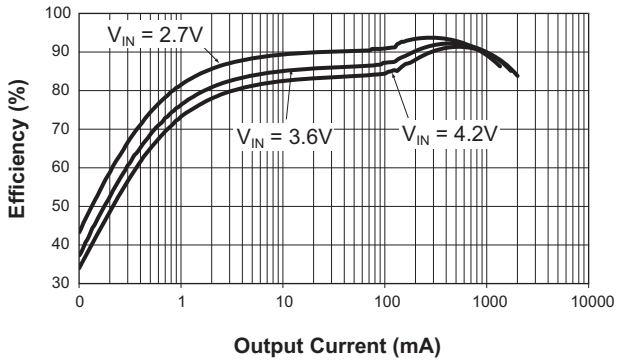
Efficiency vs. Output Current
(V_{OUT} = 3.3V)



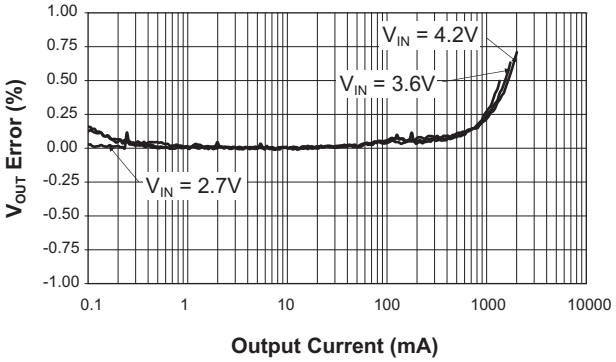
Load Regulation
(V_{OUT} = 3.3V)



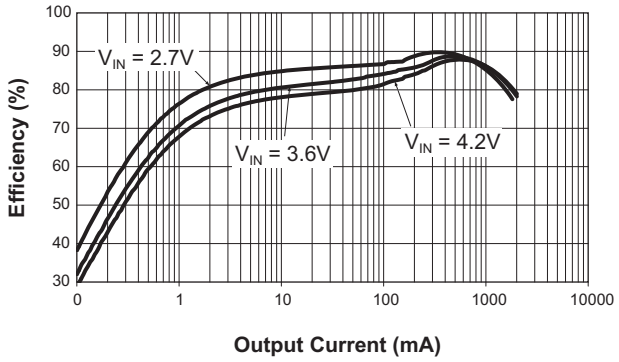
Efficiency vs. Output Current
(V_{OUT} = 1.8V)



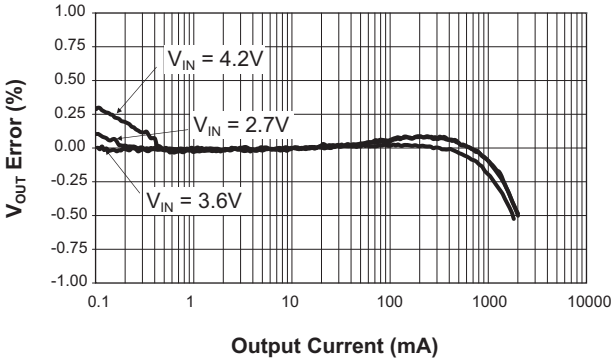
Load Regulation
(V_{OUT} = 1.8V)



Efficiency vs. Output Current
(V_{OUT} = 1.2V)

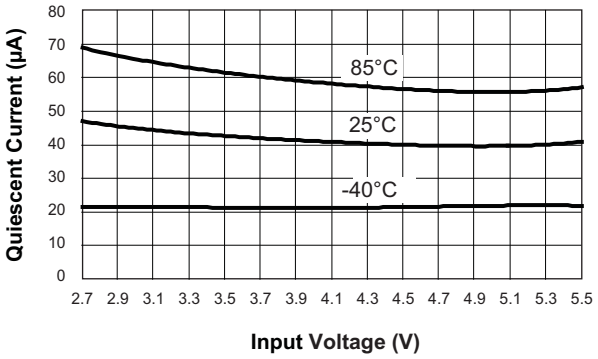


Load Regulation
(V_{OUT} = 1.2V)

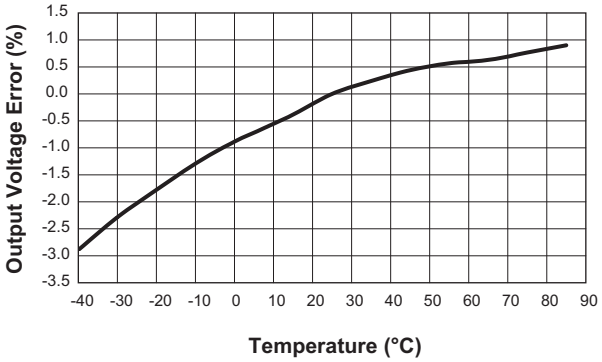


Typical Characteristics

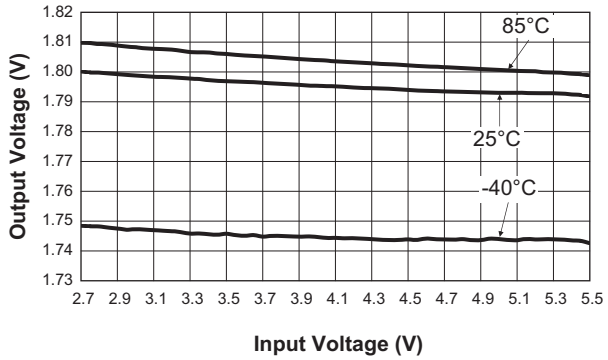
Quiescent Current vs. Input Voltage
(V_{OUT} = 1.8V; No Load)



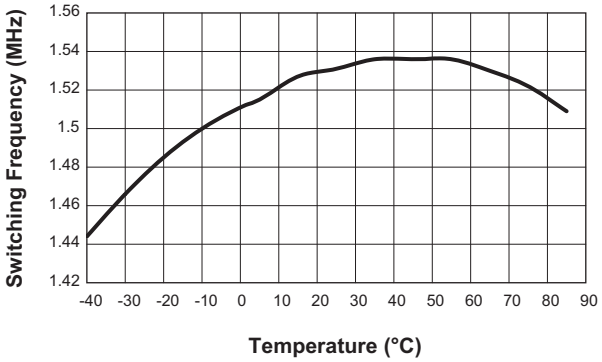
Output Voltage vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 1A)



Output Voltage vs. Input Voltage
(V_{OUT} = 1.8V; I_{OUT} = 1A)

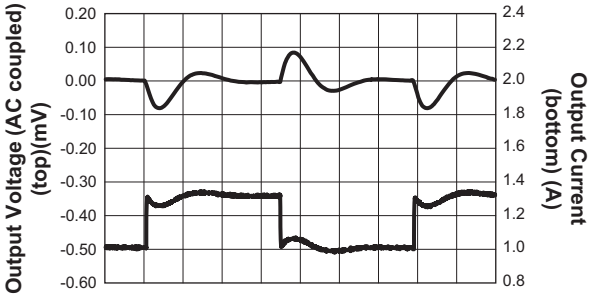


Switching Frequency vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 1A)



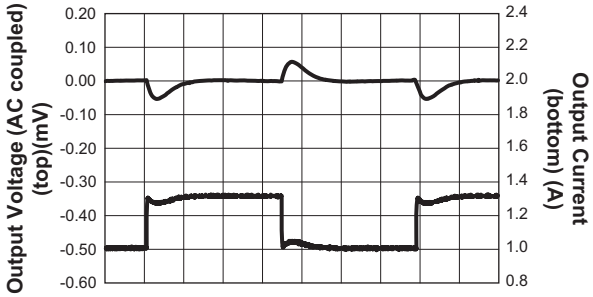
Typical Characteristics

Load Transient Response
(V_{OUT} = 1.8V)



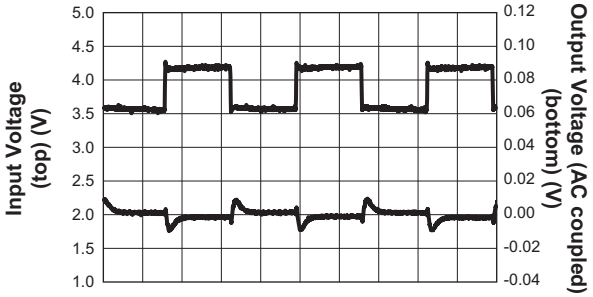
Time (100µs/div)

Load Transient Response
(V_{OUT} = 1.8V; C_{FF} = 100pF)



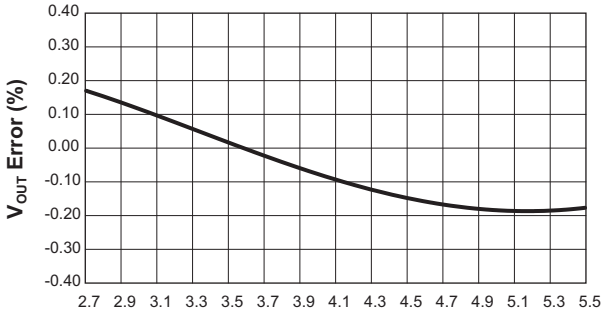
Time (100µs/div)

Line Transient Response
(V_{OUT} = 1.8V; I_{OUT} = 1.5A; C_{FF} = 100pF)



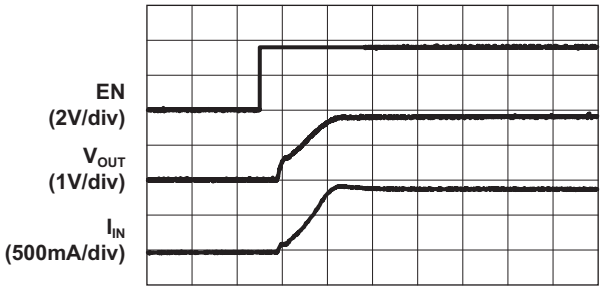
Time (100µs/div)

Line Regulation
(V_{OUT} = 1.8V; I_{OUT} = 1A)



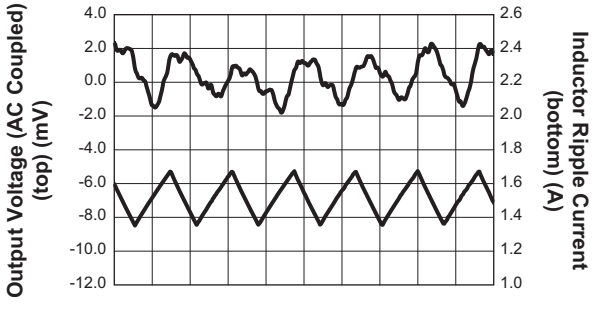
Input Voltage (V)

Enable Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.5A)



Time (100µs/div)

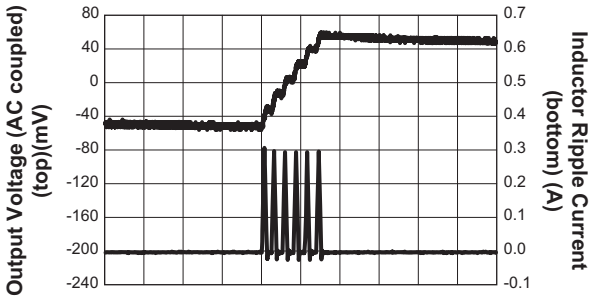
Heavy Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.5A)



Time (500ns/div)

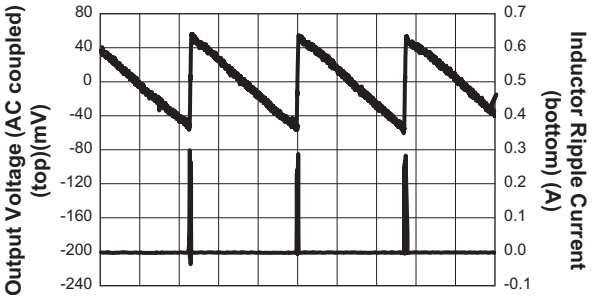
Typical Characteristics

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 0pF)



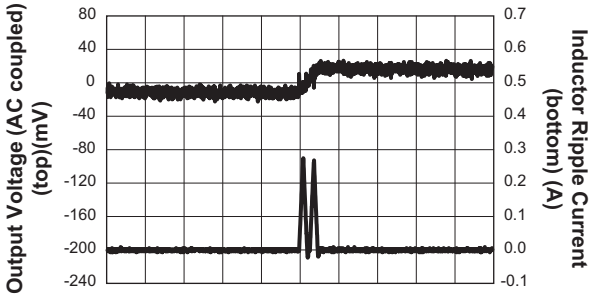
Time (5µs/div)

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 0pF)



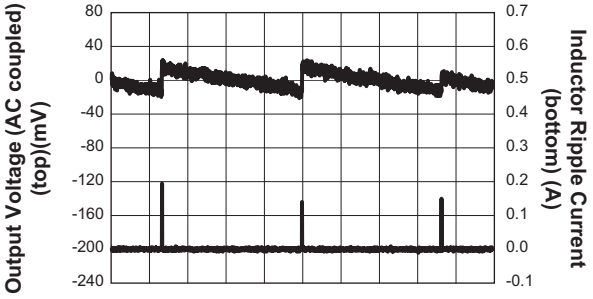
Time (200µs/div)

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 100pF)



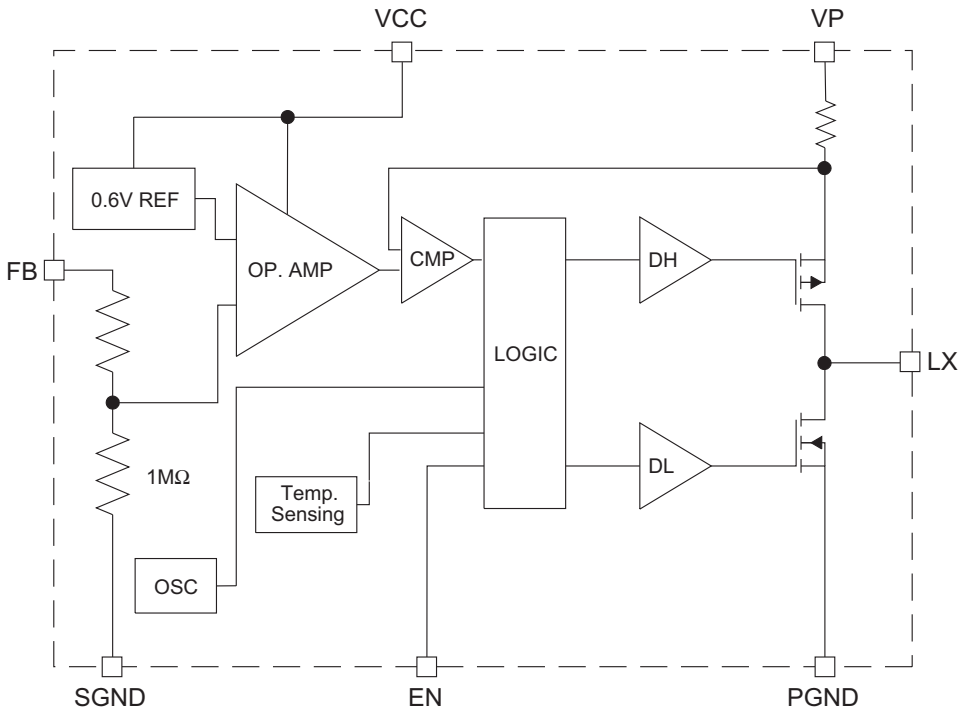
Time (5µs/div)

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 100pF)



Time (500µs/div)

Functional Block Diagram



Functional Description

The AAT2158 is a high performance 1.5A monolithic step-down converter operating at a 1.4MHz switching frequency. It minimizes external component size, optimizes efficiency over the complete load range, and produces reduced ripple and spectral noise. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 3.3µH inductor and a 22µF ceramic capacitor are recommended for a 3.3V output (see table of recommended values).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high-side MOSFET (plus the DC drop of the external inductor). The device integrates extremely low $R_{DS(ON)}$ MOSFETs to achieve low dropout voltage during 100% duty cycle operation. This is advantageous in applications requiring high output voltages (typically > 2.5V) at low input voltages.

The integrated low-loss MOSFET switches can provide greater than 95% efficiency at full load. Light load operation maintains high efficiency, low ripple and low spectral noise even at lower currents (typically <150mA).

In battery-powered applications, as V_{IN} decreases, the converter dynamically adjusts the operating frequency prior to dropout to maintain the required duty cycle and provide accurate output regulation. Output regulation is maintained until the dropout voltage, or minimum input voltage, is reached. At 1.5A output load, dropout voltage headroom is approximately 200mV.

The AAT2158 typically achieves better than ±0.5% output regulation across the input voltage and output load range. A current limit of 2.0A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 42µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. Soft start eliminates output voltage overshoot when the enable or the input voltage is applied. Under-voltage lockout prevents spurious start-up events.

Control Loop

The AAT2158 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2158 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

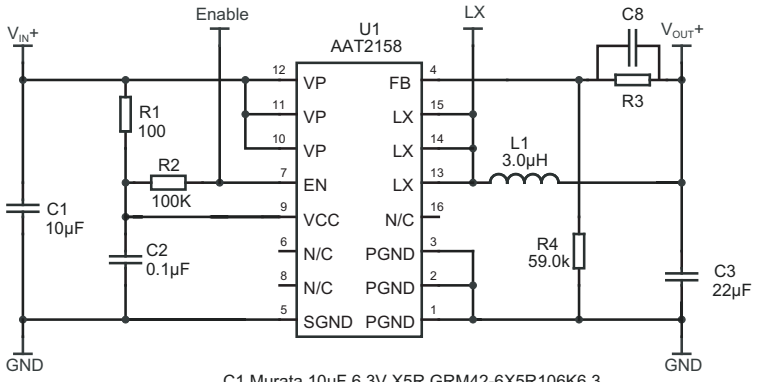
Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VCC input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.



V_{OUT}(V)	R3 (kΩ)
0.8	19.6
0.9	29.4
1.0	39.2
1.1	49.9
1.2	59.0
1.3	68.1
1.4	78.7
1.5	88.7
1.8	118
2.0	137
2.5	187
3.3	267

C1 Murata 10µF 6.3V X5R GRM42-6X5R106K6.3
C3 Murata 22µF 6.3V GRM21BR60J226ME39L X5R 0805
L1 Sumida CDRH5D28-3R0NC (see Table 2)
R1 and C2 are an optional noise filter for internal V_{CC}.
R6, C4, C5-C7 are not populated
C8 100pF feed forward

Figure 3: AAT2158 Evaluation Schematic.

Component Selection

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The inductor should be set equal to the output voltage numeric value in µH. This guarantees that there is sufficient internal slope compensation.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 3.3µH CDRH4D28 series Sumida inductor has a 49.2mΩ worst case DCR and a 1.57A DC current rating. At full 1.5A load, the inductor DC loss is 97mW which gives less than 1.5% loss in efficiency for a 1.5A, 3.3V output.

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2158. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 2).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Adjustable Output Resistor Selection

The output voltage on the AAT2158 is programmed with external resistors R3 and R4. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R4 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

The external resistor R3, combined with an external 100pF feed forward capacitor (C8 in Figure 1), delivers enhanced transient response for extreme pulsed load applications and reduces ripple in light load conditions. The addition of the feed forward capacitor typically requires a larger output capacitor C3-C4 for stability. The external resistors set the output voltage according to the following equation:

$$V_{OUT} = 0.6V \left(1 + \frac{R3}{R4}\right)$$

or

$$R3 = \left[\left(\frac{V_{OUT}}{V_{REF}} - 1\right)\right] R4$$

V_{OUT} (V)	R4 = 59kΩ R3 (kΩ)	R4 = 221kΩ R3 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.0	237	887
3.3	267	1000

Table 1: AAT2158 Resistor Values for Various Output Voltages.

Thermal Calculations

There are three types of losses associated with the AAT2158 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)H} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the QFN33-16 package, which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT2158 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C1) should connect as closely as possible to VP and PGND.
2. C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or FB pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground to avoid unwanted noise coupling.

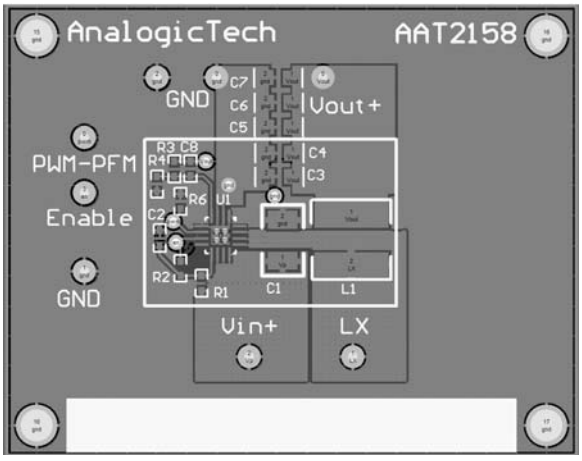


Figure 2: AAT2158 Evaluation Board Top Side Layout.

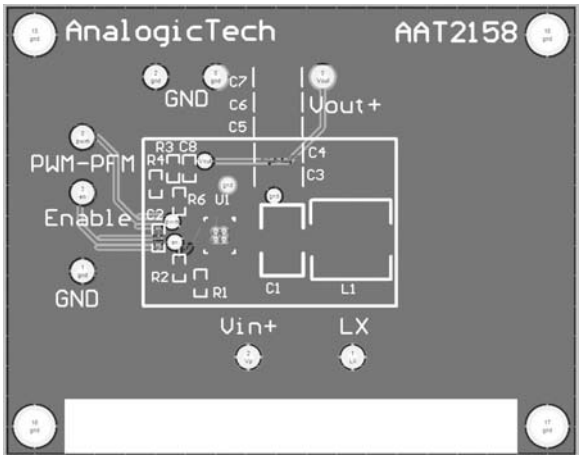


Figure 3: AAT2158 Evaluation Board Bottom Side Layout.

Design Example

Specifications

V_O 3.3V @ 1.4A, Pulsed Load ΔI_{LOAD} = 1.4A

V_{IN} 2.7V to 4.2V (3.6V nominal)

F_S 1.2MHz

T_{AMB} 85°C in QFN33-16 Package

Output Inductor

L1 = V_O(µH) = 3.3µH; see Table 2.

For Sumida inductor CDRH4D28 3.3µH DCR = 49.2mΩ max.

$$\Delta I_1 = \frac{V_O}{L1 \cdot F_S} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{3.3V}{3.3\mu H \cdot 1.2MHz} \cdot \left(1 - \frac{3.3V}{4.2V}\right) = 179mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I_1}{2} = 1.4A + 0.089A = 1.49A$$

$$P_{L1} = I_{O1}^2 \cdot DCR = 1.4A^2 \cdot 49.2m\Omega = 96mW$$

Output Capacitor

V_{DROOP} = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 1.4A}{0.2V \cdot 1.2MHz} = 17.5\mu F; \text{ use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (4.2V - 3.3V)}{3.3\mu H \cdot 1.2MHz \cdot 4.2V} = 52mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (52mA)^2 = 13.3\mu W$$

Input Capacitor

Input Ripple V_{PP} = 50mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{50mV}{1.4A} - 5m\Omega\right) \cdot 4 \cdot 1.2MHz} = 6.8\mu F; \text{ use } 10\mu F$$

$$I_{RMS(MAX)} = \frac{I_O}{2} = 0.7Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.7A)^2 = 2.45mW$$

AAT2158 Losses

Total losses can be estimated by calculating the dropout ($V_{IN} = V_O$) losses where the power MOSFET $R_{DS(ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 120°C junction temperature with the QFN 50°C/W package.

$$P_{LOSS} = I_{O1}^2 \cdot R_{DS(ON)H} = 1.4A^2 \cdot 0.16\Omega = 0.31W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 310mW = 101°C$$

The total losses are also investigated at the nominal lithium-ion battery voltage (3.6V). The simplified version of the $R_{DS(ON)}$ losses assumes that the N-channel and P-channel $R_{DS(ON)}$ are equal.

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)} + [(t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}]$$

$$= 1.4A^2 \cdot 152m\Omega + [(5ns \cdot 1.2MHz \cdot 1.4A + 50\mu A) \cdot 3.6V] = 328mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 328mW = 101°C$$

V_{OUT} (V)	Inductance (µH)	Part Number	Manufacturer	Size (mm)	Rated Current (A)	I_{RMS} (A)	I_{SAT} (A)	DCR (Ω)
3.3	3.0	CDRH5D28	Sumida	6x6x3	2.4			24.0
3.3	3.3	CDRH4D28	Sumida	5x5x3	1.57			49.2
2.5	2.2	CDRH4D28	Sumida	5x5x3	2.04			31.3
1.8	1.8	CDRH4D28	Sumida	5x5x3	2.2			27.5
1.5	1.8	CDRH4D28	Sumida	5x5x3	2.2			27.5
1.2	1.2	CDRH4D28	Sumida	5x5x3	2.56			23.6
1.0	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.8	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.6	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042

Table 2: Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
MuRata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
MuRata	GRM21BR60J226ME39	22µF	6.3V	X5R	0805

Table 3: Surface Mount Capacitors.

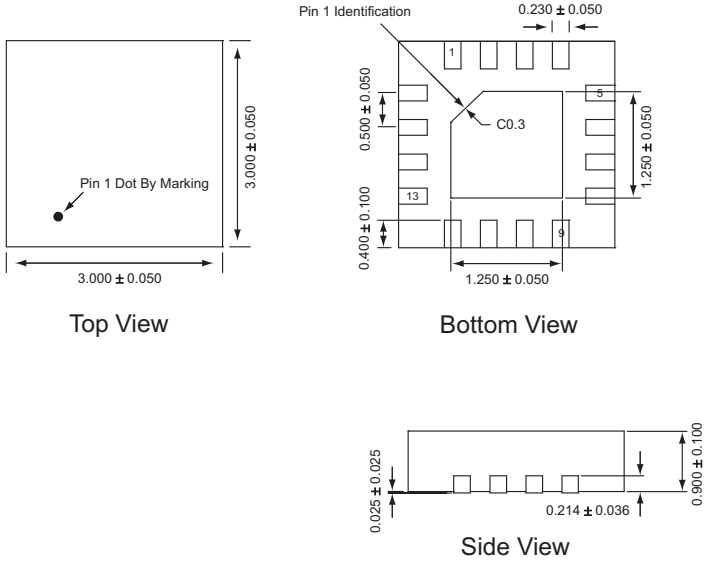
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
QFN33-16	XSXYY	AAT2158IVN-0.6-T1

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Package Information[3]

QFN33-16



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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