SBOS375 − NOVEMBER 2006

Precision Voltage-to-Current Converter/Transmitter

FEATURES

- **EASY-TO-DESIGN INPUT/OUTPUT RANGES: 0mA−20mA, 4mA−20mA, 5mA−25mA AND VOLTAGE OUTPUTS**
- **NONLINEARITY: 0.002%**
- **LOW OFFSET DRIFT: 1μV/°C**
- **ACCURACY: 0.015%**
- **SINGLE-SUPPLY OPERATION**
- **WIDE SUPPLY RANGE: 7V TO 44V**
- **OUTPUT ERROR FLAG ($\overline{EF}$)**
- **OUTPUT DISABLE (OD)**
- **ADJUSTABLE VOLTAGE REGULATOR: 3V TO 15V**

APPLICATIONS

- **UNIVERSAL VOLTAGE-CONTROLLED CURRENT SOURCE**
- **CURRENT OR VOLTAGE OUTPUT FOR 3-WIRE SENSOR SYSTEMS**
- **PLC OUTPUT PROGRAMMABLE DRIVER**
- **CURRENT-MODE SENSOR EXCITATION**

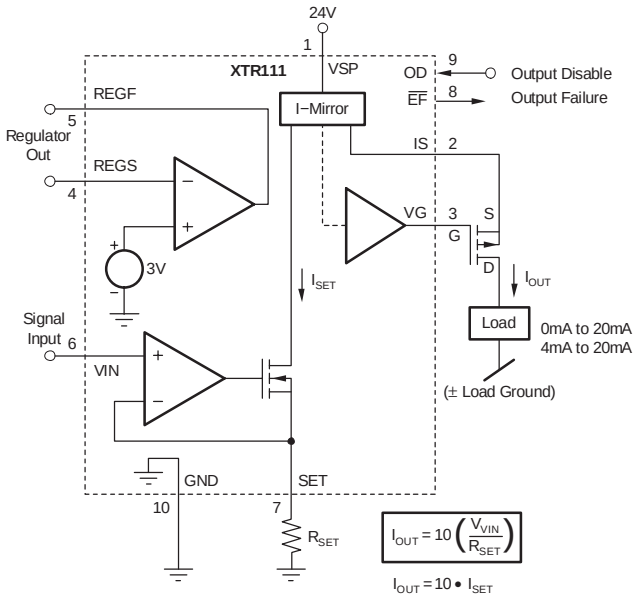
DESCRIPTION

The XTR111 is a precision voltage-to-current converter designed for the standard 0mA−20mA or 4mA−20mA analog signals, and can source up to 36mA. The ratio between input voltage and output current is set by the single resistor R_{SET}. The circuit can also be modified for voltage output.

An external P-MOSFET transistor ensures high output resistance and a broad compliance voltage range extending from 2V below the supply voltage, V_{VSP}, to voltages well below GND.

The adjustable 3V to 15V sub-regulator output provides the supply voltage for additional circuitry.

The XTR111 is available in a DFN surface-mount package.



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ABSOLUTE MAXIMUM RATINGS(1)(2)

Power Supply Voltage, V_{VSP}	+44V
Voltage at SET(3)	−0.5V to +14V
Voltage at IS(3, 5)	(V_{VSP}) − 5.5V to (V_{VSP}) + 0.5V
Voltage at REGS, REGF, VIN, OD, $\overline{EF}$	−0.5V to (V_{VSP}) + 0.5V
Voltage at REGF, VG	−0.5V to (V_{VSP}) + 0.5V
Current into any pin(3, 4)	±25mA
Output Short-Circuit Duration(5):	
VG	Continuous to common and V_{VSP}
REGF	Continuous to common and V_{VSP}
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Electrostatic Discharge Rating (HBM)	2000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Refer to the Package Option Addendum at the end of this document for lead temperature ratings.

(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited.

(4) The IS pin can source up to the output current-limit under normal operating conditions.

(5) See text in Application Section regarding safe voltage ranges and currents.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
XTR111	DFN-10	DRC	BSV

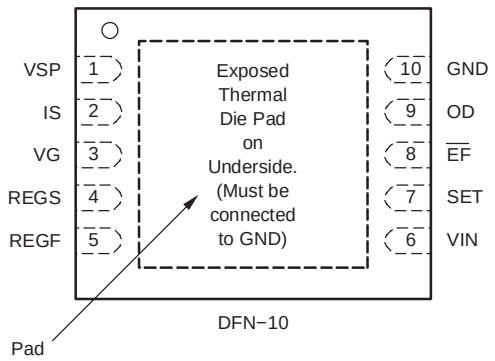
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	VSP	Positive Supply
2	IS	Source Connection
3	VG	Gate Drive
4	REGS	Regulator Sense
5	REGF	Regulator Force
6	VIN	Input Voltage
7	SET	Transconductance Set
8	$\overline{EF}$	Error Flag (Active Low)
9	OD	Output Disable (Active High)
10	GND	Negative Supply
Pad	Pad	Exposed Thermal Pad must be connected to GND

PIN CONFIGURATIONS

TOP VIEW **DFN**



DFN−10

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**.

All specifications at T_A = +25°C, V_{VSP} = +24V, R_{SET} = 2.0kΩ; REGF connected to REGS; OD = Low, External FET connected, unless otherwise noted.

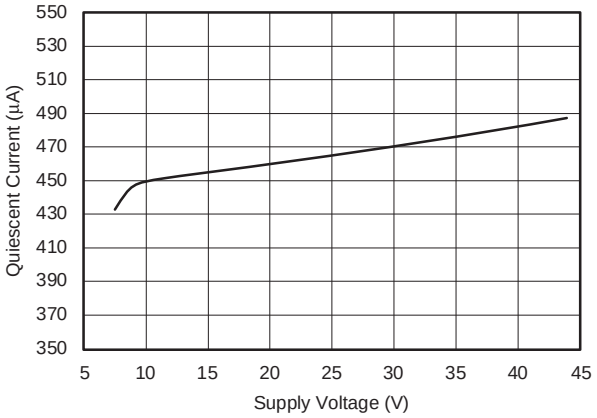
PARAMETER		CONDITION	XTR111 MIN	XTR111 TYP	XTR111 MAX	UNITS
TRANSMITTER						
Transfer Function				$I_{OUT} = 10 \bullet V_{VIN}/R_{SET}$		
Specified Output Current	I_{OUT}	Specified Performance(1)	0.1		25	mA
		Derated Performance(2)		0 to 36		mA
Current Limit for Output Current				42 ± 6		mA
Nonlinearity, I_{OUT}/I_{SET}(2, 3)		0.1 to 25mA		0.002	0.02	% of Span
		0.1 to 36mA		0.004		% of Span
Offset Current	I_{OS}	I_{OUT} = 4mA(1)		0.002	0.02	% of Span
vs Temperature				**0.0002**	**0.001**	**% of Span/°C**
vs Supply, V_{VSP}		8 to 40V Supply		0.0001	0.005	% of Span/V
Span Error, I_{OUT}/I_{SET}(2)		0.1mA to 25mA		0.015	0.1	% of Span
vs Temperature(2)		(1)		**5**		**ppm/°C**
vs Supply		(1)		0.0001		% of Span/V
Output Resistance		From Drain of Q_{EXT}(4)		> 1		GΩ
Output Leakage		OD = high		< 1		µA
Input Impedance (VIN)				2.4/30		GΩ/pF
Input Bias Current (VIN)	I_B			15	25	nA
Input Offset Voltage(2)	V_{OS}	V_{VIN} = 20mV		0.3	1.5	mV
vs Temperature				**1**		**µV/°C**
Input Voltage Range(5)	**V_{VIN}**			**0 to 12**		**V**
Noise, Referred to Input(2)		0.1Hz to 10Hz; I_{OUT} = 4mA		2.5		μV_{PP}
Dynamic Response				See Dynamic Performance Section		
V-Regulator Output (REGF)						
Voltage Reference(2)		R_{LOAD} = 5kΩ	2.85	3.0	3.15	V
vs Temperature(2)				**30**		**ppm/°C**
vs Supply(2)				0.1		mV/V
Bias Current into REGS(2)				0.8		µA
Load Regulation		0.6mA to 5mA		3	5	mV/mA
Supply Regulation(2)		R_{LOAD} = 5kΩ		0.01		mV/V
Output Current			5			mA
Short-Circuit Output Current				21		mA
DIGITAL INPUT (OD)						
V_{IL} Low-Level Threshold					**0.6**	**V**
V_{IH} High-Level Threshold			**1.8**			**V**
Internal Pull-up Current		V_{OD} < 5.5V		4		µA
DIGITAL OUTPUT ($\overline{EF}$)						
I_{OH} Leakage Current (Open Drain)				1		µA
V_{OL} Low-Level Output Voltage		I_{EF} = 2.2mA			0.8	V
I_{OL} Current to 400mV Level		V_{EF} = 400mV		2		mA
POWER SUPPLY						
Specified Voltage Range			+8		+40	V
Operating Voltage				+7 to +44		V
Quiescent Current(2)	I_Q	I_{OUT} = 0mA		450	550	µA
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−55		+125	°C
Package Thermal Impedance, θ_{JA}						
DFN				70		°C/W

(1) Includes input amplifier, but excludes R_{SET} tolerance.
(2) See Typical Characteristics.
(3) Span is the change in output current resulting from a full−scale change in input voltage.
(4) Within compliance range limited by (+V_{VSP} − 2V) +V_{DS} required for linear operation of Q_{EXT}.
(5) See Application Information, *Input Voltage* section.

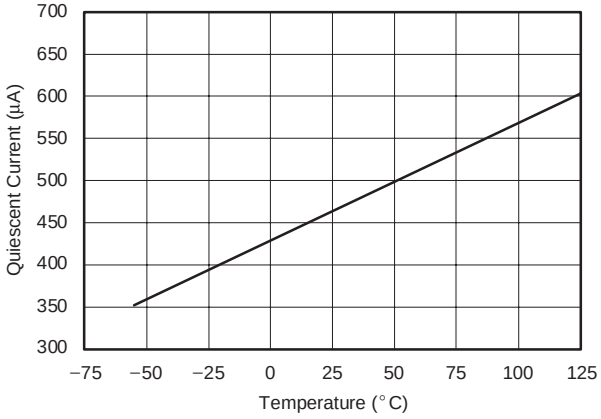
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

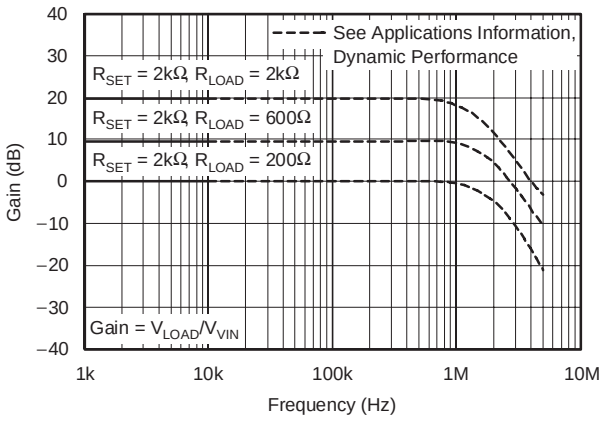
QUIESCENT CURRENT vs SUPPLY VOLTAGE



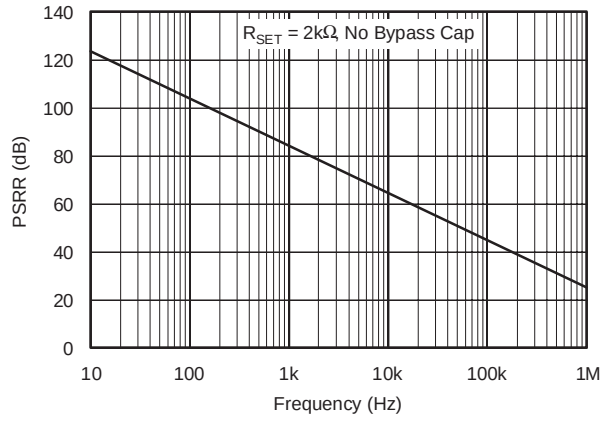
QUIESCENT CURRENT vs TEMPERATURE



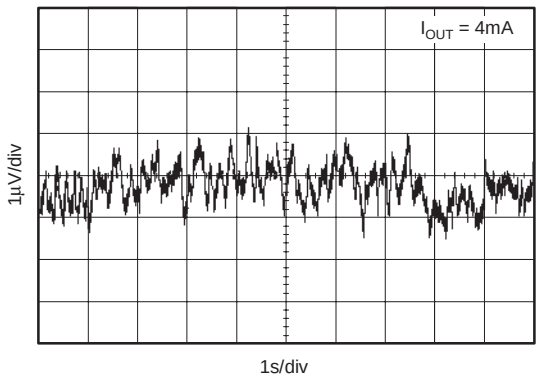
GAIN vs FREQUENCY



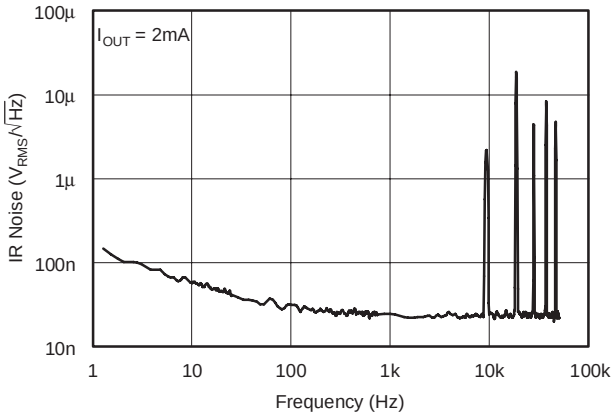
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



0.1Hz to 10Hz NOISE, RTI



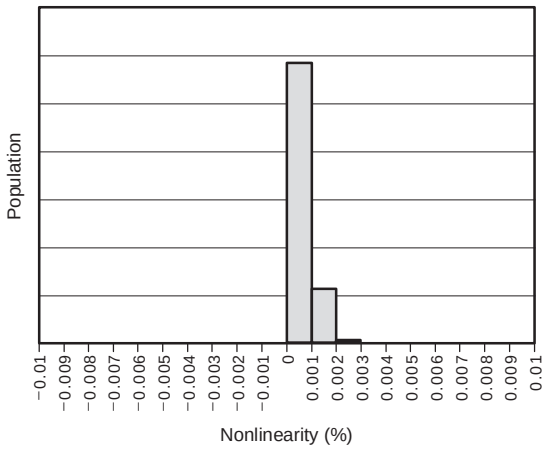
INPUT−REFERRED NOISE SPECTRUM



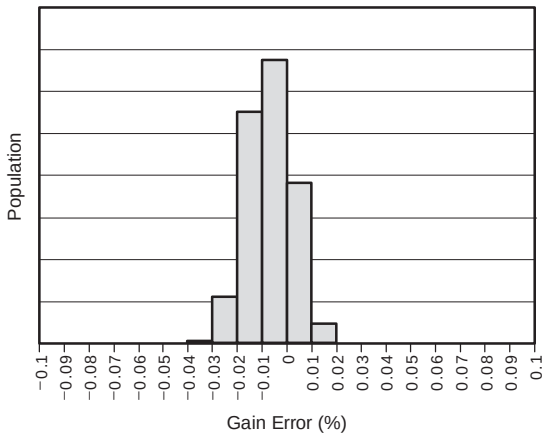
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

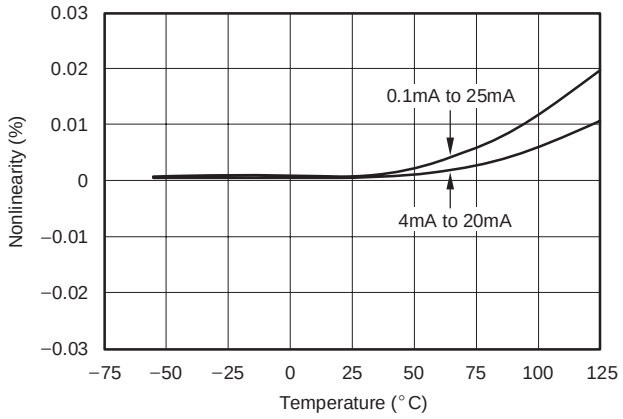
NONLINEARITY DISTRIBUTION



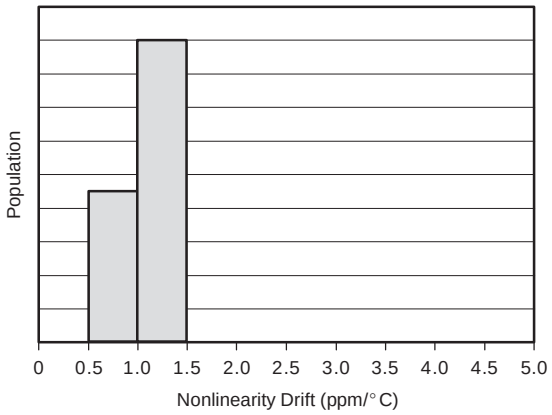
GAIN ERROR DISTRIBUTION



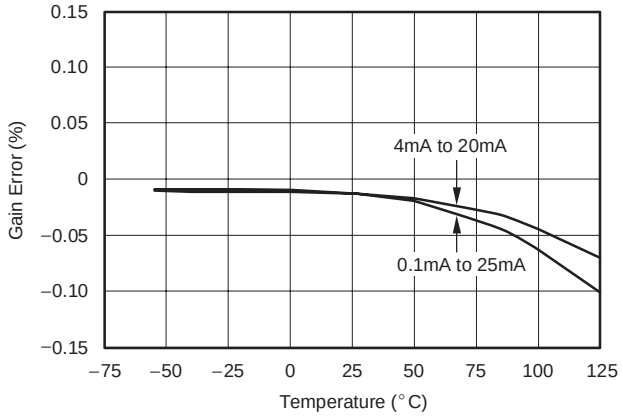
NONLINEARITY vs TEMPERATURE



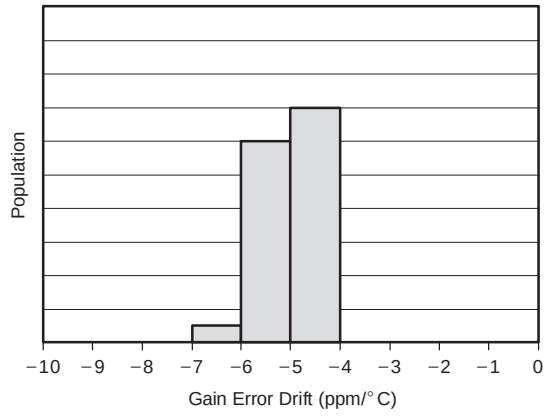
NONLINEARITY DRIFT DISTRIBUTION
(I_{OUT} = 0.1mA to 25mA; T = −55°C to +125°C)



GAIN ERROR vs TEMPERATURE



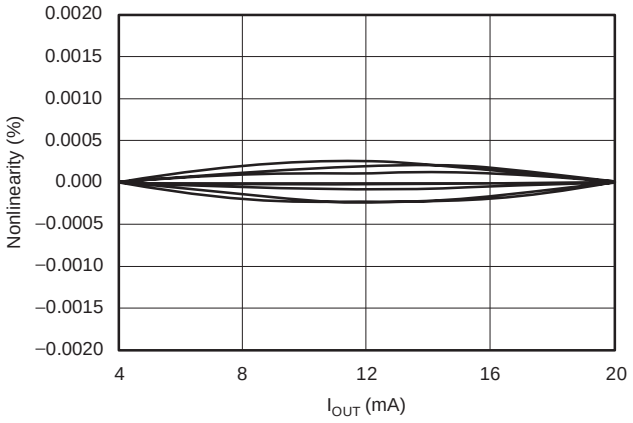
GAIN ERROR DRIFT DISTRIBUTION
(I_{OUT} = 0.1mA to 25mA; T = −55°C to +125°C)



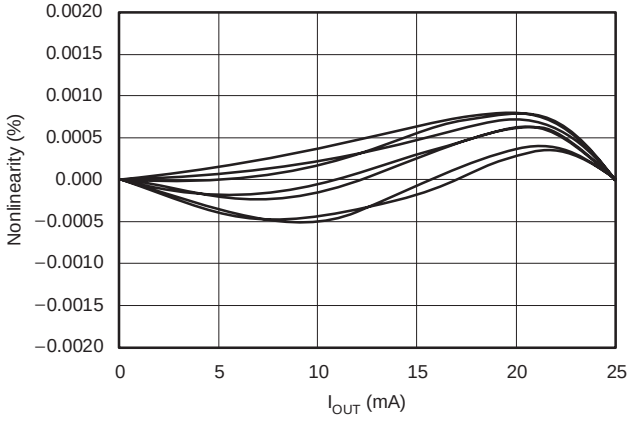
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

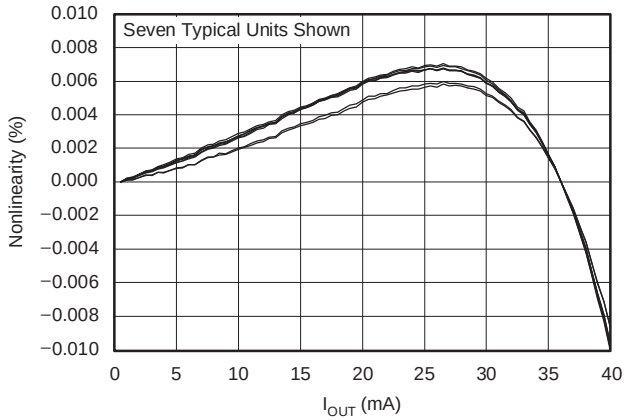
TYPICAL NONLINEARITY
(2pt Calibration at 4mA and 20mA)



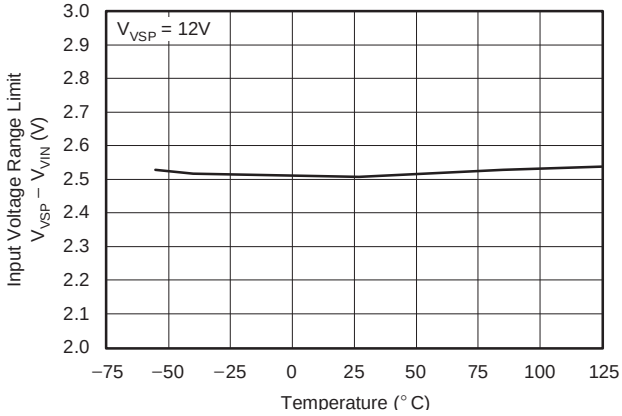
TYPICAL NONLINEARITY
(2pt Calibration at 0.1mA and 25mA)



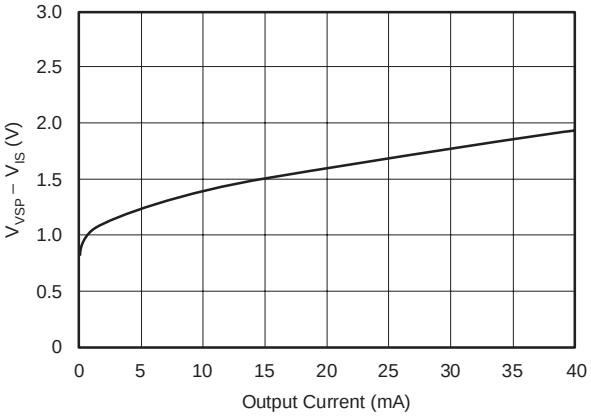
TYPICAL NONLINEARITY
(2pt Calibration at 0.1mA and 36mA)



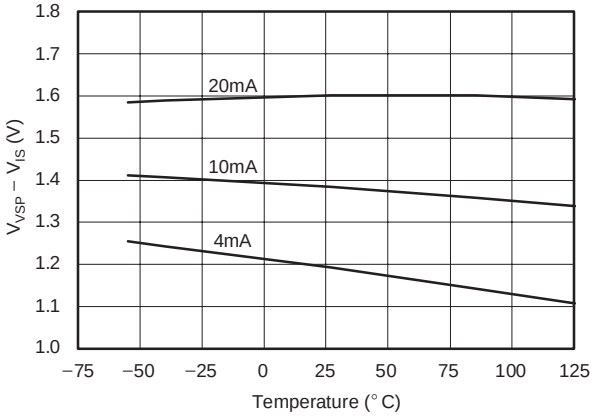
INPUT VOLTAGE RANGE LIMIT TO THE
POSITIVE SUPPLY vs TEMPERATURE



OUTPUT SWING OF THE VOLTAGE ON IS PIN (V_{IS})
vs OUTPUT CURRENT



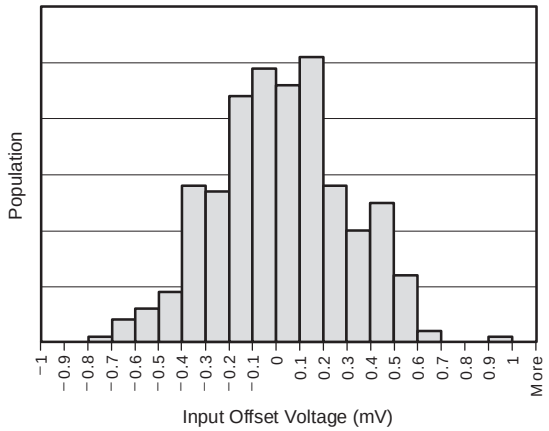
OUTPUT SWING OF THE VOLTAGE ON IS PIN (V_{IS})
vs TEMPERATURE



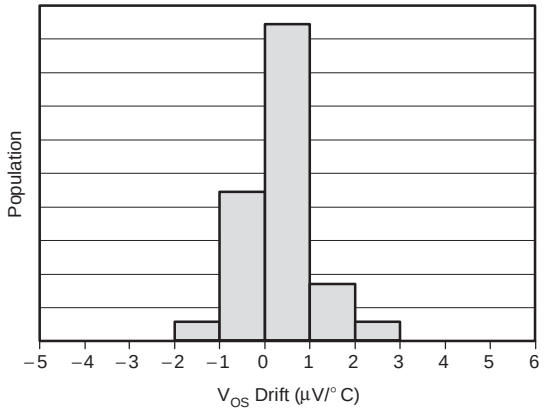
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

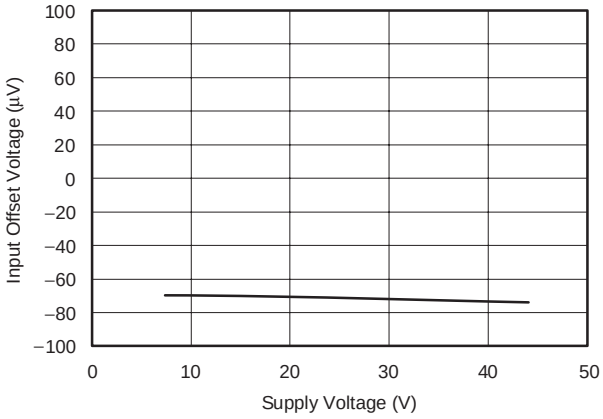
INPUT OFFSET VOLTAGE DISTRIBUTION



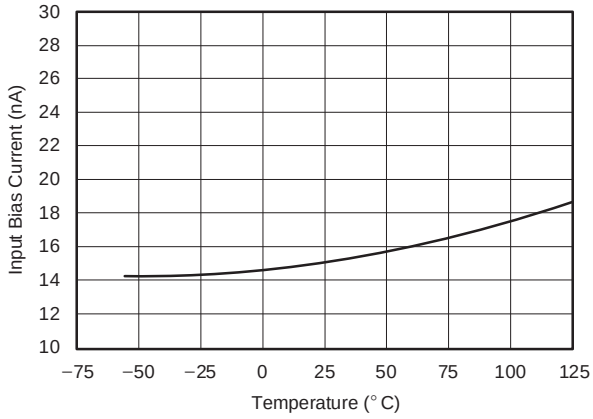
INPUT OFFSET VOLTAGE DRIFT DISTRIBUTION



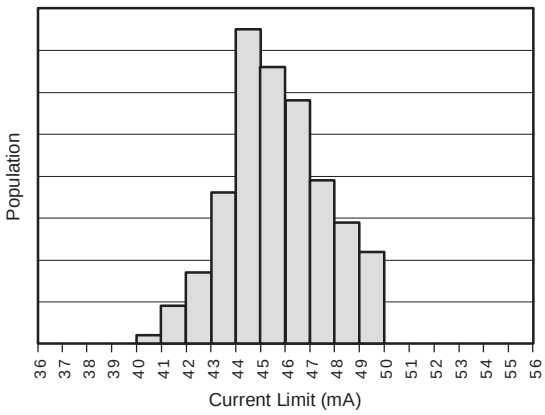
INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



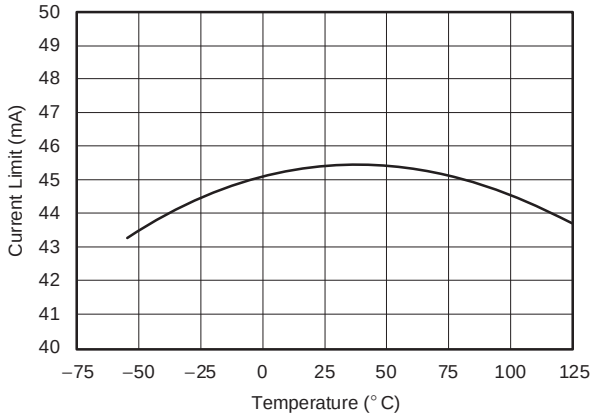
AMPLIFIER INPUT BIAS CURRENT vs TEMPERATURE



OUTPUT CURRENT LIMIT DISTRIBUTION



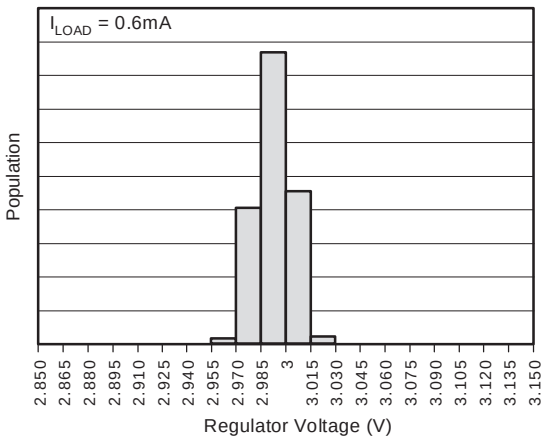
OUTPUT CURRENT LIMIT vs TEMPERATURE



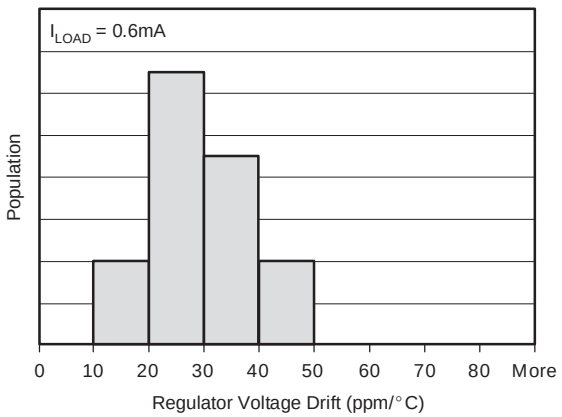
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

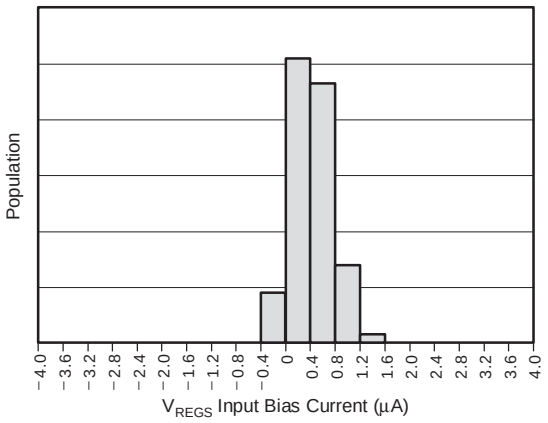
REGULATOR VOLTAGE DISTRIBUTION



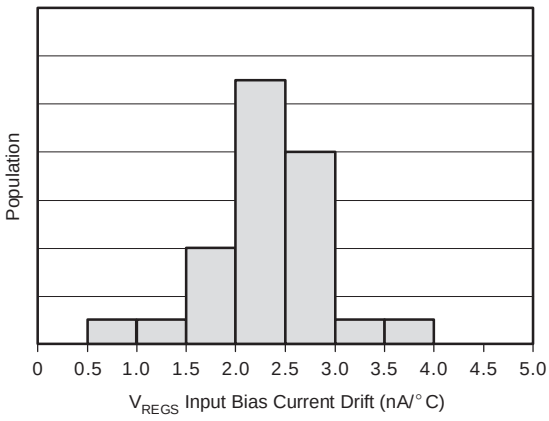
REGULATOR VOLTAGE DRIFT DISTRIBUTION



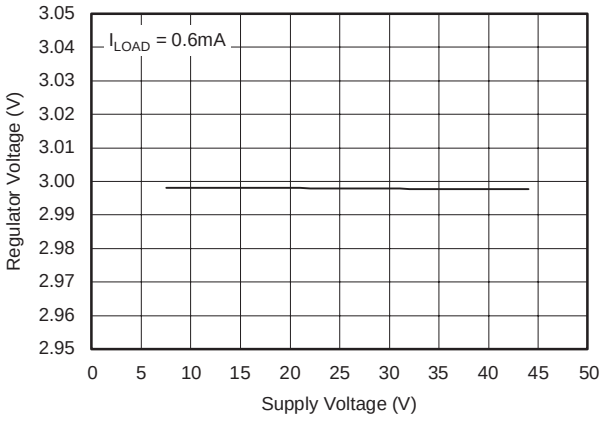
REGULATOR INPUT BIAS CURRENT DISTRIBUTION
(Current into REGS Pin)



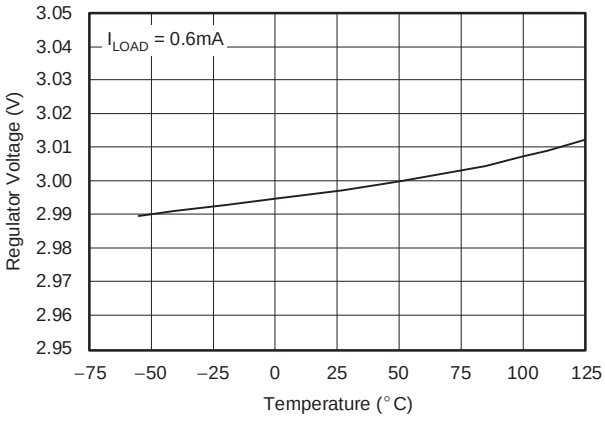
REGULATOR INPUT BIAS CURRENT
DRIFT DISTRIBUTION (Drift of Current into REGS Pin)



REGULATOR VOLTAGE vs SUPPLY VOLTAGE



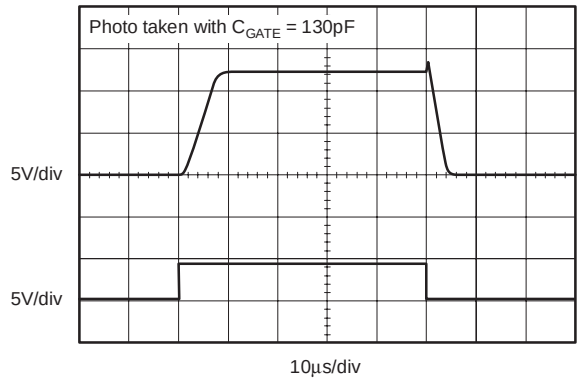
REGULATOR VOLTAGE vs TEMPERATURE



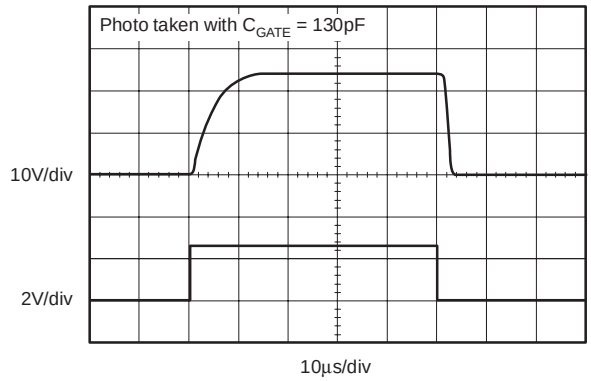
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

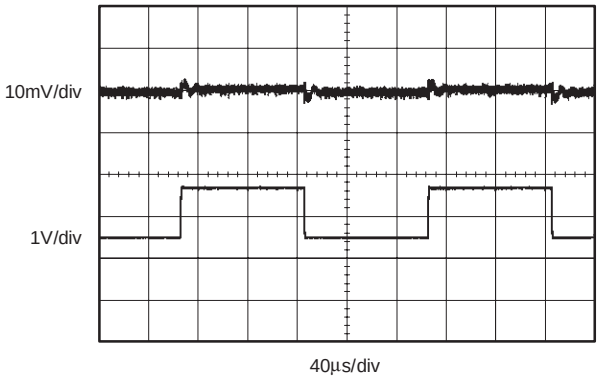
STEP RESPONSE: V_{FS} = 4V, R_{SET} = 2kΩ, R_{LD} = 600Ω
(Rising Edge Depends on C_{GATE} at VG Pin)



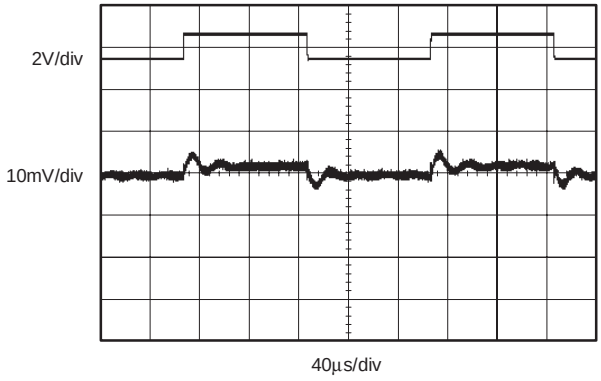
STEP RESPONSE: V_{FS} = 2.5V, R_{SET} = 1.25kΩ, R_{LD} = 600Ω
(Rising Edge Depends on C_{GATE} at VG Pin)



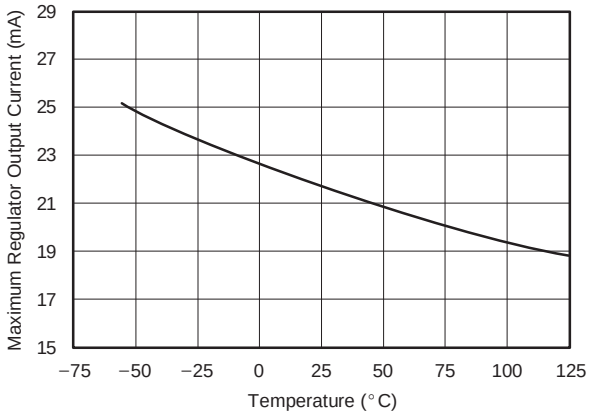
REGULATOR LOAD TRANSIENT
(V_{REG} Gain = 1V, V_{REGF} = 3V, C_L = 470nF
I_{LOAD} = 3mA ±0.3mA)



REGULATOR LOAD TRANSIENT
(V_{REG} Gain = 4V, V_{REGF} = 12V, C_L = 470nF,
I_{LOAD} = 3mA ±0.3mA)



MAXIMUM REGULATOR CURRENT vs TEMPERATURE



APPLICATION INFORMATION

The XTR111 is a voltage-controlled current source capable of delivering currents from 0mA to 36mA. The primary intent of the device is to source the commonly-used industrial current ranges of 0mA−20mA or 4mA−20mA. The performance is specified for a supply voltage of up to 40V. The maximum supply voltage is 44V. The voltage-to-current ratio is defined by an external resistor, R_{SET}; therefore, the input voltage range can be freely set in accordance with the application requirement. The output current is cascoded by an external P-Channel MOSFET transistor for large voltage compliance extending below ground, and for easy power dissipation. This arrangement ensures excellent suppression of typical interference signals from the industrial environment because of the extremely high output impedance and wide voltage compliance.

An error detection circuit activates a logic output (error flag) in case the output current cannot correctly flow. It indicates a wire break, high load resistor, or loss of headroom for the current output to the positive supply.

The output disable (OD) provided can be used during power-on, multiplexing and other conditions where the output should present no current. It has an internal pull-up that causes the XTR111 to come up in output disable mode unless the OD pin is tied low.

The onboard voltage regulator can be adjusted between 3V to 15V and delivers up to 5mA load current. It is intended to supply signal conditioning and sensor excitation in 3-wire sensor systems. Voltages above 3V can be set by a resistive divider.

Figure 1 shows a basic connection for the XTR111. The input voltage V_{VIN} reappears across R_{SET} and controls 1/10 of the output current. The I-Mirror has a precise current gain of 10. This configuration leads to the transfer function:

$$I_{OUT} = 10 \bullet (V_{VIN}/R_{SET})$$

The output of the voltage regulator can be set over the range of 3V to 12V by selecting R_1 and R_2 using the following equation.

$$V_{REGF} = 3V \bullet (R_1 + R_2)/R_2$$

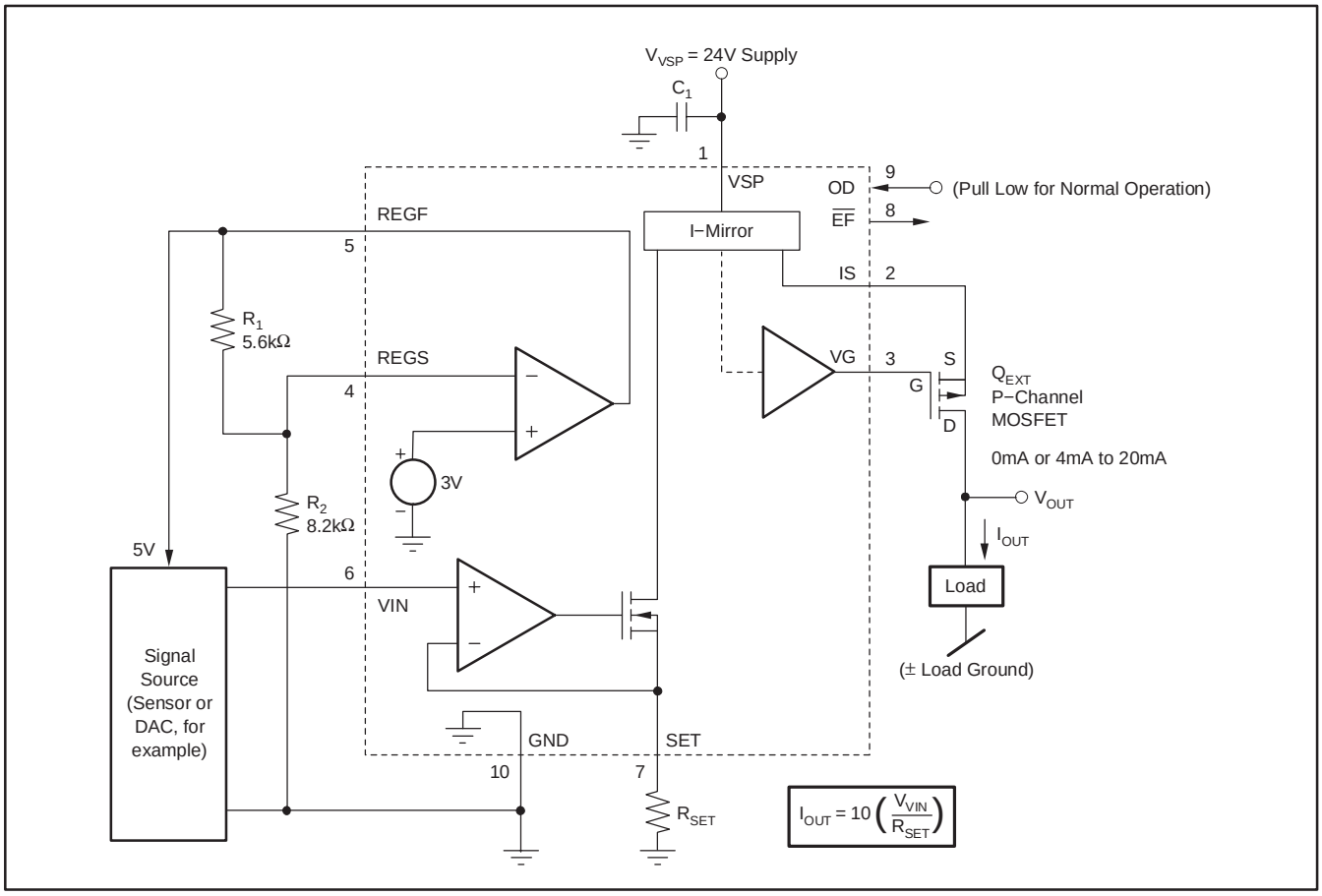


Figure 1. Basic Connection for 0mA to 20mA Related to 0V to 5V Signal Input. The Voltage Regulator is Set to 5V Output.

EXPLANATION OF PIN FUNCTIONS

VIN: This input is a conventional, noninverting, high-impedance input of the internal operational amplifier (OPA). The internal circuitry is protected by clamp diodes to supplies. An additional clamp connected to approximately 18V protects internal circuitry. Place a small resistor in series with the input to limit the current into the protection if voltage can be present without the XTR111 being powered. Consider a resistor value equal to R_{SET} for bias current cancellation.

SET: The total resistance connected between this pin and VIN reference sets the transconductance. Additional series resistance can degrade accuracy and drift. The voltage on this pin must not exceed 14V because this pin is not protected to voltages above this level.

IS: This output pin is connected to the transistor source of the external FET. The accuracy of the output current to IS is achieved by dynamic error correction in the current mirror. This pin should never be pulled more than 6.5V below the positive supply. An internal clamp is provided to protect the circuit, but it must be current-limited externally to less than 25mA.

VG: The gate drive for the external FET is protected against shorts to the supply and GND. The circuit is clamped so that it will not drive more than 18V below the positive supply. The external FET should be protected if its gate could be externally pulled beyond its ratings.

REGF: The output of the regulator buffer can source up to 5mA current, but has very limited (less than 50μA) sinking capability. The maximum short-circuit current is in the range of 15mA to 25mA, changing over temperature.

REGS: This pin is the sense input of the voltage regulator. It is referenced to an internal 3V reference circuit. The input bias current can be up to 2μA. Avoid capacitive loading of REGS that may compromise the loop stability of the voltage regulator.

VSP: The supply voltage of up to a maximum of 44V allows operation in harsh industrial environment and provides headroom for easy protection against over-voltage. Use a large enough bypass capacitor (> 100nF) and eventually a damping inductor or a small resistor (5Ω) to decouple the XTR111 supply from the noise typically found on the 24V supplies.

$\overline{\text{EF}}$: The active low error flag (logic output) is intended for use with an external pull-up to logic-high for reliable operation when this output is used. However, it has a weak internal pull-up to 5V and can be left unconnected if not used.

OD: This control input has a 4μA internal pull-up disabling the output. A pull-down or short to GND is required to activate the output. Controlling OD reduces output glitches during power-on and power-off. This logic input controls the output. If not used, connect to GND.

The regulator is not affected by OD.

EXTERNAL MOSFET

The XTR 111 delivers the precise output current to the IS pin. The voltage at this pin is normally 1.4V below V_{VSP}. It must not fall more than 5.5V below V_{VSP}.

This output requires an external transistor (Q_{EXT}) that forms a cascode for the current output. The resistor must be rated for the maximum possible voltage on V_{OUT} and must dissipate the power generated by the current and the voltage across it.

The gate drive (VG) can drive from close to the positive supply rail to 16V below the positive supply voltage (V_{VSP}). Most modern MOSFETs accept a maximum V_{GS} of 20V. A protection clamp is only required if a large drain gate capacitance can pulse the gate beyond the rating of the MOSFET. Pulling the OD pin high disables the gate driver and closes a switch connecting an internal 3kΩ resistor from the VSP pin to the VG pin. This resistor discharges the gate of the external FET and closes the channel; see Figure 2.

Table 1 lists some example devices in SO-compatible packages, but other devices can be used as well. Avoid external capacitance from IS. This capacitance could be compensated by adding additional capacitance from VG to IS; however, this compensation may slow the output down.

The drain-to-source breakdown voltage should be selected high enough for the application. Surge voltage protection might be required for negative over-voltages. For positive over-voltages, a clamp diode to the 24V supply is recommended, protecting the FET from reversing.

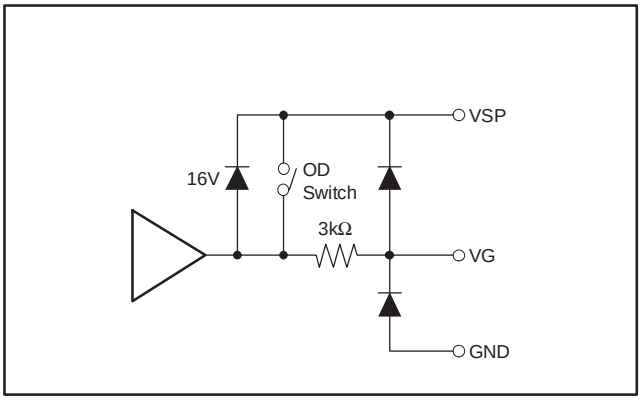


Figure 2. Equivalent Circuit for Gate Drive and Disable Switch

Table 1. P-Channel MOSFET (Examples)(1)

MANUFACTURER	PART NO.	BREAKDOWN VGS	PACKAGE	C-GATE
Infineon	BSP170P	−60V	SOT-223	328pF
International Rectifier	IRFL9014	−60V	SOT-223	270pF
NEC	2SJ326-Z	−60V	Spec.	320pF
ON Semiconductor	NTF2955	−60V	SOT-223	492pF
Supertex Inc.	TP2510	−100V	TO-243AA	80pF

(1) Data from published product data sheet; not ensured.

DYNAMIC PERFORMANCE

The rise time of the output current is dominated by the gate capacitance of the external FET.

The accuracy of the current mirror relies on the dynamic matching of multiple individual current sources. Settling to full resolution may require a complete cycle lasting around 100µs. Figure 3 shows an example of the ripple generated from the individual current source values that average to the specified accuracy over the full cycle.

The output glitch magnitude depends on the mismatch of the internal current sources. It is approximately proportional to the output current level and scales directly with the load resistor value. It will slightly differ from part to part.

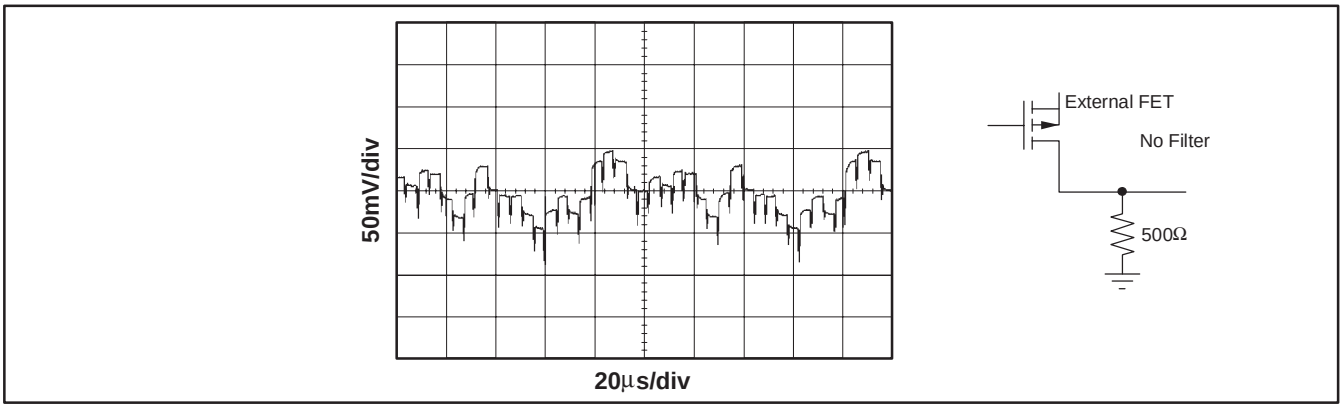


Figure 3. Output Noise without Filter into 500Ω

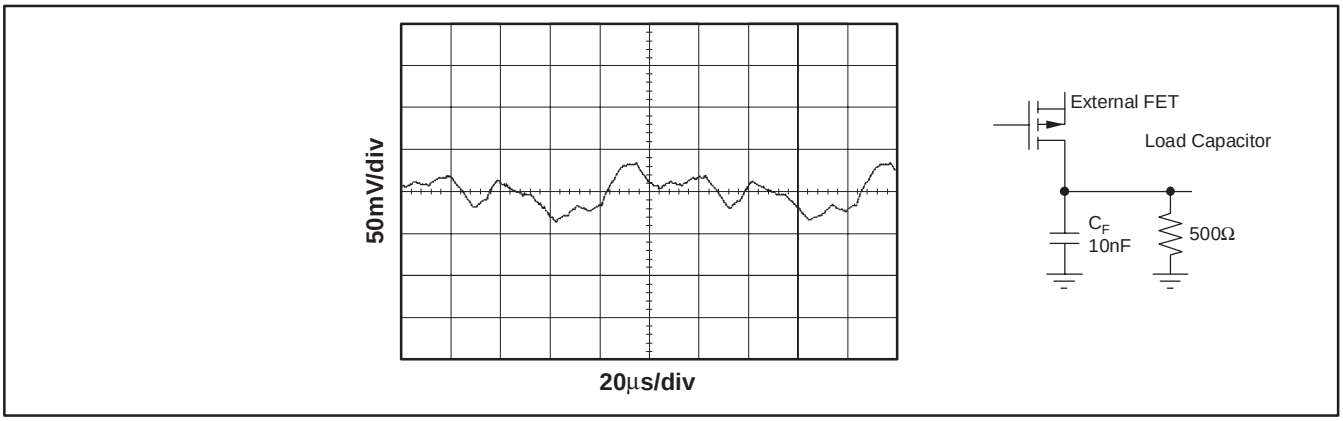


Figure 4. Output with 10nF Parallel to 500Ω

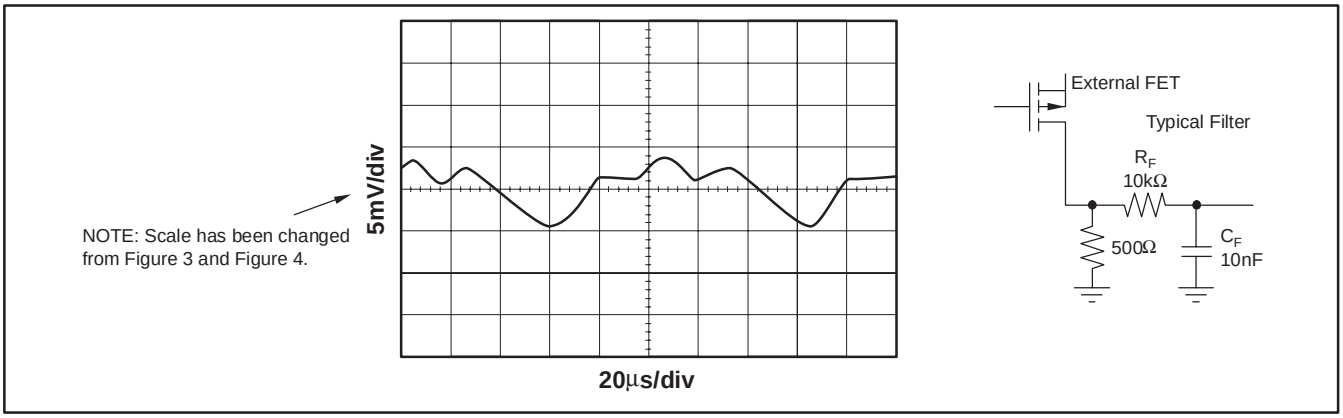


Figure 5. Output with Additional Filter

OUTPUT ERROR FLAG AND DISABLE INPUT

The XTR111 has additional internal circuitry to detect an error in the output current. In case the controlled output current cannot flow due to a wire break, high load resistance or the output voltage level approaching the positive supply, the error flag ($\overline{EF}$), an open drain logic output, pulls low. When used, this digital output requires external pull-up to logic high (the internal pull-up current is 2μA).

The output disable (OD) is a logic input with approximately 4μA of internal pull-up to 5V. The XTR111 comes up with the output disabled until the OD pin is pulled low. Logic high disables the output to zero output current. It can be used for calibration, power-on and power-off glitch reduction and for output multiplexing with other outputs connected to the same terminal pin.

Power-on while the output is disabled (OD = high) cannot fully suppress output glitching. While the supply voltage passes through the range of 3V to 4V, internal circuits turn on. Additional capacitance between pins VG and IS can suppress the glitch. The smallest glitch energy appears with the OD pin left open; for practical use, however, this pin can be driven high through a 10kΩ resistor before the 24V supply is applied, if logic voltage is available earlier. Alternatively, an open drain driver can control this pin using the internal pull-up current. Pull-up to the internal regulator tends to increase the energy because of the delay of the regulator voltage increase, again depending on the supply voltage rise time for the first few volts.

INPUT VOLTAGE

The input voltage range for a given output current span is set by R_{SET} according to the transfer function. Select a precise and low drift resistor for best performance, because resistor drift directly converts into drift of the output current. Careful layout must also minimize any series resistance with R_{SET} and the VIN reference point.

The input voltage is referred to the grounding point of R_{SET}. Therefore, this point should not be distorted from other currents. Assuming a 5V full-scale input signal for a 20mA output current, R_{SET} is 2.5kΩ. A resistance uncertainty of just 2.5Ω already degrades the accuracy to below 0.1%.

The linear input voltage range extends from 0V to 12V, or 2.3V below the positive supply voltage (whichever is smaller). The lowest rated supply voltage accomodates an input voltage range of up to 5V. Potential clipping is not detected by an error signal; therefore, safe design guard banding is recommended.

Do not drive the input negative (referred to GND) more than 300mV. Higher negative voltages turn on the internal protection diodes. Insert a resistor in series with the input if negative signals can occur eventually during power-on or -off or during other transient conditions. Select a resistor value limiting the possible current to 0.3mA. Higher currents are non-destructive (see Absolute Maximum Ratings), but they can produce output current glitches unless in disable mode.

More protection against negative input signals is provided using a standard diode and a 2.2kΩ resistor, as shown in Figure 6.

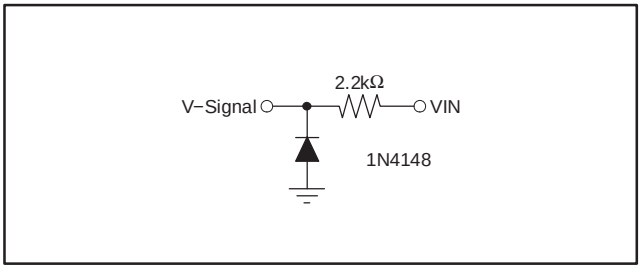


Figure 6. Enhanced Protection Against Negative Overload of V_{IN}

4mA−20mA OUTPUT

The XTR111 does not provide internal circuits to generate 4mA with 0V input signal. The most common way to shift the input signal is a two resistor network connected to a voltage reference and the signal source, as shown in Figure 7. This arrangement allows easy adjustment for over-and under-range. The example assumes a 5V reference (V_{REF}) that equals the full-scale signal voltage and a signal span of 0V to 5V for 4mA to 20mA (I_{MIN} to I_{MAX}) output.

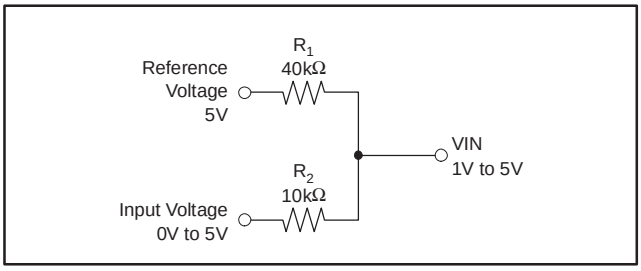


Figure 7. Resistive Divider for I_{MIN} to I_{MAX} Output (4mA to 20mA) with 0 to V_{FS} Signal Source

The voltage regulator output or a more precise reference can be used as V_{REF}. Observe the potential drift added by the drift of the resistors and the voltage reference.

LEVEL SHIFT OF 0V INPUT AND TRANSCONDUCTANCE TRIM

The XTR111 offers low offset voltage error at the input, which normally does not require cancellation. If the signal source cannot deliver 0V in a single-supply circuit, an additional resistor from the SET pin to a positive reference voltage or the regulator output (Figure 8) can shift the zero level for the input (V_{IN}) to a positive voltage. Therefore, the signal source can drive this value within a positive voltage range. The example shows a +100mV (102.04mV) offset generated to the signal input. The larger this offset, however, the more influence of its drift and inaccuracy is seen in the output signal. The voltage at SET should not be larger than 12V for linear operation

Transconductance (the input voltage to output current ratio) is set by R_{SET}. The desired resistor value may be found by choosing a combination of two resistors.

VOLTAGE REGULATOR

The externally adjustable voltage regulator provides up to 5mA of current. It offers drive (REGF) and sense (REGS) to allow external setting of the output voltage as shown in Figure 9. The sense input (REGS) is referenced to 3.0V representing the lowest adjustable voltage level. An external resistor divider sets V_{REGF}.

$V_{REGF} = V_{REGS} \bullet (R_1 + R_2)/R_2$

Table 2 provides example values for the regulator adjustment resistors.

Table 2. Examples for the Resistor Values Setting the Regulator Voltage

V_{REGF}(1)	R_1	R_2
3V	0	—
3.3V	3.3kΩ	33kΩ
5V	5.6kΩ	8.2kΩ
12.4V	27kΩ	8.6kΩ

(1) Values have been rounded.

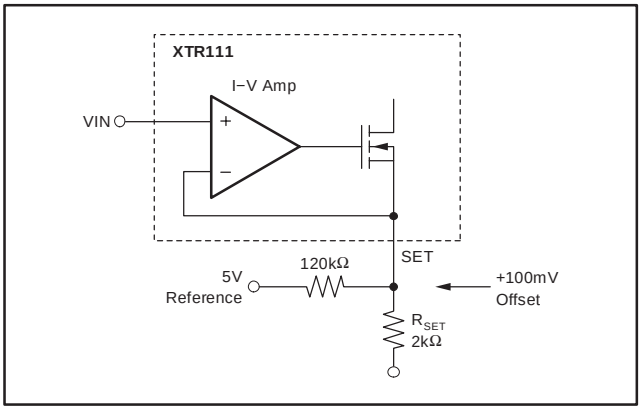


Figure 8. Input Voltage Level Shift for 0mA Output Current

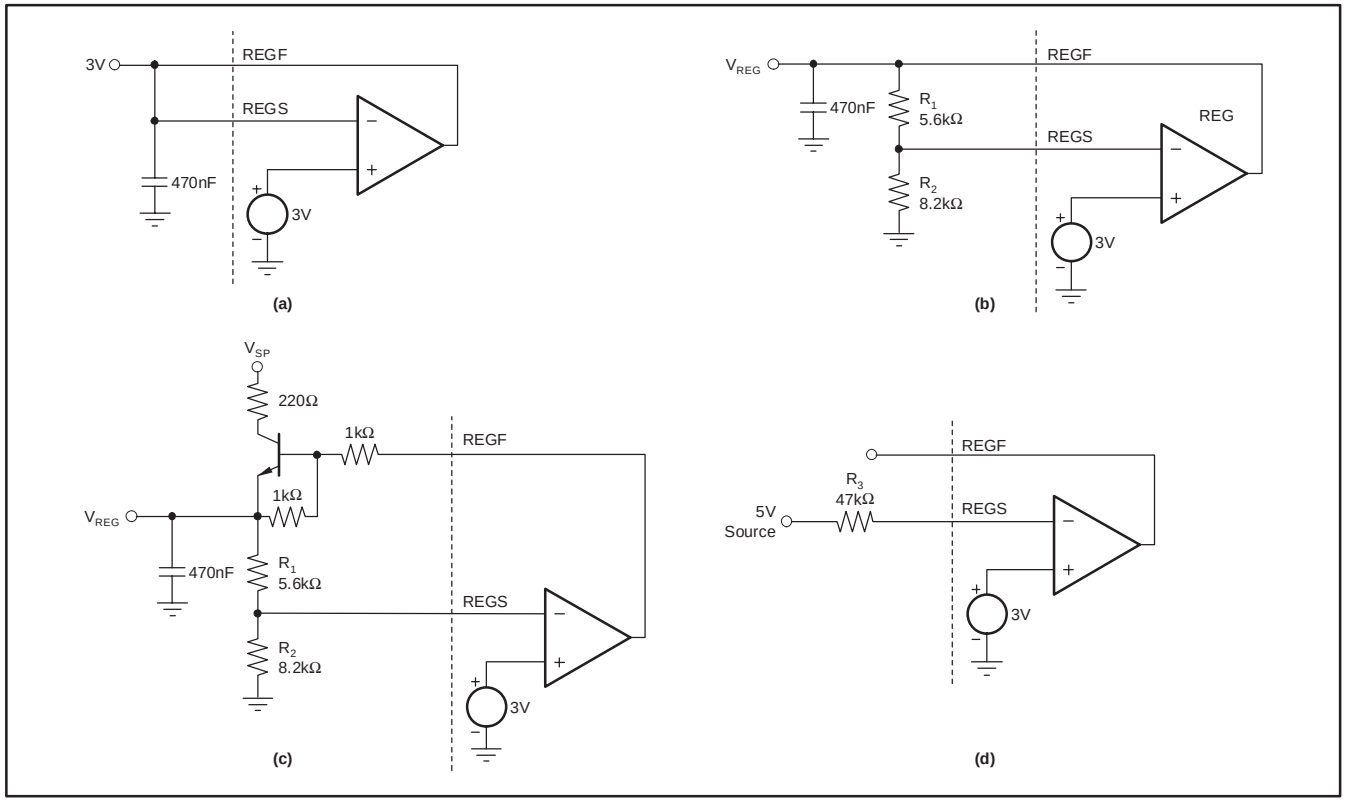


Figure 9. Basic Connections of the Voltage Regulator

The voltage at REGF is limited by the supply voltage. If the supply voltage drops close to the set voltage, the driver output saturates and follows the supply with a voltage drop of less than 1V (depending on load current and temperature).

For good stability and transient response, use a load capacitance of 470nF or larger. The bias current into the sense input (REGS) is typically less than 1µA. This current should be considered when selecting high resistance values for the voltage setting because it lowers the voltage and produces additional temperature dependence.

The REGF output cannot sink current. In case of supply voltage loss, the output is protected against the discharge currents from load capacitors by internal protection diodes; the peak current should not exceed 25mA.

If the voltage regulator output is not used, connect REGF to REGS (the 3V mode) loaded with a 2.2nF capacitor. Alternatively, overdrive the loop pulling REGS high (see Figure 9d).

APPLICATION BLOCK DIAGRAMS

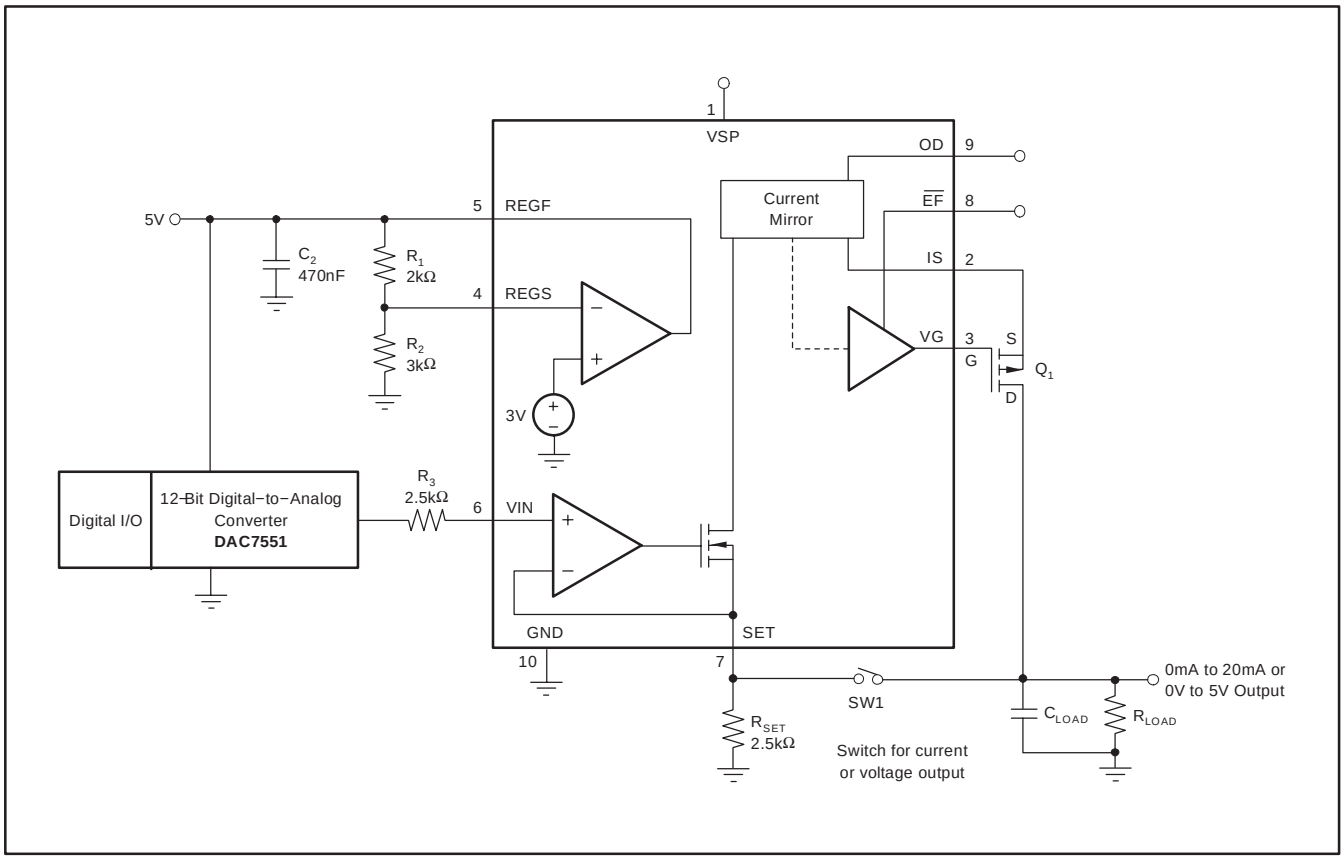


Figure 10. Current or Voltage Output (SW1) Using 0V to 5V Input from a 12-Bit Digital-to-Analog Converter DAC7551

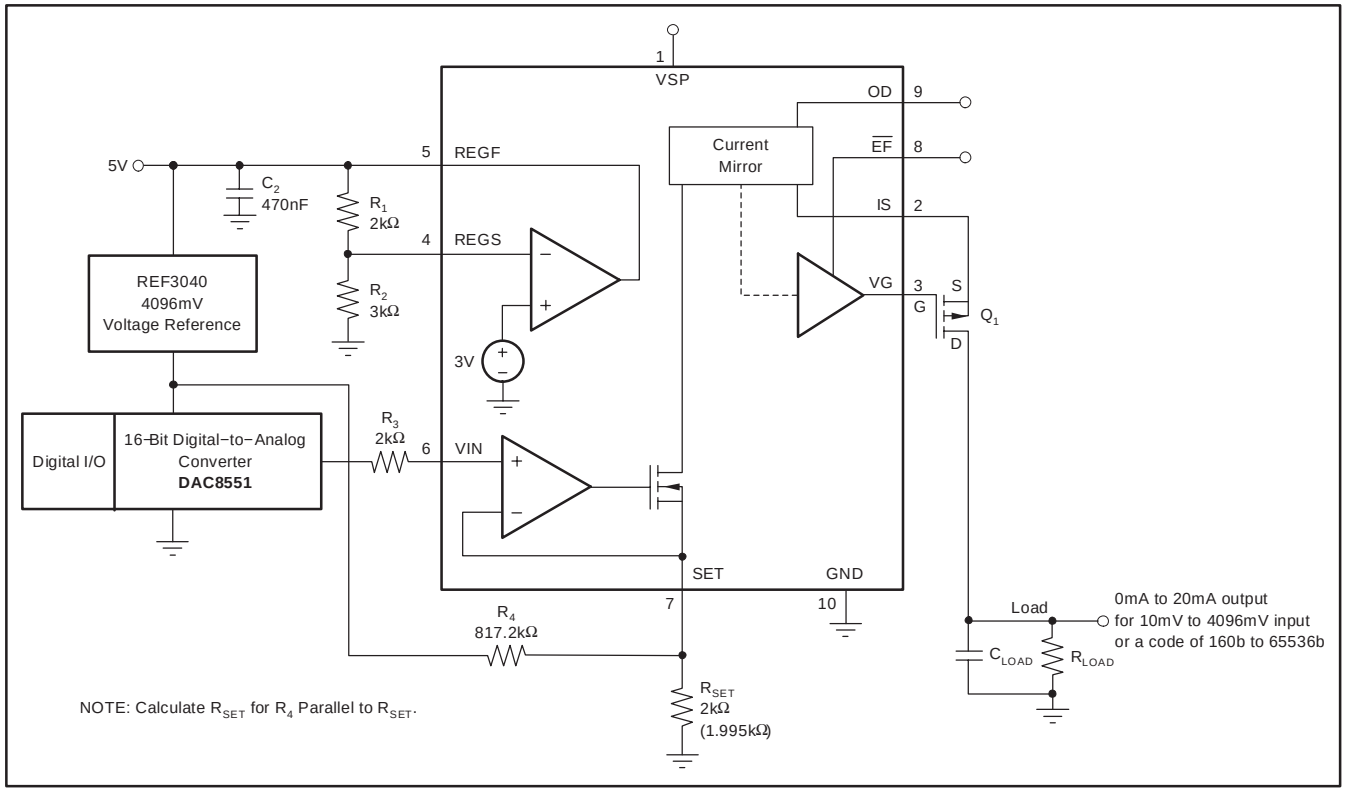


Figure 11. Precision Current Output with Signal from 16-Bit DAC. Input Offset Shifted (R4) by 10mV for Zero Adjustment Range

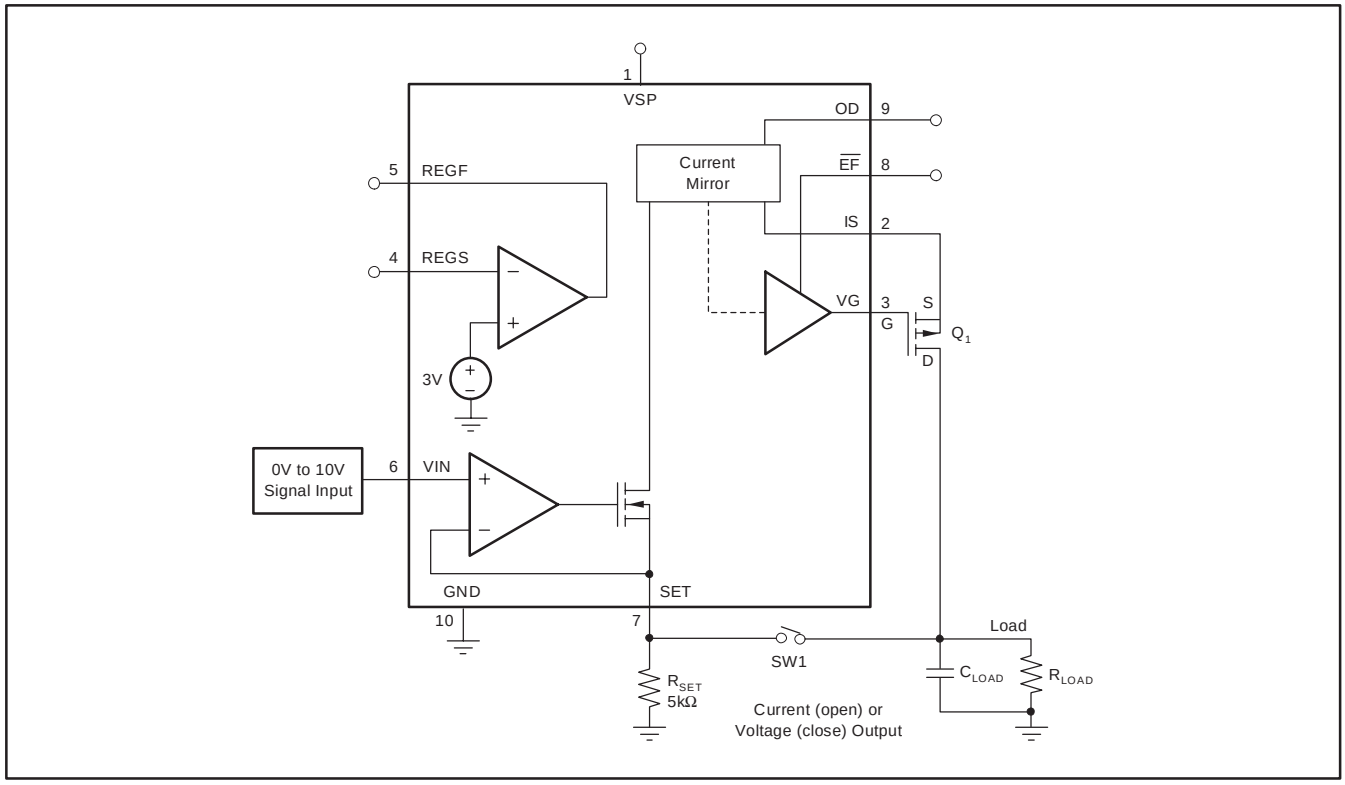
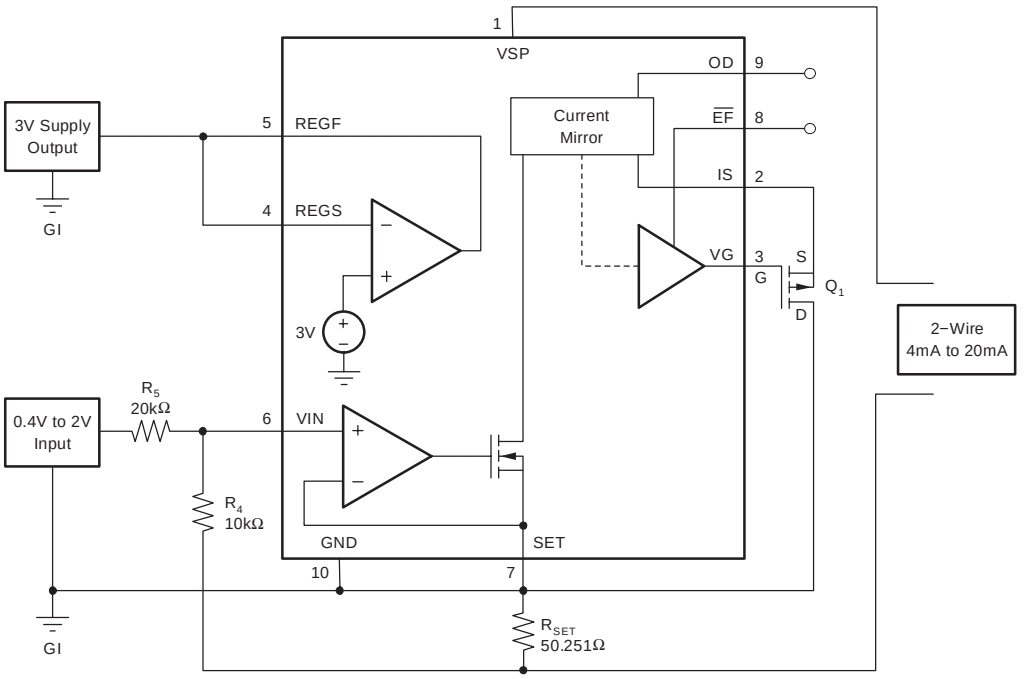
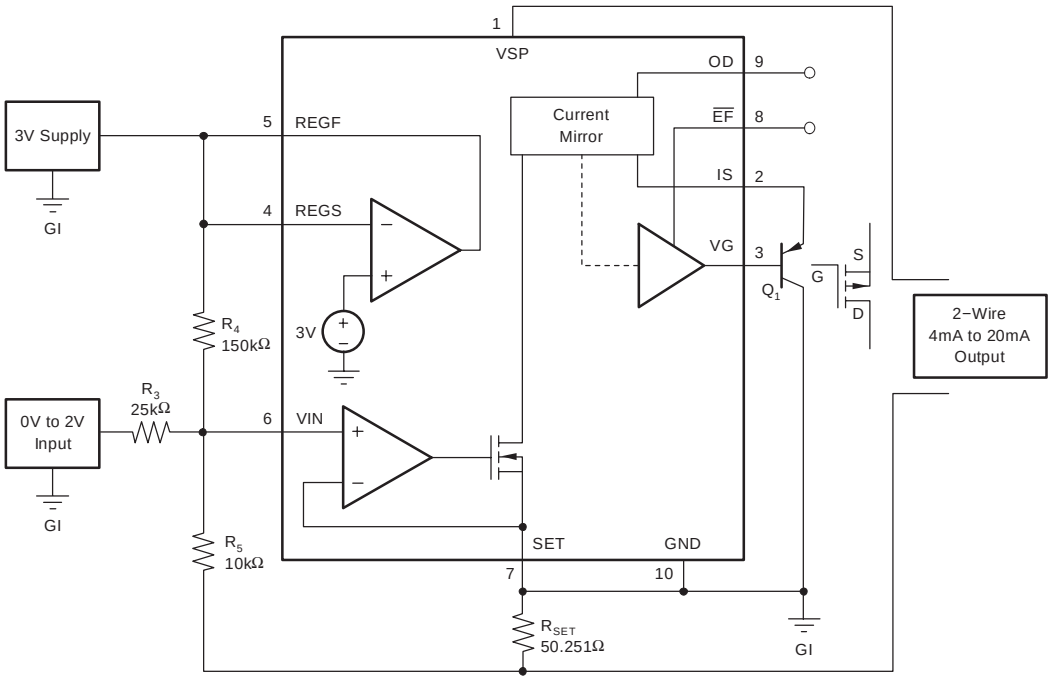


Figure 12. 0V to 10V or 0mA to 20mA Output Selected by Jumper (SW1)



NOTE: The input voltage contains the signal offset: for example 0.4V to 2V input signal. The input signal and supply output are referenced to GND (pin10).

Figure 13. 2-Wire 4mA to 20mA Current Loop Driver with Adjustable Voltage Regulator



NOTE: Input voltage range is set by the four external resistors. Q_1 can be a FET or a PNP transistor. Internal GND reference is GI.

Figure 14. 2-Wire 4mA to 20mA Current Loop Driver for 0V to 2V Signal Input

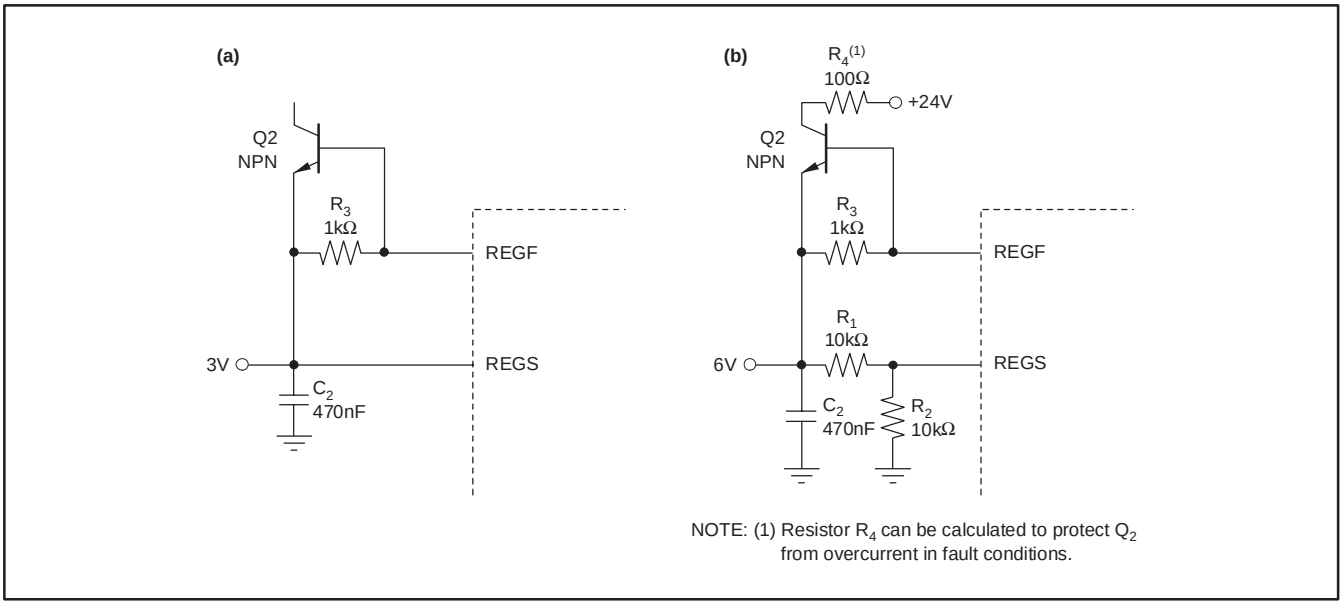


Figure 15. Voltage Regulator Current Boost Using a Standard NPN Transistor

PACKAGE AND HEAT SINKING

The dominant portion of power dissipation for the current output is in the external FET.

The XTR111 only generates heat from the supply voltage with the quiescent current, the internal signal current that is 1/10 of the output current and the current and internal voltage drop of the regulator.

The exposed thermal pad on the bottom of the XTR111 package allows excellent heat dissipation of the device into the printed circuit board (PCB).

THERMAL PAD

The thermal pad must be connected to the same voltage potential as the device GND pin.

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. The thermal resistance from junction-to-ambient (T_{JA}) is specified for the packages with the exposed thermal pad soldered to a normalized PCB, as described in Technical Brief SLMA002, PowerPAD Thermally-Enhanced Package. See also EIA/JEDEC Specifications JESD51-0 to 7, QFN/SON PCB Attachment (SLUA271), and Quad Flatpack No-Lead Logic Packages (SCBA017). These documents are available for download at www.ti.com.

NOTE: All thermal models have an accuracy 20%.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.

LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGING INFORMATION

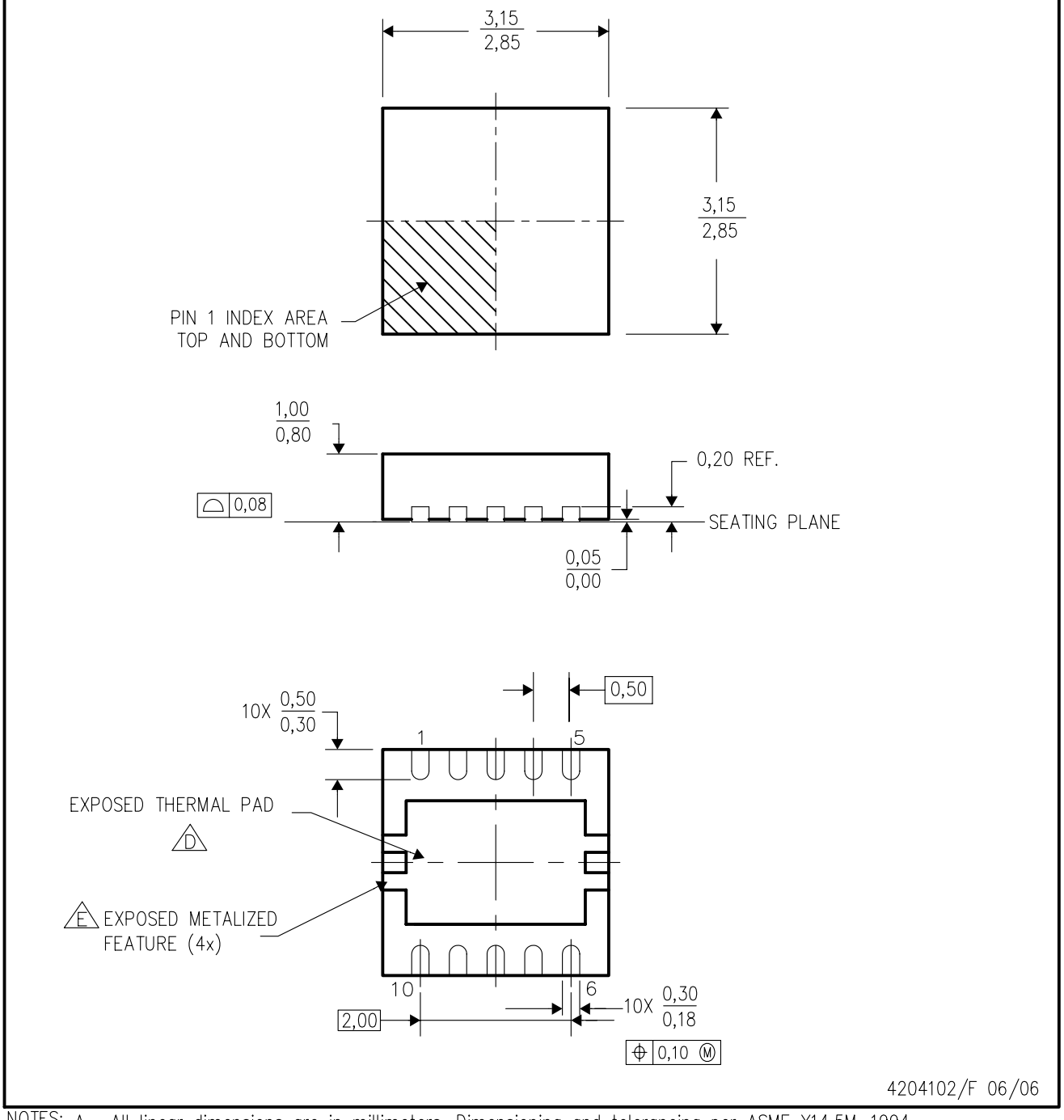
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
XTR111AIDRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
XTR111AIDRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
XTR111AIDRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
XTR111AIDRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

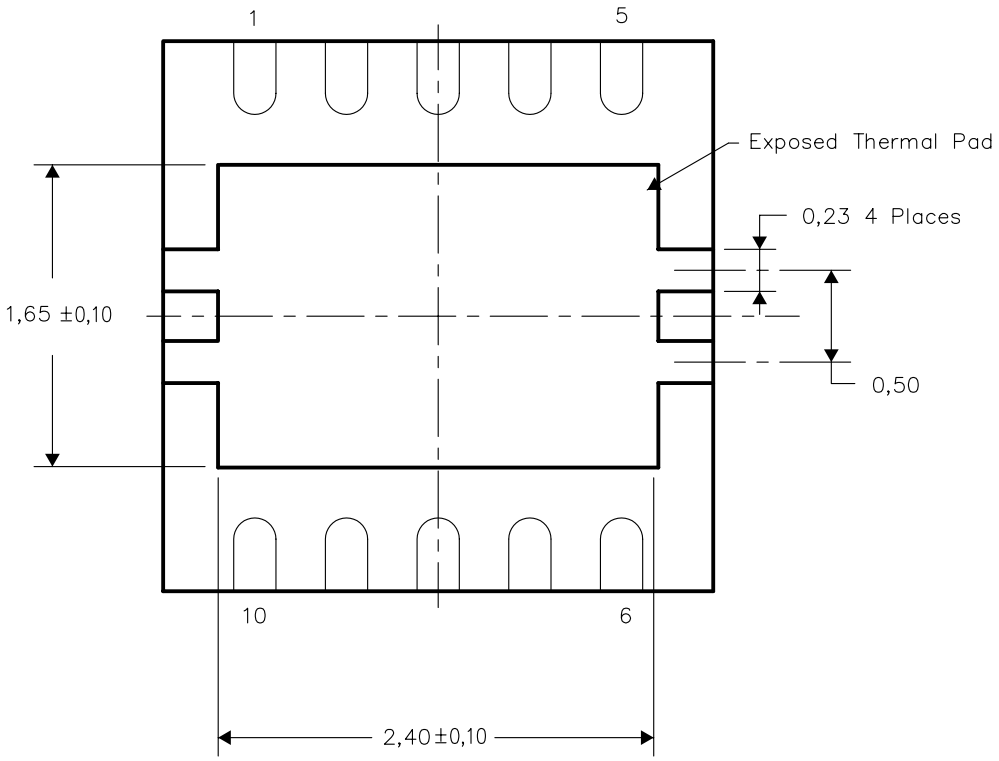
DRC (S–PDSO–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

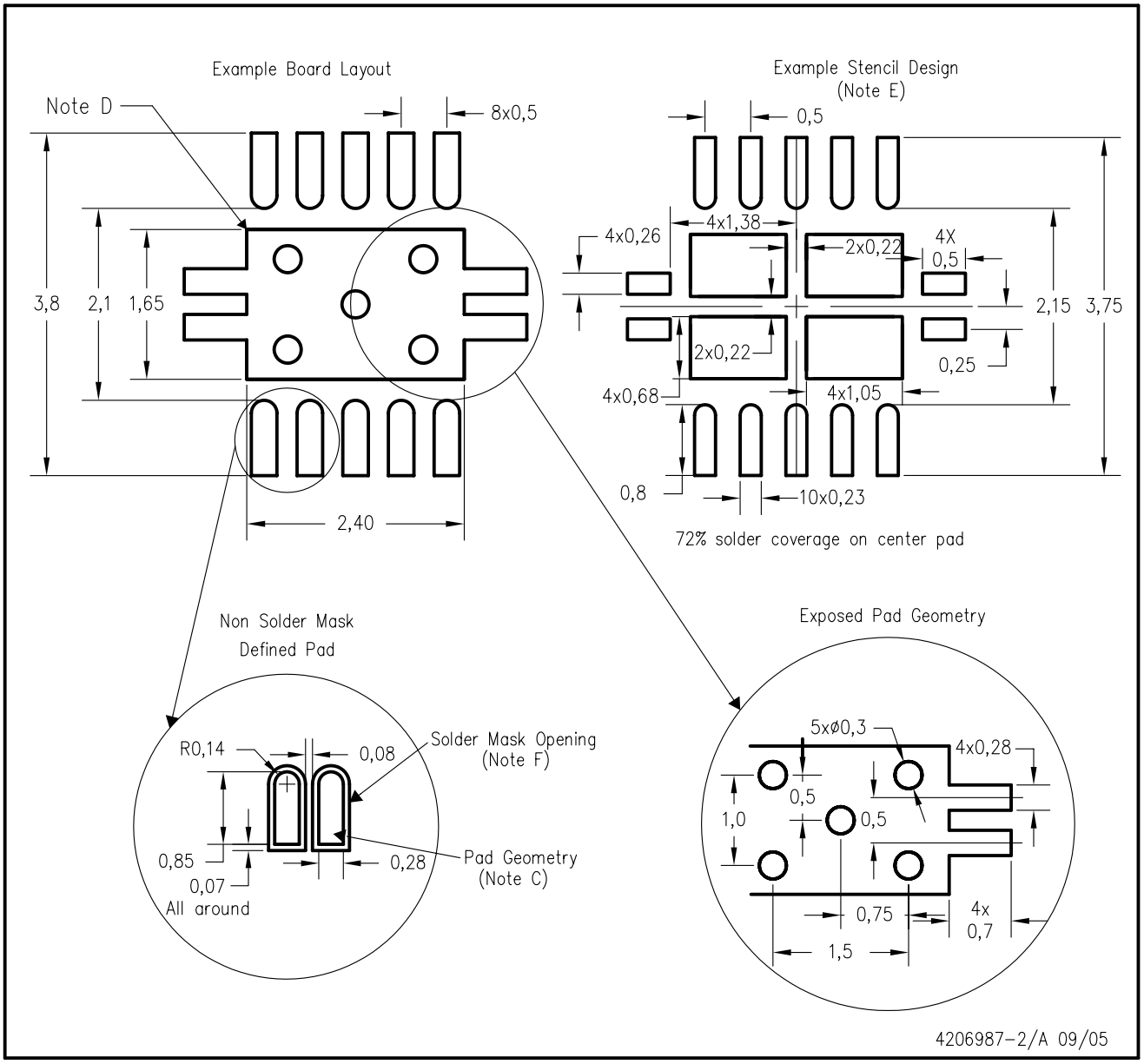


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S–PDSO–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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