W99888 Data Sheet

WINBOND

USB2.0 MULTIMEDIA CONTROLLER

Revision History

REVISION	DATE	DESCRIPTION
1.02	Dec. 8, 2004	Initial Issued
1.03	April 13, 2005	Add Important Notice as Disclaimer Clause

Table of Contents-

1. GENERAL DESCRIPTION

The W99888 is a highly integrated, single chip high-speed USB2.0 compliant digital video imaging controller. Utilizing a high-speed high-bandwidth isochronous pipe, it is able to provide 30 frames per second (FPS) of uncompressed video data at VGA resolution or 15 frames per second (FPS) at XGA resolution. In addition, it provides an 8 bit monaural audio stream that conforms to the USB audio device class specification.

W99888 implements high-speed USB controller complying with USB Spec. Rev. 2.0. It includes six endpoints in which one Control transfer for control data, two isochronous transfers for video and audio data, two programmable bulk transfers for compressed image data or MASS STORAGE data tyransfer and one interrupt transfer for status or event.

W99888 includes a turbo 8032 compatible CPU core, a 12K-byte SRAM and two 16-bit programmable timers. The internal 8032 can be optional to disable and connects with external micro-controller for software development.

W99888 supports a flexible flash memory interface and can directly connect to ATAPI Device, CompactFlash card (CF), NAND type flash and Secure Digital card (SD) or Multi Media card (MMC). It also supports the DMA data transfer between USB_FIFO, USB and flash memory.

2. FEATURES

- **Support Video Interface, Uncompressed video data stream**
  - 1024x768 resolution at up to 15 fps
  - 640x480 resolution at up to 30 fps
  - Software image enhancement filter and sensor control for maximum flexibility
  - Hardware windowing and decimation
  - No external buffer RAM required
- **Support MPEG2 Encoder (W99201) output stream Interface**
- **Support Audio Interface:**
  - Support I2S (Philips UDA1345TS Audio codec)
- **Support USB 2.0 Interface:**
  - Complies with Universal Serial Bus specification rev. 2.0.
  - Transfer Rate for USB Interface: “High speed” Up to 480 Mbits/sec
  - Supports 6 Endpoints:
    - Control (EP0).
    - Bulk In (EP1).
    - Bulk Out (EP2).
    - Interrupt In (EP3).
    - Isochronous In (EP4, EP5).

- Embedded USB 2.0 UTMI transceiver.
- USB2.0 Isochronous video pipe can transfer up to 24MB/sec.
- USB2.0 Isochronous audio pipe can transfer up to 8kB/sec.

■ **Support ATA Interface Device Mode**
- Complies with ATA-2 specification rev 4c.
- Support the True IDE Standards.
- Data transfer rate = 16.6Mbytes/sec (PIO4 data transfer).
- 5V tolerance pad for IDE interface.

■ **Support ATAPI 6.0 Interface Host Mode**
- Complies with ATA/ATAPI-6 specification rev 3b.
- 5V tolerance pad for IDE interface.

■ **Support Mass Storage Card Interface:**
- Type I/II CompactFlash Card (CF) / IBM MicroDrive (MD)
  - Fully compatible with CompactFlash Specification Version 2.0
- NAND Flash Interface:
  - Support capacity 8/16/32/64/128M Bytes for Samsung/Toshiba “Flash Memory”
  - Support capacity 32/64/128/256M Bytes for Samsung “Advance Flash Memory”

  Note: This interface don’t support the VCC=1.8V Advance Flash Memory
- Build-in standard hardware ECC circuit
- Support 4 NAND Flash chips
- Secure Digital/ Multi Media Card Interface
  - Complies with Secure Digital Version 1.0 / MMC interface specification Version 3.3.
  - Supports different clock rate from 375 KHz to 20 MHz.

■ **Support External Turbo 8051 ICE Interface:**
- Compatible with Winbond W77E516 controller
- Support External Turbo ICE mode for customer development

■ **Support 8051 UART Interface from P3.0 and P3.1**

■ **Support External EEPROM of W39L512 ISP Function (In System Programming)**

■ **Support SPI Master and Slave Modes Controller**

■ **Internal RAM/Buffer Interface:**
- Internal RAM size: 12K Bytes (0xC000 ~ 0xEFFF) for “MOVX RAM”

  Note: 12KB RAM include Internal USB FIFO size

- USB FIFO definetion
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
  - Bi-directional 512/2K Byte Buffer for Bulk Endpoint
  - 8 Bytes Interrupt In
  - 1K Bytes Isochronous In X 2.

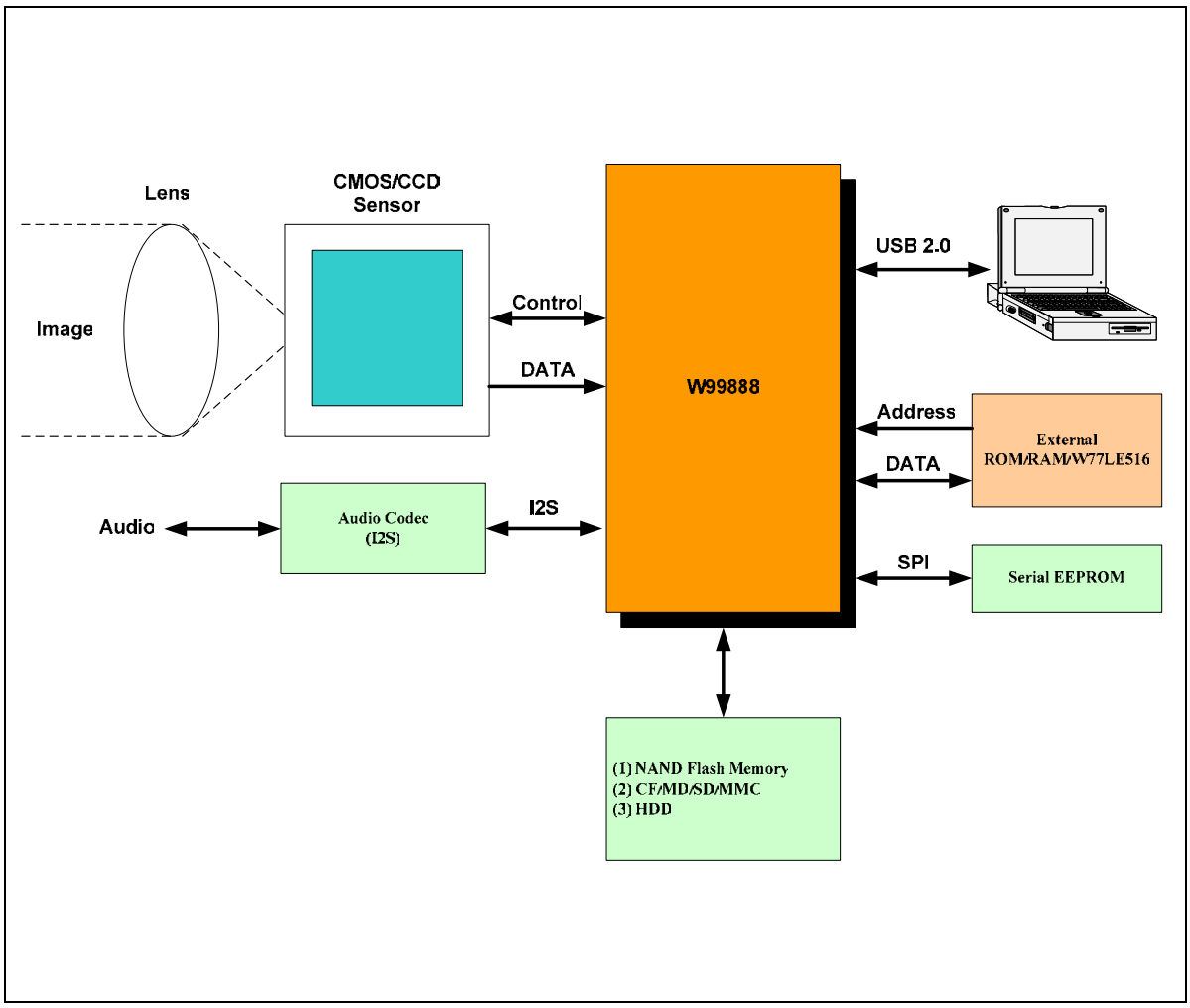
- **Support Five sets 8 Bits General Purpose I/O**
  - AGPIO0[7:0]
  - AGPIO1[7:0]
  - AGPIO2[7:0]
  - uP8051_Port1[7:0]
  - uP8051_Port2[7:0]

- **5V tolerant inputs, 3.3V output drive**
- **Crystal clock synthesis from 48MHz**
- **Available package in**
  - 128-pin LQFP (14 mm * 14mm)
  - 111 Ball TFBGA (8 mm * 8mm)

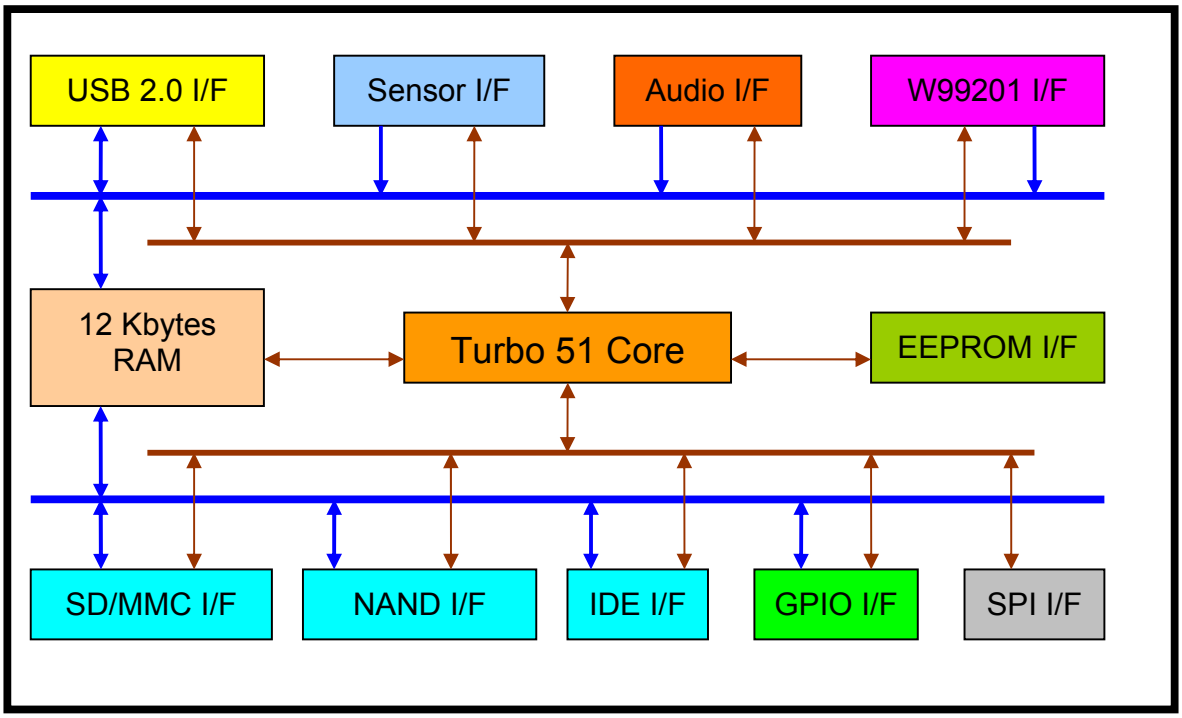
Typical Applications:

- MP3 Player
- PDA, Camera, Mobile Phone MP3
- Home Audio/Multimedia MP3
- USB2.0 Portable Device, Portable USB2.0 HDD
- USB 2.0 Card Reader (CF/MD/SD/MMC)
- USB2.0 Pen-Drive
- Non-Compress USB 2.0 PC Camera

3. SYSTEM OVERVIEW



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT AND DESCRIPTION

Ipu: Input with pull-up
O: Output
O/Z: Output / High impedance
I/O: Input / Output
PWR: Power
#: Low Active

USB Control Interface

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
USB_DP	A7	77	I/O	USB D+ Line
USB_DM	A9	75	I/O	USB D- Line
VDDA33T x 2	C7, C8	73, 79	PWR	USB Transceiver Power Pin
VSSA33T x 3	A6, A8, A10, B7, B8, B9	74, 76, 78	PWR	USB Transceiver Ground Pin
VDDA33C	D9	71	PWR	USB Common Power Pin
VSSA33C	C10	70	PWR	USB Common Ground Pin
REXT	D8	72	I	Reference resister connect
XTALI	B10	68	I	48MHz crystal input
XTALO	C9	69	O	48MHz crystal output
USB_Test	E7	67	I	Test Pin
USB_VBUS	B6	81	I	USB cable power pin, it should be connected to 100K pull down resistor.

ICE Interface

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
uP_ALE	J6	18	I	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/4th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
uP_PSEN#	H6	17	I	PROGRAM STORE ENABLE: uP_PSEN# enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no uP_PSEN# strobe signal outputs originate from this pin.

ICE Interface, continued

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
uP_RD#	L10	35	I	Input with internal pull-ups. It is also used for 8051 microprocessor External Data Memory Read Strobe.
uP_WR#	L9	29	I	Input with internal pull-ups. It is also used for 8051 microprocessor External Data Memory Write Strobe.
uP_INT0	C11	60	O	uP Interrupt of INT0, If ICEMode_En# pin Enable
uP_INT1	B11	61	O	uP Interrupt of INT1, If ICEMode_En# pin Enable
uP_D0[7:0]	H7, J7, K7, L7, J8, K8, L8, K9	21, 22, 23, 24, 25, 26, 27, 28	I/O	This port also provides a multiplexed low order address/data bus during the External Data Memory access.
uP_AH[7:0]	E11, E10, E9, E8, F11, F10, G9, G10	57, 56, 55, 54, 53, 52, 51, 46	I	This port also provides a multiplexed high order address bus during the External Data Memory access
ICEMode_En#	E6	82	Ipu	ICE Mode Select, “H” ICE mode disable.
ICEClk_Out	D11	58	O	ICE Clock Output

External RAM, ROM Interface: (ICEMode_En# = H)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
uP_PSEN#	H6	17	O	In this mode, As External ROM Read Pin.
uP_RD#	L10	35	O	In this mode, As External RAM Read Pin.
uP_WR#	L9	29	O	In this mode, As External RAM Write Pin.
uP_INT0	C11	60	O	In this mode, As External ROM chip selcet Pin.
uP_INT1	B11	61	O	In this mode, As External ROM Write Pin.
uP_D0[7:0]	H7, J7, K7, L7, J8, K8, L8, K9	21, 22, 23, 24, 25, 26, 27, 28	I/O	This port also provides a multiplexed low order address/data bus during the External Data Memory access.
uP_AH[7:0]	E11, E10, E9, E8, F11, F10, G9, G10	57, 56, 55, 54, 53, 52, 51, 46	O	This port also provides a high order address bus during the External Data Memory access
uP_AL[7:0]	G11, H10, H11, J9, J10, J11, K10, K11	45, 44, 41, 40, 39, 38, 37, 36	O	This port also provides a low order address bus during the External Data Memory access

Note: External RAM address is 0x0000~0xBFFF

Power Interface

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
VDDIO_33 x 4	F9, C4, K6, G4	19, 50, 89, 116	PWR	Digital Power
VSSIO_33 x 4	F8, B4, L6, G3	20, 49, 90, 117	PWR	Digital Ground
VDDCORE_18 x 2	H8, E4	43, 110	PWR	CPU core Power
VSSCORE_18 x 2	H9, E3	42, 109	PWR	CPU core Ground
USBVDD_18	G7	48	PWR	USB core Power
USBVSS_18	G8	47	PWR	USB core Power
PLLVDD_18	K2	6	PWR	PLL circuit Power
PLLVSS_18	J3	7	PWR	PLL circuit Power

Other Interface

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SYS_RST	D10	59	I	Controller Reset Pin
TEST0	D7	80	I	Chip Test Pin
TEST1	K4	10	I	Chip Test Pin
TEST2	J4	11	I	Chip Test Pin

UART Signal Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
uP_P3RxT[0]	H5	16	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Serial Port Input.
uP_P3RxT[1]	J5	15	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Serial Port Output.

SPI Control Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SPI_MISO	K3	8	I/O	MASTER IN, SLAVE OUT The MISO line is defined as an input line into the master device and as an output in a slave device. The MISO line transfers data in the opposite direction to the MOSI line, it transfers data from a slave device to the master.

SPI Control Interface: (ICEMode_En# = don't care), continued

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SPI_MOSI	L3	5	I/O	MASTER OUT, SLAVE IN The MOSI line is defined as an output line from the master device to an input into the slave devices. The MOSI line transfers data in one direction only, from the master to a slave.
SPI_SCLK	L2	4	O	SERIAL CLOCK The SCLK line is used to synchronize both data in and out of a device via the MOSI and MISO lines. The SCLK line is generated by the master device and thus is an input into all slave devices.
SPI_SS#	K1	125	I	SLAVE SELECT The Slave Select (SS) lines are controlled by the master to select a slave device. The SS line must be low prior to data transactions and must stay low for the duration of the transaction. Each slave device requires its own SS input line from the master.
SPI_CS0#	J1	124	O	Serial Chip Select0
SPI_CS1#	H2	121	O	Serial Chip Select1
SPI_CS2#	H1	122	O	Serial Chip Select2
SPI_CS3#	J2	123	O	Serial Chip Select3

8051 I/O Interface (ICEMode_En# = High)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
uP_P1[7:0]	J1, J2, H1, H2, H3, G1, G2, F1	124, 123, 122, 121, 120, 119, 118, 115	I/O	General Purpose I/O compatible 8051 Port1
uP_P2[7:0]	K5, L5, H4, L4, K3, L3, L2, K1	14, 13, 12, 9, 8, 5, 4, 125	I/O	General Purpose I/O compatible 8051 Port2

PS: The Port1 and Port2 does not emulate by ICE mode.

AGPIO Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
AGPIO0[7:0]	B3, A4, A5, B5, C5, D5, C6, D6	92, 91, 88, 87, 86, 85, 84, 83	I/O	Alternate General Purpose I/O0
AGPIO1[7:0]	D1, C3, C2, C1, B2, B1, A2, A3	104, 103, 102, 101, 100, 99, 94, 93	I/O	Alternate General Purpose I/O1
AGPIO2[7:0]	F2, F3, F4, E2, E1, D4, D3, D2	114, 113, 112, 111, 108, 107, 106, 105	I/O	Alternate General Purpose I/O2

USB2.0 Card Reader Controller

Compact Flash Card (Host) Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
ATA(CF)_DAT[15:0]	D1, C3, C2, C1, B2, B1, A2, A3, J1, J2, H1, H2, H3, G1,G2, F1	104, 103, 102, 101, 100, 99, 94, 93, 92, 91, 88, 87, 86, 85, 84, 83	I/O	CF Data Bus
ATA(CF)_ADDR[2:0]	D4, D3, D2	107, 106, 105	O	CF Address Bus
ATA(CF)_IOR#	E2	111	O/Z	CF Device Read Strobe Signal
ATA(CF)_IOW#	E1	108	O/Z	CF Device Write Strobe Signal
ATA(CF)_IORDY	F1	115	I	CF Ready
ATA(CF)_CS0#	H3	120	O/Z	CF Chip Select 0
ATA(CF)_CS1#	G1	109	O/Z	CF Chip Select 1
ATA(CF)_RST#	F4	112	O/Z	CF Reset
CF_CD1#	L4	9	Ipu	CF detected Pin 1
CF_CD2#	H4	12	Ipu	CF detected Pin 2

NAND Flash Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SM_IO[7:0]	B3, A4, A5, B5, C5, D5, C6, D6	92, 91, 88, 87, 86, 85, 84, 83	I/O	SM Card Data Bus/Advance NAND Flash Low Byte Data Bus
SM_IO[15:8]	D1, C3, C2, C1, B2, B1, A2, A3	104, 103, 102, 101, 100, 99, 94, 93	I/O	Advance NAND Flash High Byte Data Bus
SM_CLE	D2	105	O	SM Card/NAND Flash Command Latch Enable

NAND Flash Interface: (ICEMode_En# = don't care), continued

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SM_ALE	G1	119	O	SM Card/NAND Flash Address Latch Enable
SM_CE[3:0]#	K5, H3, J2, D4	14, 120, 118, 107	O/Z	SM Card/NAND Flash Chip Enable
SM_RE#	E2	111	O/Z	SM Card/NAND Flash Read Enable
SM_WE#	E1	108	O/Z	SM Card/NAND Flash Write Enable
SM_WP#	D3	106	Ipu	SM Card/NAND Flash Write Protect
SM_RBY#	F1	115	I	SM Card/NAND Flash Ready/Busy

Note1: SM_D[15:8] are used for SAMSUANG "K9F1G16U0M-Y, K9K2G16U0M-Y…" Advance NAND Flash.
Note2: These interface does'nt support the "SM Media Card".

Secure Digital Card Interface (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SD_CLK	H4	12	O	Serial Clock
SD_CMD	L5	13	O	Command Line
SD_WP#	F4	112	I	Card Write Protected Pin
SD_CD#	F3	113	I	Card Detected Pin
SD_PWR_CTRL#	F2	114	O	Power Control
SD_DAT[3:0]	J2, H1, H2, L4	123, 122, 121, 9	I/O	Data I/O

USB2.0 Audio/Non-Compress Video Bridge Controller

Audio Codec Interface: (ICEMode_En# = don't care)

PIN NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
ADO	D6	83	O	Data output to Audio Codec
ABCLK	C6	84	I/O	Bit clock, Input at AC97, output at I2S
ACodec_clk	D5	85	O	Clock output to Audio Codec when I2S
ADI	C5	86	I	Audio Codec data input
AWS	B5	87	O	Word select at I2S, or SYNC at AC97
ARST#	A5	88	O	AC97 Audio Codec reset

Video Sensor Interface: (ICEMode_En# = don't care)

PIN NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
PCLK	D2	105	I	Clock for Sensor or Video Data Input (Programmable polarity)
SCLK	D3	106	O	Video Master Clock
VS	D4	107	I/O	Vertical Sync. (Programmable polarity) Slave mode: Vsync act as input Master mode: Vsync act as Output
HS	E1	108	I/O	Horizontal Sync Input. (Programmable polarity). Slave mode: Hsync act as input Master mode: Hsync act as Output
PDAT[7:0]	D1, C3, C2, C1, B2, B1, A2, A3	104, 103, 102, 101, 100, 99, 94, 93	I	Sensor or Video Data Input

USB2.0/MPEG2 Encoder (W99201) Bridge Controller

MPEG2 (W99201) Interface: (ICEMode_En# = don't care)

PIN NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
MPEG_CS#	D2	105	O	W99201 Chip Enable
EDACK	D3	106	O	Encoder data stream permission signal from VPRE (Programmable polarity)
EDRDY	D4	107	I	Encoder data stream delay signal (Programmable polarity)
EDCLK	E1	108	I	Encoder data stream sync clock (Programmable polarity)
EDAT[7:0]	D1, C3, C2, C1, B2, B1, A2, A3	104, 103, 102, 101, 100, 99, 94, 93	I	Encoder data stream

Software I2C Interface: (ICEMode_En# = don't care)

PIN NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SCL	J5	15	O	Serial Clock
SDA	H5	16	I	Serial Data

USB2.0/ATAPI Bridge Controller

CF/ATAPI (Host) Control Interface (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
ATA(CF)_DAT[15:0]	D1, C3, C2, C1, B2, B1, A2, A3, J1, J2, H1, H2, H3, G1, G2, F1	104, 103, 102, 101, 100, 99, 94, 93, 92, 91, 88, 87, 86, 85, 84, 83	I/O	ATAPI Data Bus
ATA(CF)_ADDR[2:0]	D4,D3,D2	107,106,105	O	ATAPI Address Bus
ATA(CF)_IOR#	E2	111	O/Z	ATAPI Device Read Strobe Signal
ATA(CF)_IOW#	E1	108	O/Z	ATAPI Device Write Strobe Signal
ATA(CF)_IORDY	F1	115	I	ATAPI Ready
ATA(CF)_CS0#	H3	120	O/Z	ATAPI Chip Select 0
ATA(CF)_CS1#	G1	109	O/Z	ATAPI Chip Select 1
ATA(CF)_RST#	F4	112	O/Z	ATAPI Reset
ATA_DMARQ	F2	114	I	ATAPI DMA Request
ATA_DMACK#	F3	113	O/Z	ATAPI DMA Acknowledge
ATA_INTRQ	G2	118	I	ATAPI Interrupt Request.

ATA (Device) Control Interface: (ICEMode_En# = don't care)

SIGNAL NAME	BGA PIN NO	LQFP PIN NO	TYPE	DESCRIPTION
SIDE_D[15:0]	D1, C3, C2, C1, B2, B1, A2, A3, J1, J2, H1, H2, H3, G1, G2, F1	104, 103, 102, 101, 100, 99, 94, 93, 92, 91, 88, 87, 86, 85, 84, 83	I/O	ATA Data Bus
SIDE_A[2:0]	D4, D3, D2	107,106,105	I	ATA Address Bus
SIDE_IOR#	E2	111	Ipu	ATA Device Read Strobe Signal
SIDE_IOW#	E1	108	Ipu	ATA Device Write Strobe Signal
SIDE_CS0#	H3	120	Ipu	ATA Chip Select 0
SIDE_CS1#	G1	109	Ipu	ATA Chip Select 1
SIDE_RST#	F4	112	I	ATA Reset
SIDE_INTRQ	G2	118	O	ATA Interrupt Request.

6. ABSOLUTE MAXIMUM RATINGS

V_{DD} = VDD33, V_{SS} = VSS33

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}-V_{SS}	DC Power Supply	-0.3	+3.48	V
V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
Ta	Operating Temperature	0	+70	°C
Tst	Storage Temperature	-55	+150	°C

7. D.C. CHARACTERISTICS

(T_A= 25°C, VDD33 = 3.3V ± 5%, VDDCORE_18 = 1.8V ± 5%, Fosc = 48MHz, unless otherwise specified.)

7.1 Input Leakage Current:

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LK}	Input Leakage Current	V_{IN} = 0 to VDD33	-10	-	+10	µA

7.2 Input Characteristics

SYMBOL	PARAMETER	SPECIFICATION			UNIT
		MIN.	TYP.	MAX.	
VDD33	Operating Voltage	3.13	3.3	3.48	V
VDDCORE_18	Core Voltage	1.71	1.8	1.89	V
I_{DDINT}	Unconfigured Current	-	-	100	mA
I_{DD}	Operating Current	-	-	85	mA
I_{PWDN}	Power Down Current	-	12µA @VDD33 = 3.3V	200µA @VDD33 = 3.48V	µA
V_{IH}	Input High Voltage	2.0	-	VDD33+0.2	V
V_{IL}	Input Low Voltage	0	-	0.4	V
V_{IH}	Input High Voltage Schmitt Trigger	-	1.8	-	V
V_{IL}	Input Low Voltage Schmitt Trigger	-	1.0	-	V

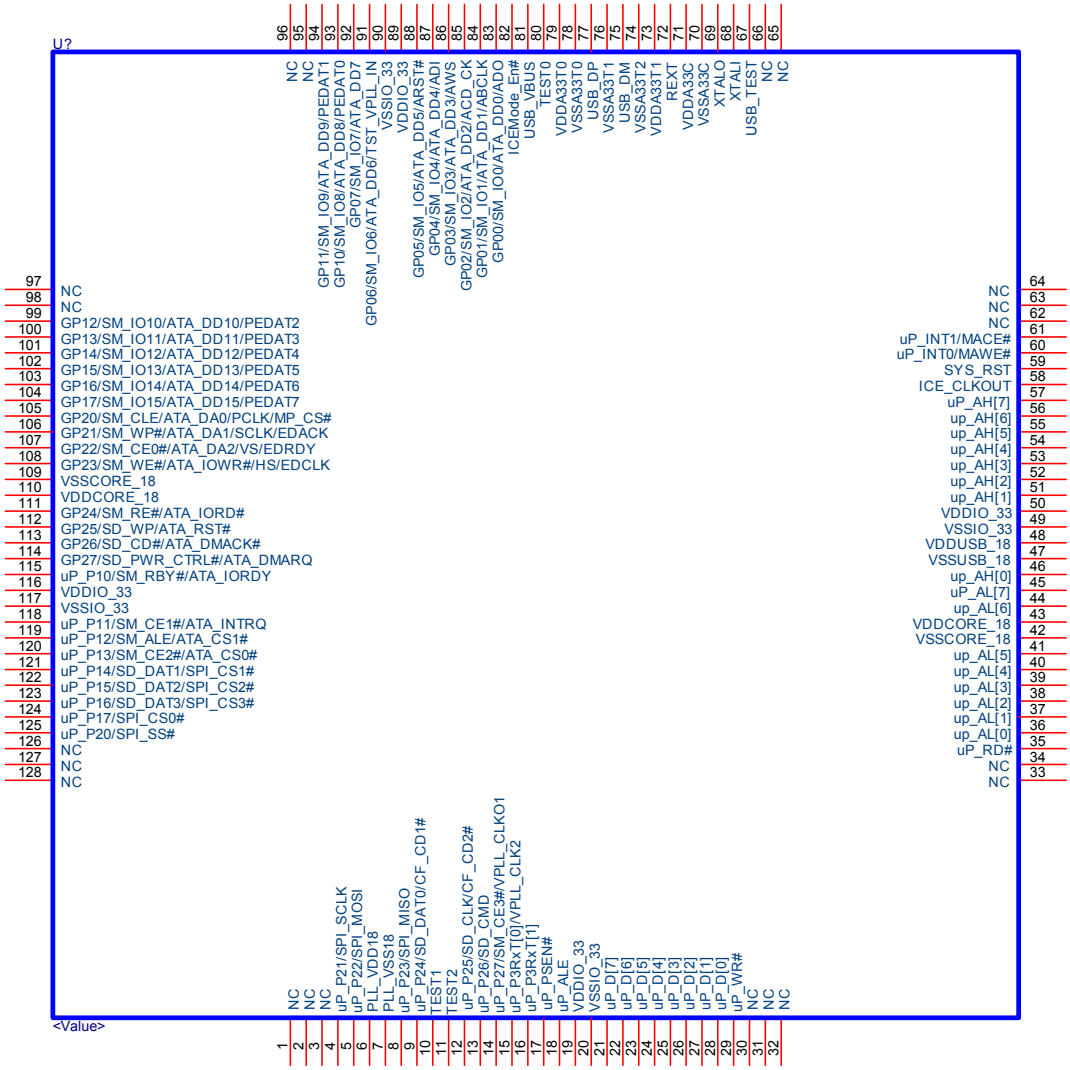
7.3 Output Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
VOL	Output Low Voltage / VDD33 = 3.3V	IOL = +8mA	-	-	0.4	V
VOH	Output High Voltage / VDD33 = 3.13V	IOH = -8mA	2.4	-	-	V
IOZ	TRI-State Leakage Current	VOL = VDD33 VOH = VSS33	-10	-	+10	uA

8. PIN ASSIGNMENT

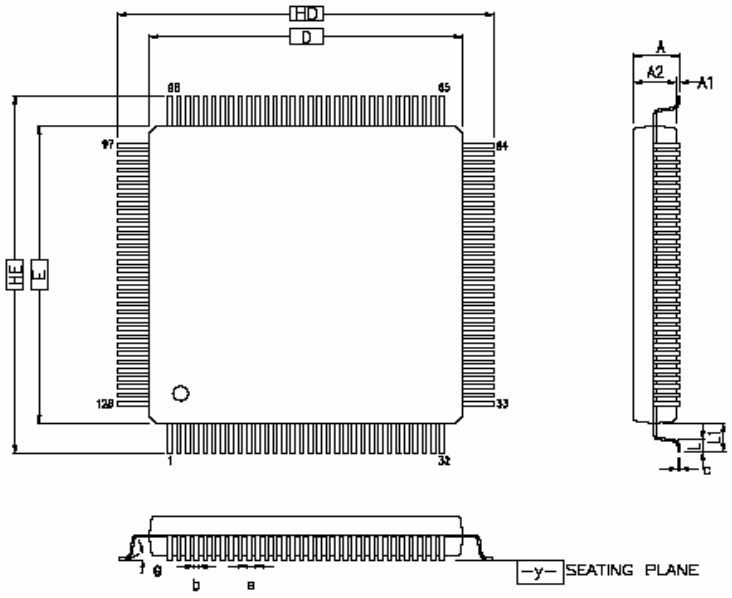
8.1 TFBGA111: (W99888)

8.2 LQFP128: (W99888F)



9. PACKAGE SPECIFICATION

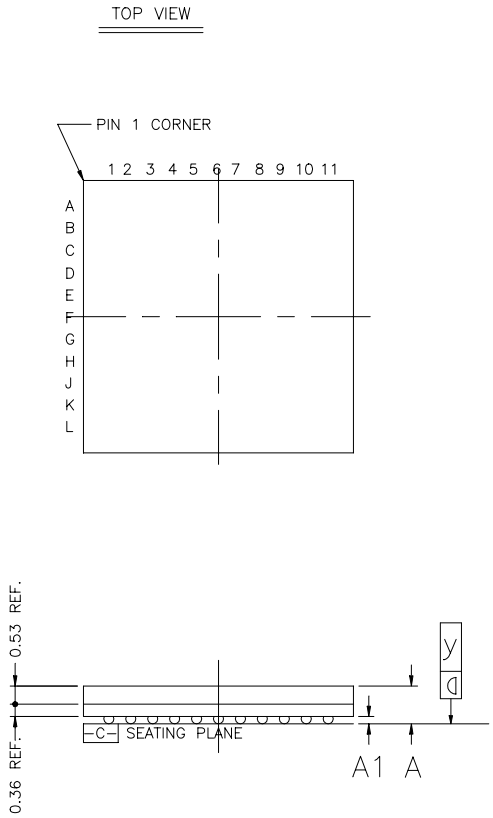
128L LQFP – 14 x1 4 x 1.4 mm footprint 2.0 mm

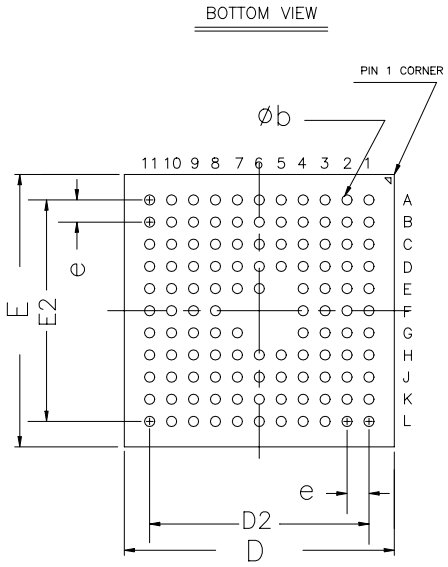


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

TFBGA 115Ball (8 x 8 MM^2, Ball pitch: 0.65 mm, Ø = 0.3 mm)





Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.16	–	0.26	0.006	–	0.010
D	7.95	8.00	8.05	0.313	0.315	0.317
D2		6.50 REF.			0.255 REF.	
E	7.95	8.00	8.05	0.313	0.315	0.317
E2		6.50 REF.			0.255 REF.	
y		0.08 REF.			0.003 REF.	
øb	0.27	–	0.37	0.0106	–	0.0145
e	---	0.65	---	---	0.0255	---

Important Notice

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