MOBILE MULTIMEDIA PROCESSOR

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1. GENERAL DESCRIPTION

W99702G is a highly integrated, low-power and high performance MPEG-4 audio/video chip with embedded memory for multimedia cellular phones. It contains a 32-bit ARM CPU, Sensor ISP, JPEG image codec, MPEG-4 video codec, Audio engine, 2-D graphics engine, video processing engine, display controller, USB 1.1 device controller, and flash memory card interface.

W99702G supports 8-bit YCbCr or 10-bit raw data RGB CMOS / CCD sensor interface and provides advanced AEC / AWB / AFC algorithm to deliver professional photo image quality. The supported image resolution can be up to 2M pixels.

The JPEG image codec is compliant with ISO/IEC 10918-1 baseline standard and JFIF format. It is capable of encoding or decoding 30fps JPEG pictures at VGA resolution.

The MPEG-4 video codec is compliant with ISO/IEC 14496-2 Visual standard Simple Profile Level 3. It can also support H.263 short header mode for the implementation of 3GP movie. The video codec supports smart bit rate control and performs up to 30fps CIF simultaneous encode and decode for video conferencing applications.

The audio engine integrates a single channel 16-bit ADC, as well as audio control interface for external audio codec or melody chip. W99702G can provide voice recorder and high quality MP3 and AAC music playback.

The 2-D graphics engine is used for MMI and JAVA acceleration.

The video processing engine is used for the image / video data processing. It can provide versatile functions for image / video capture and playback such as sticker, rotation, color effects, etc.

The display controller can support dual LCM display and bypass mode. The supported LCM can be up to 262K colors.

The USB device controller is compliant with USB1.1 specification and can support configurable pipes for rich USB functions such as Mass storage, PC camera, Virtual COM port and PictBridge.

The flash memory card interface can support embedded NAND type flash and SD / mini-SD / MMC / RS-MMC / T-Flash for storing multimedia data.The file system is FAT compatible and can be accessed by host through host interface.

The internal 32-bit ARM CPU handles audio/video synchronization, file system and all multimedia functions such as still camera, video camcorder, MP3 player and voice recorder according to the high-level commands from host. The host driver programmer can control W99702G without knowing its register programming to shorten the development cycle.

2. FEATURES

- **CPU**
  - Built-in 32-bit ARM CPU with I-cache and D-cache.
  - Programmable with CPU operating frequency from 200KHz to 166MHz.
  - Program code can be downloaded into program buffer through Host Interface or JTAG port.
  - Integrate JTAG port to support real time, non-stop ICE function for system development and debug.

- **Sensor Interface and ISP**
  - Support up to 2M pixels CMOS / CCD image sensor.
  - Support 8-bit CCIR-656 YCbCr or 10-bit raw RGB Bayer input format.
  - Support both master mode and slave mode sensors.
  - Support universal serial interface to program CMOS / CCD image sensor.
  - Support 30fps real-time preview.
  - Support sensor ISP for color image processing:
    - Black Level Clamping
    - Missing Color Interpolation
    - Auto Exposure Control (AEC)
    - Auto White Balance Control (AWB)
    - Auto Focus Control (AFC)
    - Bad Pixel Concealment
    - Flash Light Control
    - Lens Shading Compensation
    - False Color Suppression
    - Edge Enhancement
    - Color Correction
    - Gamma Correction
    - Contrast Stretching / Hue / Saturation Adjustment
  - Support complete software utilities for sensor module calibration.

- **Video Processing Engine**
  - Support hardware image sticker function for both preview and compression data.
  - Support real-time hardware flip / mirror / rotation (90, 180 and 270 degree) function.
  - Support special image color effect functions such as B&W, Negative, Sepia, Oil, Emboss, Binary, etc.
  - Support linear scaling down from 1 ~ X/256 with 2D filter for better image quality.
  - Support YUV-to-RGB and RGB-to-YUV Color Format Conversion and Data Format Transformation for video display and image editing.

❑ **MPEG-4 Video Codec**

- Support MPEG4 Simple Profile Level 3 compression tools and compliant with ISO/IEC 14496-2 Visual Standard.
- Support I-VOP and P-VOP.
- Support motion estimation with 16×16 search range and half pixel resolution.
- Support AC/DC prediction, 4 motion vectors per macro block, unrestricted motion compensation.
- Support RVLC and Data Partitioning for error resilience.
- Support Short Header Mode (H.263 baseline).
- Support real-time 30fps video compression/decompression up to CIF (352×288) resolution.
- Support smart bit rate control and simultaneous encode/decode for video conferencing application.

❑ **JPEG Image Codec**

- Compliant with ISO/IEC 10918-1 internal JPEG standard.
- Support resolution up to 2M pixels and capable of encoding or decoding 30fps real-time VGA JPEG.
- Support YUV 4:2:2 and 4:2:0 formats encode.
- Support YUV 4:4:4, 4:2:2 and 4:2:0 formats decode.
- Support programmable quantization table.
- Support programmable Huffman table decoding.
- Capable of decoding JPEG image with specified rectangle to a specified size.
- Support resolution scaling up and 1× ~ 8× linear digital zoom.
- Support JPEG resizing and trimming.
- Support thumbnail image.
- Support JPEG Exchangeable Image File (EXIF) format.

❑ **Audio Engine**

- Support I2S codec interface to connect with external audio codec.
- Support audio control interface for external melody chip such as Yamaha MA-3, MA-5, Winbond W56940 and W56964.
- Integrate a 16-bit ADC for microphone analog input
- Support MP3 / AMR-WB decoder.
- Support AAC-LC / AMR-NB / ADPCM codec.

❑ **2-D Graphics Engine**

- Support 8/16/32-bpp graphics modes.
- Support 5 Bit Block Transfer (BLT) function with ROP function.
  - Write BitBLT
  - Read BitBLT
  - Copy BitBLT
  - Pattern Fill BitBLT
  - Solid Fill BitBLT

- Hardware Clipper.
- Tile BLT.
- Mono-to-Color Expansion for text output acceleration.
- Transparency Control (Sprites).
- Image Blending (Semi-Transparency).
- Bit Plane Mask.
- Programmable 2D filter functions for special color effects.
- Support Bresenham Line and Frame Drawing.

❑ **Display Controller**

- Support 8/12/16/18-bit RGB data output interface to connect with 80/68 series MPU type LCM module.
- Support LCM resolution up to 240×320.
- Support dual LCM control for MPU interfaced LCM.
- Support LCM bypass mode that allows the host to access LCM directly while W99702G is in suspend mode.
- Support RGB444 (4K colors), RGB565 (65K colors) and RGB666 (262K colors) color formats for display output.
- Support 8/16/32-bit graphics mode OSD.
- Support graphics / video overlay using color key and alpha blending control.
- Support 1× ~ 8× linear scaling up.
- Support playback pan / tilt / zoom.
- Support CCIR-656 8-bit YUV output for external TV encoder.
- Support picture-in-picture display for video conferencing applications.

❑ **USB Device Controller**

- Compliant with USB 1.1 specification.
- Support four USB pipes including one control pipe and 3 configurable pipes for rich USB functions.
- Support USB Mass Storage.
- Support USB PC Camera (DirectShow).
- Support USB Virtual COM Port with modem capability.
- Support USB PictBridge.

❑ **Memory Card Interface**

- Support NAND Type flash.
- Support SD, mini-SD, MMC, RS-MMC,and T-Flash.

❑ **Host Bus Interface**

- Support 8/9/16/18-bit parallel slave interface to connect with 80 or 68 series host MPU.
- Support bypass mode to allow the host to access the LCM and melody chip directly.
- Support DMA data transfer between host MPU and W99702G.
- Allow host to access W99702G memory buffer and control registers.

- **Peripheral Support**
  - Support two Timers and one programmable 24-bit Watch-Dog timer.
  - Supports universal synchronous serial interface for connecting with synchronous serial device.
  - Support GPIOs for system control.
- **J2ME MIDP 2.0 Graphics / Game native layer acceleration**
- **Multimedia File Format Support**
  - 3GP (H.263+AMR-NB)
  - MP4 (MP4+AAC-LC)
  - AVI
  - ASF
- **Flash File System Support**
  - Support FAT12/16/32
  - Support long filename.
- **Power Supply**
  - Core Power Supply: 1.2V
  - Host Interface: 1.8V - 3.3V
  - I/O Power Supply:
    - General Digital I/O: 2.5V – 3.3V
    - USB Transceiver: 3.0V – 3.3V
    - Audio ADC: 2.5V – 3.3V
- **Package: LFBGA 184-Balls package (10mm x 10mm), Lead-free.**

3. PIN DESCRIPTION

3.1 W99702G Pin Definition

The following signal types are used in these descriptions.

3.1.1 Pin Type Definition

TYPE	DESCRIPTION
I	Input pin
IS	Input pin with Schmitt trigger
B	Bi-directional input/output pin
BU	Bi-directional input/output pin with internal pull-up
BD	Bi-directional input/output pin with internal pull-down
O	Output pin
A	Analog input/output pin
P	Power supply pin
G	Ground pin
#	Active low

3.1.2 Pin List

USB Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DP	B1	A	USB DP (D+) Signal
DM	D2	A	USB DM (D-) Signal
USBVDD	D18	P	USB Power Supply +3.3V ± 0.3V.
USBVSS	E7	G	USB Ground.

Sensor or Video Input Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SVID[1:0] / GPIOA[1:0]	J6, N1	BD	Sensor Data Input [1:0] GPIO Function : GPIOA[1:0]
SVID[9:2]	K18, L6, G18, R1, J18, N2, P1, K6	ID	Sensor Data Input [9:2]
SPCLK	P2	ID	Clock Input from Sensor for Pixel Data
SVS	R2	BD	Vertical Sync.
SHS	N18	BD	Horizontal Sync.
SCLK	L5	O	Clock Output to Sensor

Sensor or Video Input Interface, continued

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SCK / GPIOA[2]	T1	BU	Serial Interface Clock GPIO Function: GPIOA[2]
SDI/SDA / GPIOA[3]	L13	BU	Serial Data Input/ Serial Data Acknowledge GPIO Function: GPIOA[3]
SDO/SDE / GPIOA[4]	L14	BU	Serial Interface Data Output / Serial Data Enable GPIO Function: GPIOA[4]

Audio Digital Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
ASCLK / GPIOA[8]	F2	BU	Audio Interface: Audio System Clock GPIO Function: GPIOA[8]
ADO / GPIOA[9]	M18	BU	Audio Interface: I2S=> Audio Data Output GPIO Function: GPIOA[9]
AWS / GPIOA[10]	F1	BU	Audio Interface: I2S=> Audio Word Select GPIO Function: GPIOA[10]
ABCLK / GPIOA[11]	G5	BD	Audio Interface: I2S=> Audio Bit Clock Output GPIO Function: GPIOA[11]
ADI / GPIOA[12]	F8	BD	Audio Interface: I2S=> Audio Data Input GPIO Function: GPIOA[12]
ARST# / GPIOA[13]	E1	BD	Audio Interface: Audio Reset GPIO Function: GPIOA[13]

Audio Analog Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CAD1	B2	A	Decoupling for ADC
MIC_IN	A2	A	Audio (Microphone) Input
MIC_BIAS	B17	A	Microphone Bias
VREFC	B18	A	ADC Reference Voltage
ADO_AVDD	A17	P	Audio ADC Analog Power Supply *+3.3V*
ADO_AVSS	B15	G	Audio ADC Analog Ground
ADO_DVDD	J13	P	Audio Digital Power Supply 1.2V
ADO_DVSS	C1	G	Audio Digital Ground

JTAG Interface Pins

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
TCK	U12	ID	JTAG Test Clock
TMS	V16	IU	JTAG Test Mode Select
TDI	V12	IU	JTAG Test Data in
TDO	U11	O	JTAG Test Data out
TRST#	V11	IU	JTAG Reset

UART Interface Pins

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
RTS# / GPIOA[16]	K14	BD	Request To Send / GPIO Function: GPIOA[16]
DTR# / GPIOA[17]	N5	BD	Data Terminal Ready GPIO Function: GPIOA[17]
SOUT / GPIOA[18]	K17	BD	Serial Data Output (TXD) GPIO Function: GPIOA[18]
CTS# / GPIOA[19]	U2	BD	Clear To Send GPIO Function: GPIOA[19]
DSR# / GPIOA[20]	U5	BD	Data Set Ready GPIO Function: GPIOA[20]
RLSD# / GPIOA[21]	U4	BD	Receive Line Signal Detect GPIO Function: GPIOA[21]
RI# / GPIOA[22]	L18	BD	Ring Indicator GPIO Function: GPIOA[22]
SIN / GPIOA[23]	M14	BD	Serial Data Input (RXD) GPIO Function: GPIOA[23]
SOUT2 / GPIOA[24]	V2	BD	Serial Data Output –2 (High Speed TXD) GPIO Function: GPIOA[24]
SIN2 / GPIOA[25]	U1	BD	Serial Data Input – 2 (High Speed RXD) GPIO Function: GPIOA[25]

LCM Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
LCLK / LA0	H13	BD	Clock Input for output Data to TV encoder LCM Interface (O): Address-0, R/S# (CMD/DAT#)
LCLKO / LCS0#	H5	O	Clock for Digital Display Data Output LCM Interface : LCD Chip Select-0
LCS1# / GPIOB[17]	G1	BU	LCM Interface : LCD Chip Select-1 GPIO Function : GPIOB[17]
LWR# / LR/W#/ LHSYNC	H1	O	LCM 80-series interface: Write Enable, Active Low LCM 68-series interface: “1” => Read, “0”=> Write Horizontal Sync to TV encoder
LRD# / LE / LVSYNC	G17	O	LCM 80-series interface: Read Enable, Active Low LCM 68-series interface: Data Enable, Active High Vertical Sync to TV encoder
LDAT [7:0]	L1, H17, L2, J17, M1, H6, M2, H18	BU	LCM Data Bus / TV-encoder Data Bus Bit-7_0
LDAT [15:8] *GPIOB[7:0]*	H2, J5, H14, K5, K1, J2, J14, K2	BU	LCM Data Bus Bit-15_8 GPIO Function : GPIOB[7:0]
LDAT [17:16] / *GPIOB[9:8]*	G2,J1	BU	LCM Data Bus Bit-17_16 GPIO Function : GPIOB[9:8]
LCS2# GPIOB[16]	G14	BU	MCU Interface : LCD Chip Select 2 GPIO Function : GPIOB[16]

Memory Bus Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
MSCE#	E8	BU	Memory Slave (I) : Chip Enable Signal
MSA3	B6	BU	Memory Slave (I) : Address – 3
MSWR# / MSR/W#	A5	BU	Memory Slave 80 (I): Write Enable Signal Memory Slave 68 (I): Read/Write Control
MSRD# / MSE	E10	BU	Memory Slave 80 (I): Read Enable Signal Memory Slave 68 (I): Data Enable
MSA[2:0]	F17, A4, B14	BD	Memory Slave (I): Address MSA[2:0]
MSD[7:0] /	F11, B9, F10, A8, E17, A7, E11, B7	BD	Memory Slave (I): Data Bus Bit-7_0
MSD[15:8] / GPIOB[31:24]	F14, A11, B11, A10, D17, B10, E12, A9	BD	Memory Slave (I): Data Bus Bit-15_8 GPIO Function: GPIOB[31:24]
MSD[16] / GPIOB[18]	B8	BD	Memory Slave (I): Data Bus Bit-16 GPIO Function : GPIOB[18]
MSD[17] GPIOB[19]	A6	BD	Memory Slave (I) : Data Bus Bit-17 GPIO Function : GPIOB[19]

NAND / SD / MMC Memory Card Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SCS0# / GPIOS[0]	P13	BU	NAND Flash Interface =>(O): Chip-0 Enable GPIO Function: GPIOS[0]
SCS1# / SD_CLK / GPIOS[1] / MMC_CLK	V14	BU	NAND Flash Interface =>(O): Chip-1 Enable SD : Clock GPIO Function: GPIOS[1] MMC : Clock
SALE / GPIOS[2]	U18	BU	NAND Flash Interface => (O): Address Latch Enable GPIO Function: GPIOS[2]
SCLE / GPIOS[3]	U10	BU	NAND Flash Interface => (O): Command Latch Enable GPIO Function: GPIOS[3]
SWE# / GPIOS[4]	P9	BU	NAND Flash Interface => (O): Write Enable GPIO Function: GPIOS[4]
SRE# / GPIOS[5]	U9	BU	NAND Flash Interface => (O): Read Enable GPIO Function: GPIOS[5]
SRB# / GPIOS[6]	T18	BU	NAND Flash Interface => (I): Ready/Busy Signal GPIO Function: GPIOS[6]
SWP# / GPIOS[7]	V9	BU	NAND Flash Interface => (O): Write Protect GPIO Function: GPIOS[7]
SD[0] / SD_DAT0 / GPIOS[8]/ MMC_DO	N11	BU	NAND Flash Interface => (I/O): Data Bus Bit-0 SD : Data-0 GPIO Function: GPIOS[8] MMC : Data-Out
SD[2:1] / SD_DAT[2:1] / GPIOS[10:9]	R17,V8	BU	NAND Flash Interface => (I/O): Data Bus Bit-2_1 SD : Data-2:1 GPIO Function: GPIOS[9]
SD[3]/ SD_DAT[3] / GPIOS[11]/ MMC_CS#	U8	BU	NAND Flash Interface => (I/O): Data Bus Bit-3 SD : Data-3 GPIO Function: GPIOS[10] MMC : Chip Select
SD[4] SD_CMD / GPIOS[12]/ MMC_DI	N10	BU	NAND (I/O): Data Bus Bit-4 SD : Command GPIO Function: GPIOS[11] MMC : Data-In
SD[7:5] / GPIOS[15:13]	U7, N9, V7	BU	NAND Flash Interface => (I/O): Data Bus Bit-7_5 GPIO Function: GPIOS[15:12]

GPIO Pins

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
GPIO[0] / HGPIO[0] / PCLK-A	V5	BU	General Purpose I/O [0] Programmable Clock Output-A (PWM Function)
GPIO[1] / HGPIO[1] / MSRDYO	A12	BU	General Purpose I/O [1] Force GPIO[1] to low state.
GPIO[2] / HGPIO[2] / FL_TRG	P11	BD	General Purpose I/O [2] Flashlight Trigger Control
GPIO[3] / HGPIO[3] / MSINTO	P18	BD	General Purpose I/O [3]
GPIO[5:4] / HGPIO[5:4] / FEINT[1:0]	P17, U6	BU	General Purpose I/O [5:4] Fast External Interrupt Input [1:0]
GPIO[7:6] / HGPIO[7:6] / FEINT[3:2]	R18, V6	BD	General Purpose I/O [7:6] Fast External Interrupt Input [3:2]
GPIO[8]	E18	BD	General Purpose I/O [8]
GPIO[9]	E2	BD	General Purpose I/O [9]
GPIO[10]	D1	BD	General Purpose I/O [10]
GPIO[11]	F18	BD	General Purpose I/O [11]
GPIO[12] USK	V3	BU	General Purpose I/O [12] Universal Serial Interface (USI): USK
GPIO[13] / UDI	P7	BU	General Purpose I/O [13] Universal Serial Interface (USI): UDI
GPIO[14] / UDO	V4	BU	General Purpose I/O [14] Universal Serial Interface (USI): UDO
GPIO[15] / UCS0	N8	BU	General Purpose I/O [15] Universal Serial Interface (USI) : UCS0
GPIO[16] / UCS1	P10	BU	General Purpose I/O [16] Universal Serial Interface (USI) : UCS1
GPIO[17] / CLK_IN2	N17	BU	General Purpose I/O [17] Clock-2 Input Pin
GPIO[18] / STDBY	L17	BD	General Purpose I/O [18] System Standby Flag STDBY Output
GPIO[19] / PCLK-B	M17	BD	General Purpose I/O [19] / Programmable Clock Output-B (PWM Function)

Miscellaneous

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
XIN	V13	I	Reference clock input from crystal or clock source.
XOUT	U13	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is used.
TME	U14	ID	Test Mode Enable. Only for test, this pin must be connected to GND for normal operation.
RST#	U17	IS	Reset In. This pin is active low to reset chip.
S2_PWR	A3	O	Power Plate Control Section 2.

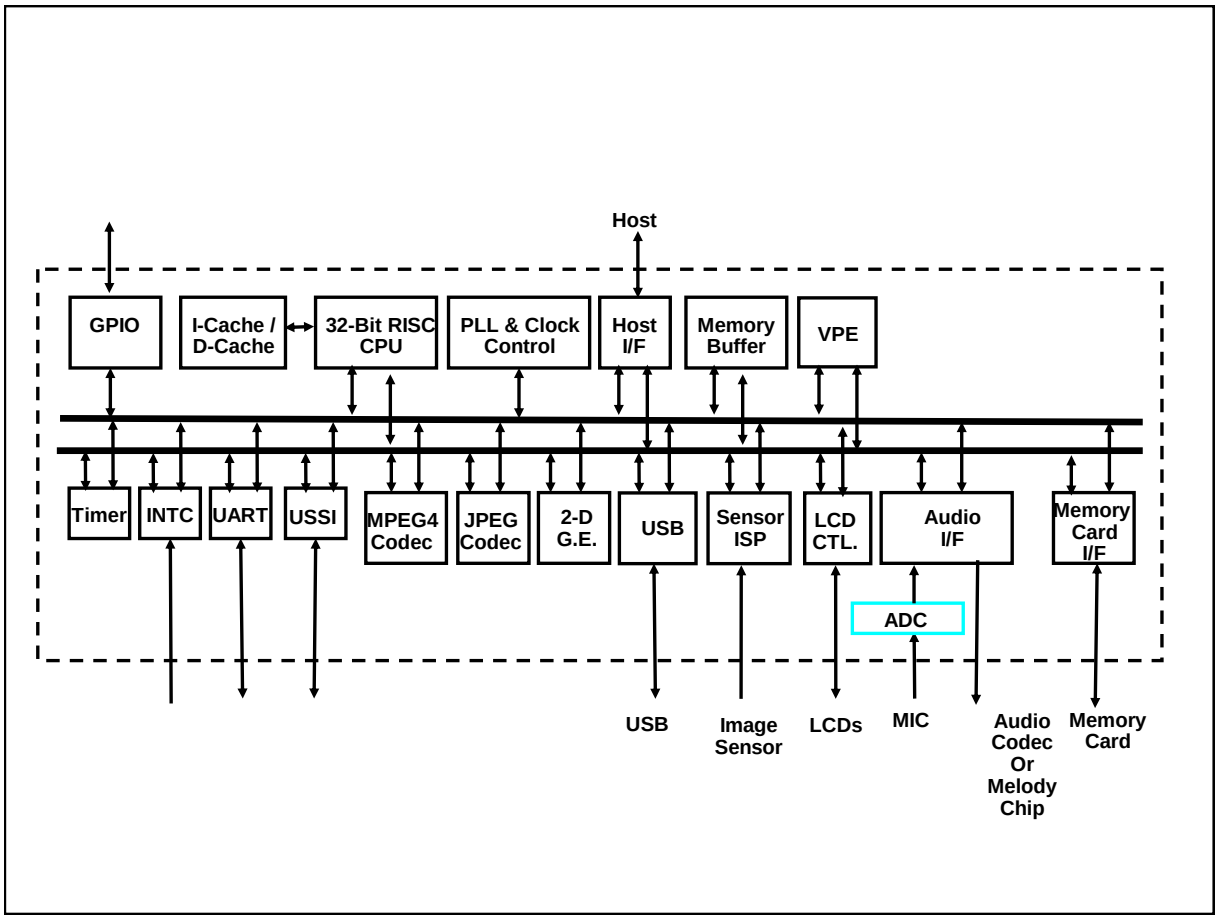
Power and Ground

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCC	F5, F9, M5, N14, P8, B5	P	I/O Pad Buffer Power Supply (2.5V~3.3V)
VCC_LCM	C18, E13	P	I/O Pad Buffer to Frame buffer Power Supply (2.6V~3.3V)
VCC_HIC	B12	P	HOST BUS Interface Buffer Supply (1.8V~3.3V)
GND	F12, F13, F6, F7, G13, G6, K13, M13, M6, N12, N13, N6, N7, V17, B4, A16	G	Ground.
VDDHI	B13	P	Internal Core Logic Power Supply (1.2 V)
VDDI	E9, P12, P6, E6, A15	P	Internal Core Logic Power Supply (1.2 V)
AVDDP	V15	P	PLL Power Supply (1.2 V)
AVSSP	U15	G	PLL Ground
FB_VCC	A13, A14	P	Frame Buffer Power Supply (2.6V ~ 3.3V)
VPRO	V10	ID	NC

3.2 W99702G Pin Assignment (Bottom View)

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	•∠
D	ADO_ AVDD	GND	VDD1	FB_ VCC	FB_ VCC	HGPIO1	MSD14	MSD12	MSD8	MSD4	MSD2	msd17	mswR#	MSA1	S2PWR	MIC_IN	D	A
VRE FC	MIC_ BIAS		ADO_ AVSS	MSA0	VDDHI	VCC_ HIC	MSD13	MSD10	MSD6	msd16	MSD0	msa3#	VCC	GND		CADI	DP	B
VCC_LCM																	ADO_ DVSS	C
USB VDD	MSD11															DM	GPIO 10	D
GPIO8	MSD3			D	VCC_LCM	MSD9	MSD1	MSRD#	VDDI	msCE#	USB VSS	CDDI	D			GPI O9	ARS T#	E
GPIO 11	MSA2			MSD15	GND	GND	MSD7	MSD5	VCC	ADI	GND	GND	VCC			ASC LK	AWS	F
SVID7	LRD#			ICS2#	GND							GND	ABC LK			LDAT 17	LCS 1#	G
LDAT0	LDAT6			LDAT 13	LA0							LDAT2	LCS 0#			LDAT 15	LWR#	H
SVID5	LDAT4			LDAT9	ADO_ DVDD							SVID1	LDAT 14			LDAT 10	LDAT 16	J
SVID9	SOUT			RTS#	GND							SVID2	LDAT 12			LDAT8	LDAT 11	K
RI#	GPIO 18			SDO	SDA							SVID8	SCLK			LDAT5	LDAT7	L
ADO	GPIO 19			SIN	GND							GND	VCC			LDAT1	LDAT3	M
shs	GPIO 17			VCC	GND	GND	SD_ DAT0	SD_ CMD	GPIOS14	GPIO 15	GND	GND	DTR#			SVID4	SVID0	N
HGPIO3	HGPIO5			D	FSCS0#	VDDI	HGPIO 2	GPIO 16	GPIOS4	VCC	GPIO 13	VDDI	D			SPC LK	SVID3	P
HGPIO7	SD_ DAT2															SVS	SVID6	R
GPIOS6																	SCK	T
GPIOS2	RST#		AVS SP	TME	XOUT	TCK	TDO	GPIOS3	GPIOS5	SD_ DAT3	GPIOS15	HGPIO4	DSR#	RLSD#		CTS#	SIN2	U
D	GND	TMS	AVD DP	SD_ CLK	XIN	TDI	TRST#	VPRO	GPIOS7	SD_ DAT1	GPIOS13	HGPIO6	HGPIO0	GPIO 14	GPIO 12	SOUT2	D	V

4. W99702G BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 Digital Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient temperature	-20	85	°C
Storage temperature	-40	125	°C
DC supply voltage for core (1.2V) power (VDDI)	0	1.3	V
DC supply voltage for I/O (3.3V) power (VDDB)	0	3.6	V
I/O pin voltage with respect to V_{SS}	-0.3	VDDB +0.4	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 Digital DC Characteristics

Table 5-2 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDDB	Power Supply for I/O Pads		2.6	3.0	3.6	V
USBVDD	Power Supply for USB Transceiver		3.0	3.30	3.6	V
AVDDP	Power Supply for PLL		1.15	1.20	1.30	V
VDDI	Power Supply for Core		1.15	1.20	1.30	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2.0		VDDB +0.3	V
V_{OL}	Output Low Voltage	I_{OUT} = 2mA			VSS+0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2mA	2.4			V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V			10	µA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V			-10	µA
I_{UP}	Pull-up Current	V_{IN} = 0V			-500	µA
I_{PD}	Power Down Current No load, Host inactived.			5	10	µA
I_{DD}	Active Current 3GP recording, CIF-30fps	VDDB=2.8V		15		mA
		VDDI=1.2V		60		
Top	Operation Temperature		-20		70	°C

5.3 Digital AC Characteristics

5.3.1 Reset AC Characteristics

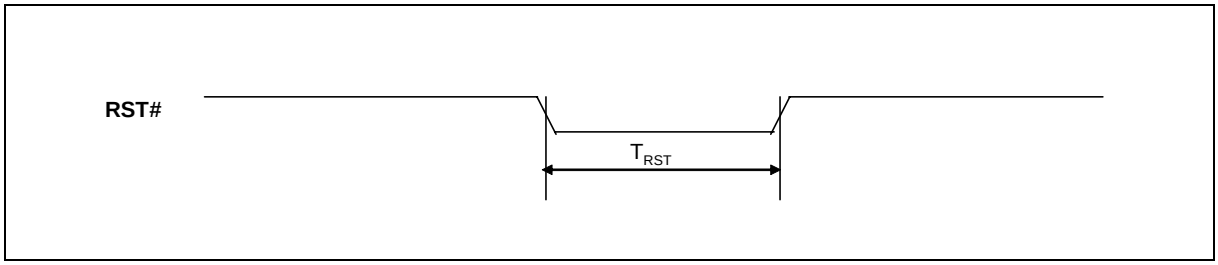


Figure 5-1 Reset Timing Diagram

Table 5-3 Reset Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{RST}	Reset Pulse Width		10.0		mS

5.3.2 Clock Input Characteristics

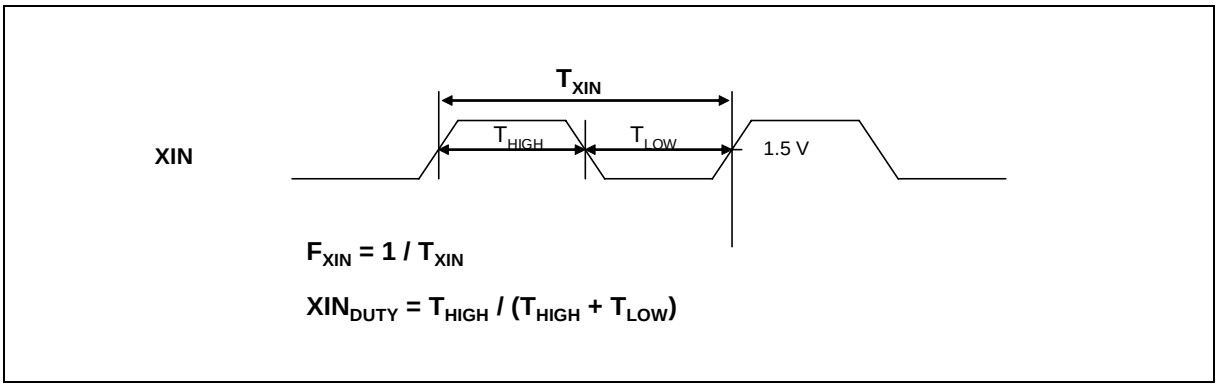


Figure 5-2 Clock Input Timing Diagram

Table 5-4 Clock Input Timing Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
F_{XIN}	Clock Input Frequency	4	12.0		MHz
XIN_{DUTY}	Clock Input Duty Cycle	45	50	55	%
V_{IL} (XIN)	XIN Input Low Voltage	0		0.8	V
V_{IH} (XIN)	XIN Input High Voltage	2.0		VDDB +0.3	V

5.3.3 Video Input AC Characteristics

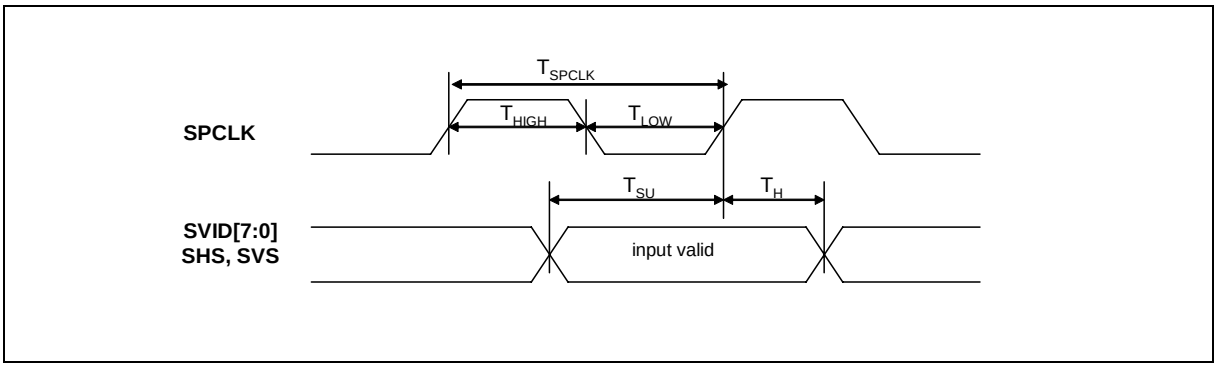


Figure 5-3 Input Video Timing Diagram

Table 5-5 Input Video Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
F_{SPCLK}	SPCLK Frequency = 1 / T_{SPCLK}	---	96	MHz
T_{HIGH}	SPCLK Clock High Time	8.0	---	ns
T_{LOW}	SPCLK Clock Low Time	8.0	---	ns
T_{SU}	SVID[9:0], SHS, SVS Setup Time	1.0	---	ns
T_H	SVID[9:0], SHS, SVS Hold Time	1.0	---	ns

5.3.4 Host Interface: Memory Bus AC Characteristic

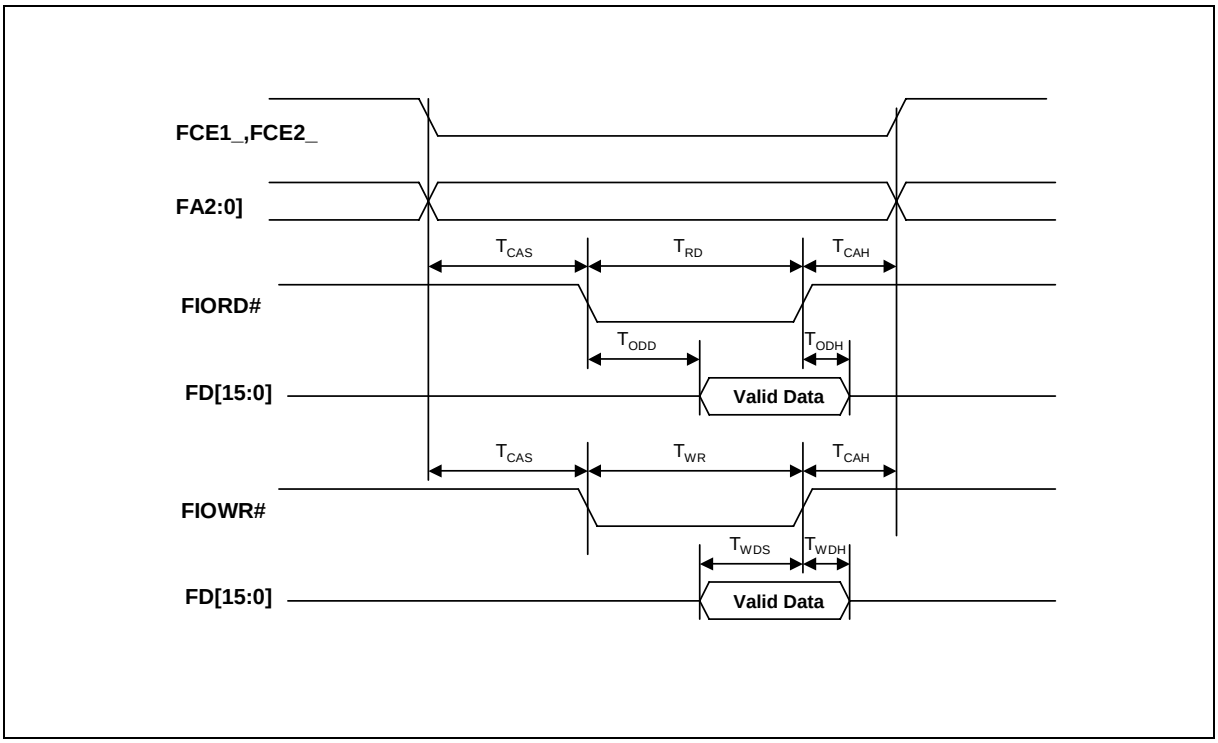


Figure 5-4 Host Interface : Memory Bus Timing Diagram

Table 5-6 Host Interface: Memory Bus Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{CAS}	Set-up time, FCE1_, FCE2_ and FA valid before FIORD# & FIOWR# low	0	---	ns
T_{CAH}	Hold time, FCE1_, FCE2_ and FA valid after FIORD# & FIOWR# high	0	---	ns
T_{ODD}	FIORD# Low to Data Valid Delay	---	8.5	ns
T_{ODH}	Read Data Output Hold Time	2.65	---	ns
T_{RD}	FIORD# Pulse Width	12	---	ns
T_{WDS}	Set-up time, FD valid before FIOWR# low	0	---	ns
T_{WDH}	Hold time, FD valid after FIOWR# high	0	---	ns
T_{WR}	FIOWR# Pulse Width	12	---	ns

5.3.5 LCD Interface AC Characteristics

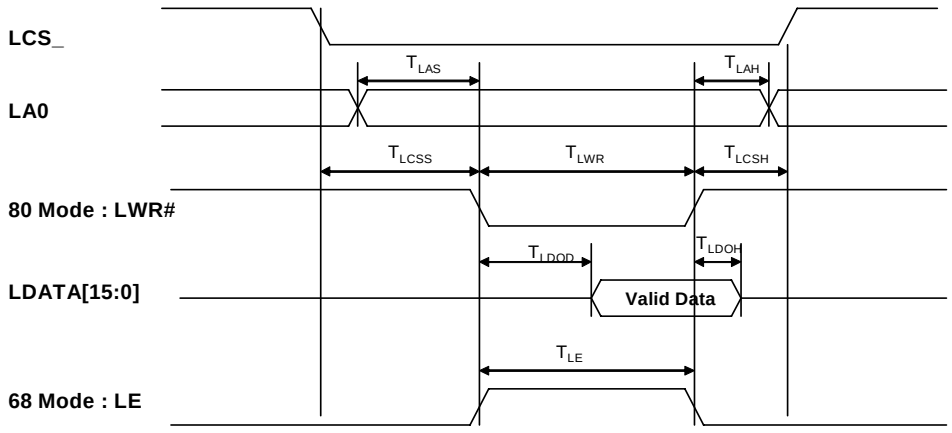


Figure 5-5 LCD Interface Timing Diagram

Table 5-7 LCD Interface Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{LCSS}	Chip Select Set-up Time		1/2	---	PCLK
T_{LCSH}	Chip Select Hold Time		1/2	---	PCLK
T_{LAS}	Address Set-up Time		1	---	PCLK
T_{LAH}	Address Hold Time		1	---	PCLK
T_{LDOD}	Write Data Active Delay		0	1/2	PCLK
T_{LDOH}	Write Data Hold Time		1/2	---	PCLK
T_{LWR}	LWR# Pulse Width	80 Mode	1/2	---	PCLK
T_{LE}	LE Pulse Width	68 Mode	1/2	---	PCLK

5.3.6 SD/MMC Host Interface AC Characteristics

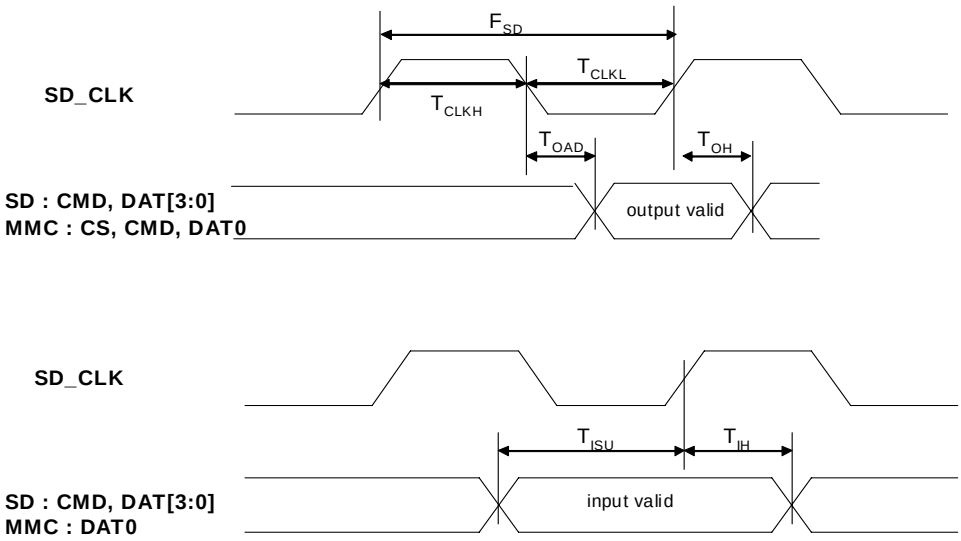


Figure 5-6 SD/MMC Host Interface Timing Diagram

Table 5-8 SD/MMC Host Interface Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
F_{SD}	SD/MMC Clock Frequency	Identification Mode	0	400	KHz
F_{SD}	SD/MMC Clock Frequency	Data Transfer Mode	0	25	MHz
T_{CLKH}	SD/MMC Clock High Time		10	---	ns
T_{CLKL}	SD/MMC Clock Low Time		10	---	ns
T_{ISU}	CMD & Data Input Setup Time		5	---	ns
T_{IH}	CMD & Data Input Hold Time		5	---	ns
T_{OAD}	Output Active Delay (Falling Edge)		---	14	ns
T_{OH}	Output Hold Time		20	---	ns

5.3.7 NAND Flash Memory Interface AC Characteristics

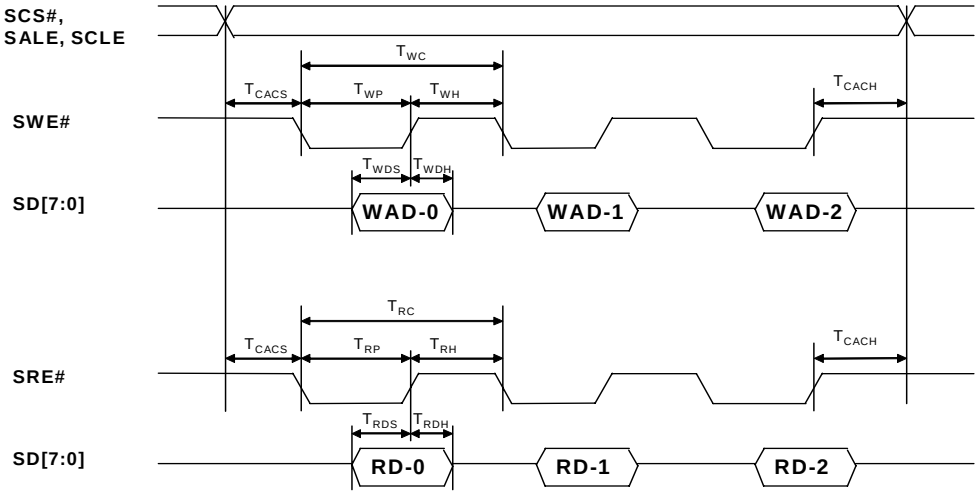


Figure 5-7 NAND Flash Memory Interface Timing Diagram

Table 5-9 NAND Flash Memory Interface Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{CACS}	SCS#, SALE, SCLE Setup Time before SWE#, SRE# Low	20	---	ns
T_{CACH}	SCS#, SALE, SCLE Hold Time after SWE#, SRE# High	40	---	ns
T_{WP}	Write Pulse Width	40	---	ns
T_{WH}	SWE# High Time	20	---	ns
T_{WC}	Write Cycle Time	80	---	ns
T_{WDS}	Write Data Ouptut Setup Time	30	---	ns
T_{WDH}	Write Data Output Hold Time	20	---	ns
T_{RP}	Read Pulse Width	40	---	ns
T_{RH}	SRE# High Time	20	---	ns
T_{RC}	Read Cycle Time	80	---	ns
T_{RDS}	Read Data Input Setup Time	30	---	ns
T_{RDH}	Read Data Input Hold Time	20	---	ns

5.3.8 Audio I2S Interface AC Characteristics

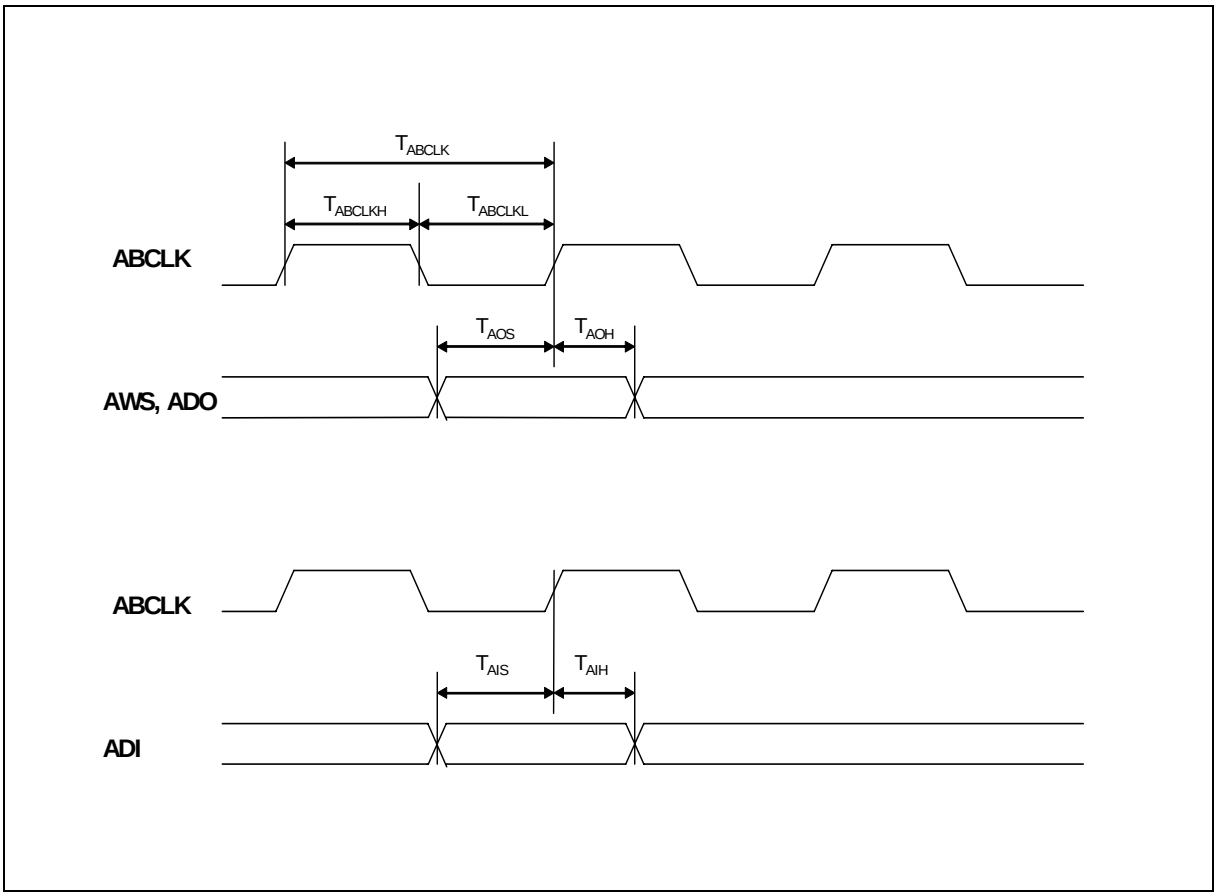


Figure 5-8 Audio I2S Interface Timing Diagram

Table 5-10 Audio I2S Interface Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{ABCLKH}	Audio Bit Clock Output High Time	16	---	ns
T_{ABCLKH}	Audio Bit Clock Output Low Time	16	---	ns
T_{ABCLK}	Audio Bit Clock Output Cycle Time	40	---	ns
T_{AOS}	Audio Data Output Setup Time	8	---	ns
T_{AOH}	Audio Data Output Hold Time	8	---	ns
T_{AIS}	Audio Data Input Setup Time	8	---	ns
T_{AIH}	Audio Data Input Hold Time	8	---	ns

5.3.9 Host Universal Synchronous Serial Interface AC Characteristics

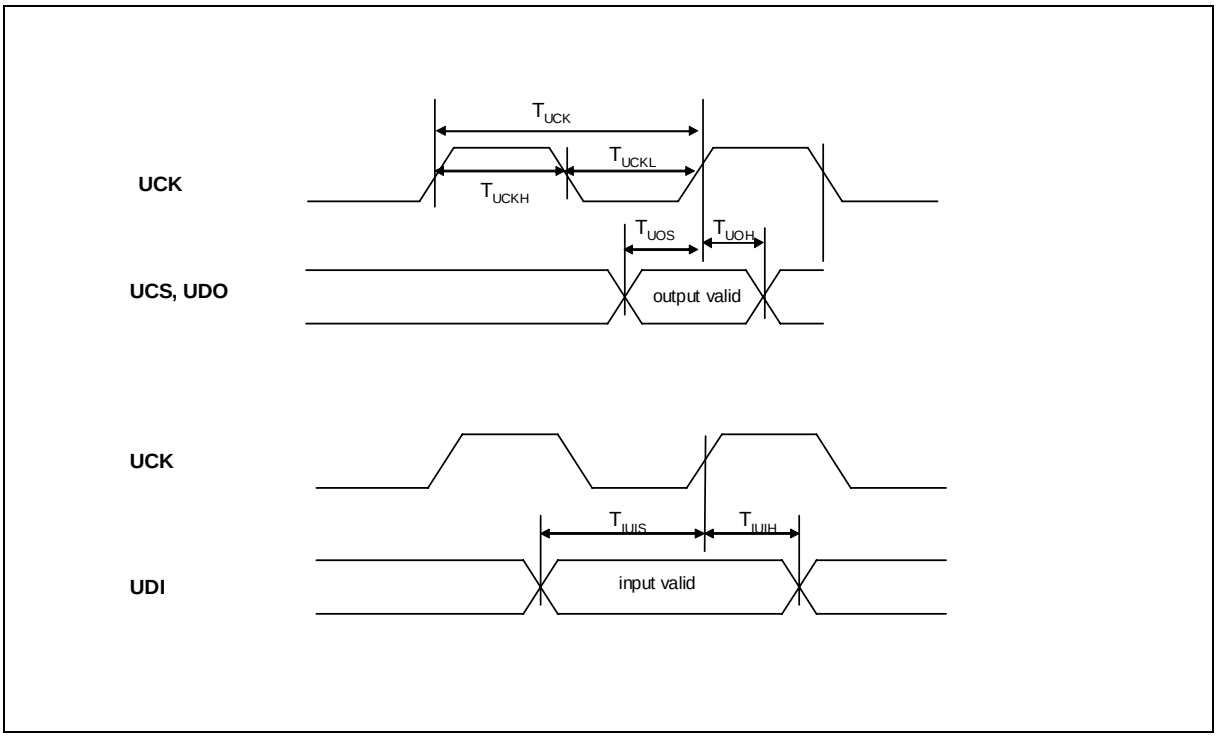


Figure 5-9 Universal Synchronous Serial Interface Timing Diagram

Table 5-11 Host Universal Synchronous Serial Interface Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{CLKH}	Clock Output High Time	0.4	---	SCLK
T_{CLKL}	Clock Output Low Time	0.4	---	SCLK
T_{CLK}	Clock Cycle Time	1.0	---	SCLK
T_{UOS}	UCS#, UDO Output Setup Time	0.3	---	SCLK
T_{UOH}	UCS#, UDO Output Hold Time	0.3	---	SCLK
T_{UIS}	UDI Input Setup Time	0.3	---	SCLK
T_{UIH}	UDI Input Hold Time	0.3	---	SCLK

Note: SCLK = 4 * PCLK (APB Clock, the frequency of this clock is specified by Clock Divider Register-0 & 1)

5.3.10 USB Transceiver AC Characteristics

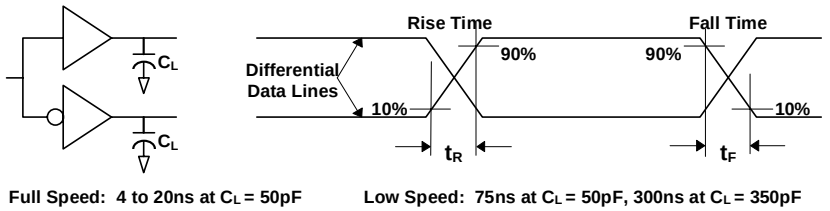


Figure 5-10 Data Signal Rise and Fall Time

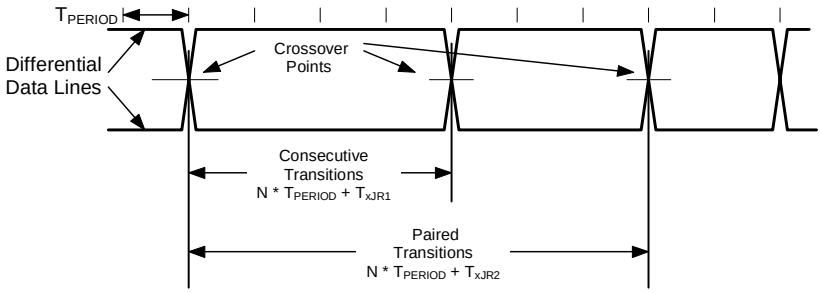


Figure 5-11 Differential Data Jitter

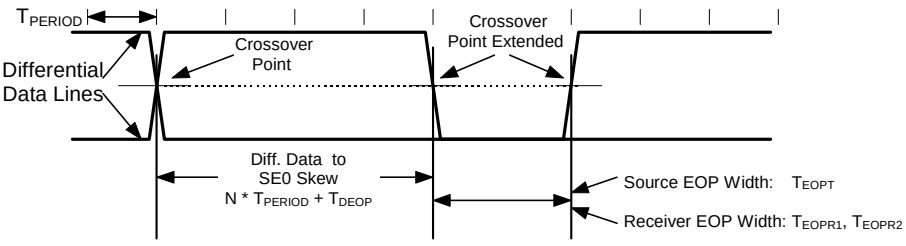


Figure 5-12 Differential to EOP Transition Skew and EOP Width

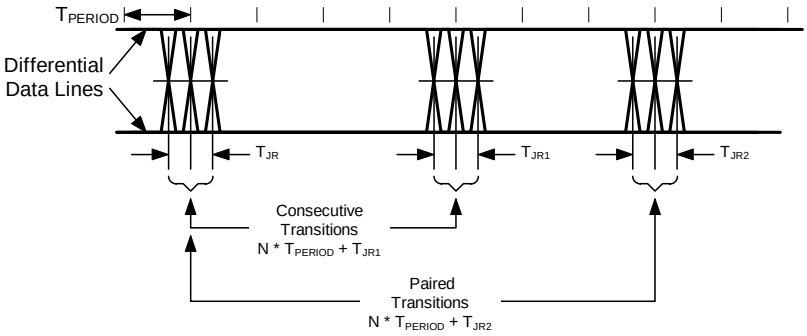


Figure 5-13 Receiver Jitter Tolerance

Table 5-12 USB Transceiver AC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_R	Rise Time	CL = 50 pF	4	20	ns
T_F	Fall Time	CL = 50 pF	4	20	ns
T_{RFM}	Rise/Fall Time Matching		90	110	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ±0.25%)	11.97	12.03	Mbps
	Source Differential Driver Jitter				
T_{DJ1}	To Next Transition		-3.5	3.5	ns
T_{DJ2}	For Paired Transitions		-4.0	4.0	ns
T_{EOPT}	Source EOP Width		160	175	ns
T_{DEOP}	Differential to EOP Transition Skew		-2	5	ns
	Receiver Data Jitter Tolerance				
T_{JR1}	To Next Transition		-18.5	18.5	ns
T_{JR2}	For Paired Transitions		-9	9	ns
	EOP Width at Receiver				
T_{EOPR1}	Must Reject as EOP		40		ns
T_{EOPR2}	Must Accept as EOP		82		ns

5.4 Audio Interface (ADC) Characteristics

5.4.1 Recommend Operation Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Digital Supply Range	ADO_DVDD	1.1	1.2	1.3	V
Analog Supply Range	AVDD	2.5	3.0	3.6	V
Ground	DVSS, AVSS		0		V
Temperature	TA	-20		85	^{o}C

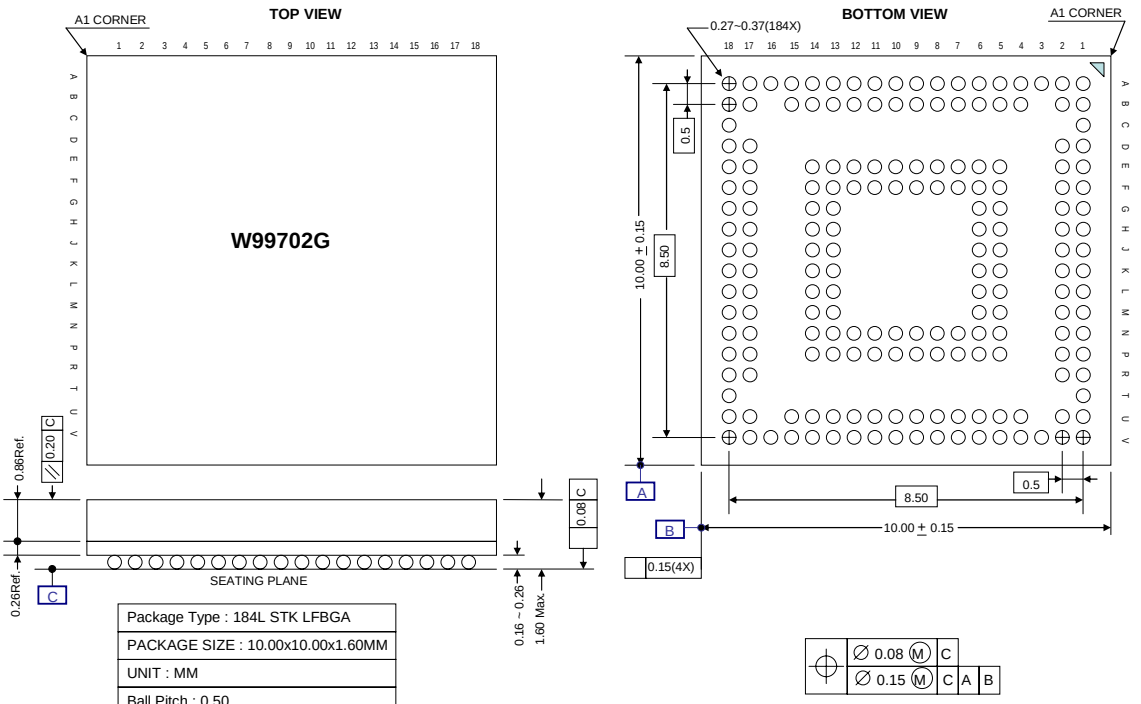
5.4.2 Electrical Characteristics

Conditions: DVDD = 1.2V, AVDD = 2.7V, TA = 30^{o}C, 1KHz Signal, fs = 48 KHz, 16-bit audio data.

PARAMETER	SYM.	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ADC : Analog Input (MIC_IN)						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	V_{INFS}	AVDD = 2.5V		0.707		V_{rms}
Input Resistance			11.2		44.8	Kohm.
Input Capacitance				10		pf
Signal to Noise Ratio	SNR			70		dB
Dynamic Range			90	95		dB
Total Harmonic Distortion	THD			70		dB
Analog Reference Level						
Reference Voltage	VREFC		-3%	1.2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current	-5%	0.9* AVDD	+5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA

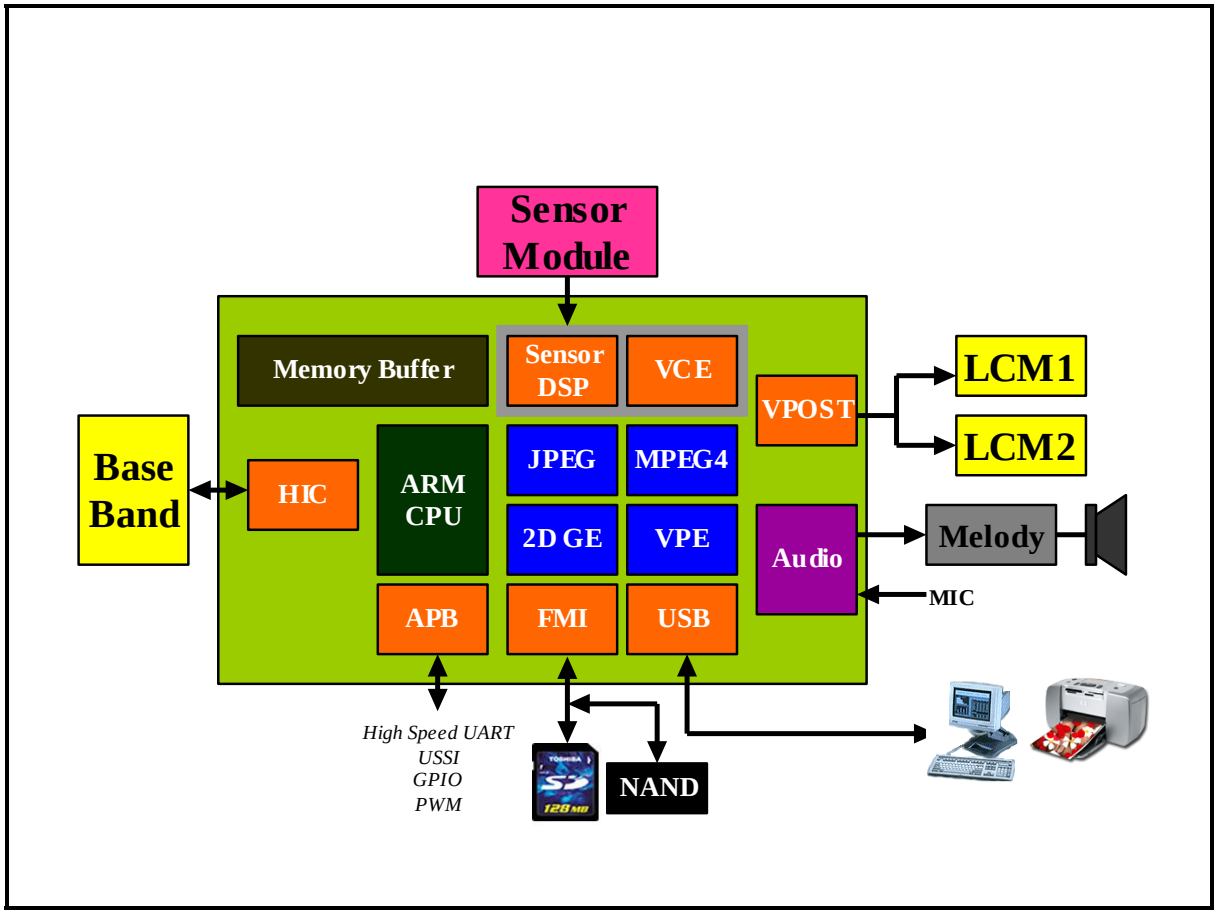
6. PACKAGE DIMENSION

W99702G Package Outline (184L STK LFBGA)



Package Type : 184L STK LFBGA
PACKAGE SIZE : 10.00x10.00x1.60MM
UNIT : MM
Ball Pitch : 0.50
Ball Diameter : 0.3
Substrate Thickness : 0.26
Mold Thickness : 0.86

7. W99702G APPLICATION DIAGRAM



8. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 22, 2004		Preliminary Edition
A2	Aug. 3, 2005		Publication release initial
A3	Oct. 3, 2005	13, 17	Update GPIO description and VDDB spec.
A4	Dec. 28, 2005	17	Update AVDDP, VDDI

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