W55VG680

TV ENCODER

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1. GENERAL DESCRIPTION

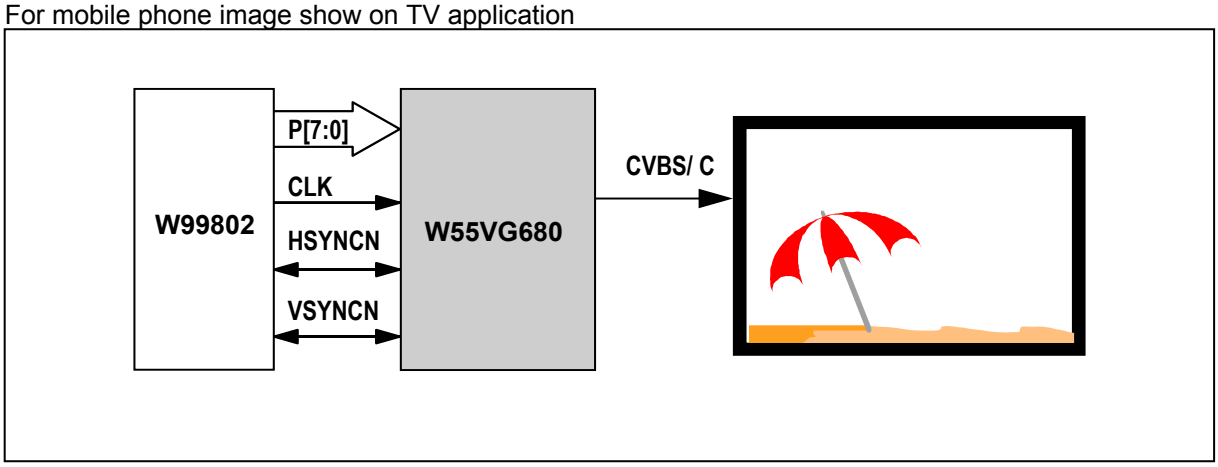
The W55VG680 digital video encoder converts YCrCb (4:2:2) 8-bit data into analog composite video and Y/C video signals. The video format is 525-line (M) NTSC/PAL or 625-line (B, D, G, H, I, M, Nc) PAL. The W55VG680 can operate at master or slave mode. The data rate can be CCIR601 or square pixel. At slave mode, the W55VG680 can auto detect the input video format from the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins and generates the corresponding video signals. At master mode, it generates the required video timing internally according to the configuration.
The input YCrCb data are converted into YUV signals. The chroma data are then low passed by a 1.3 MHz filter and modulated by a color subcarrier. The W55VG680 operates with a 2X pixel rate input.
The W55VG680 has two DAC outputs which can output two composite video or Y/C S-video signal.
The W55VG680 can operate at power-down mode by selecting the SLEEP pin. The W55VG680 is designed for digital video applications such as VCD, DVD, and video games.

2. FEATURES

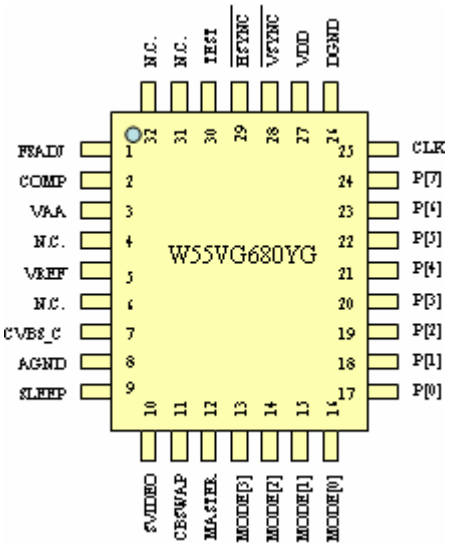
- Monolithic CMOS process
- Master clock rate 2X pixel rate
- Two composite outputs or Y/C video output (S video)
- Power-down mode
- CCIR601 or square pixel input data rates
- Master/slave sync signal switchable
- Interlaced and non-interlaced operation
- Optional internal voltage reference

3. APPLICATION

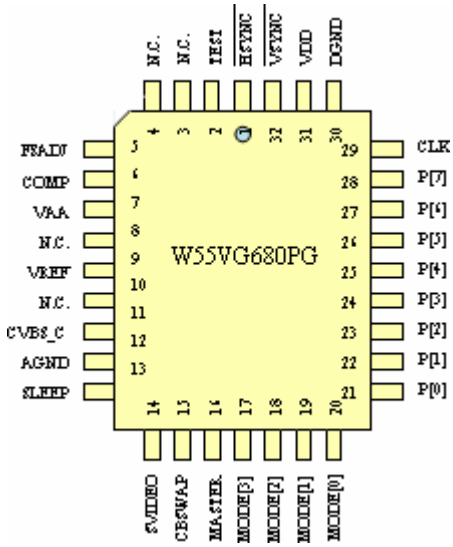
For mobile phone image show on TV application



4. PIN ARRANGEMENT



QFN package



PLCC package

5. PIN DESCRIPTION

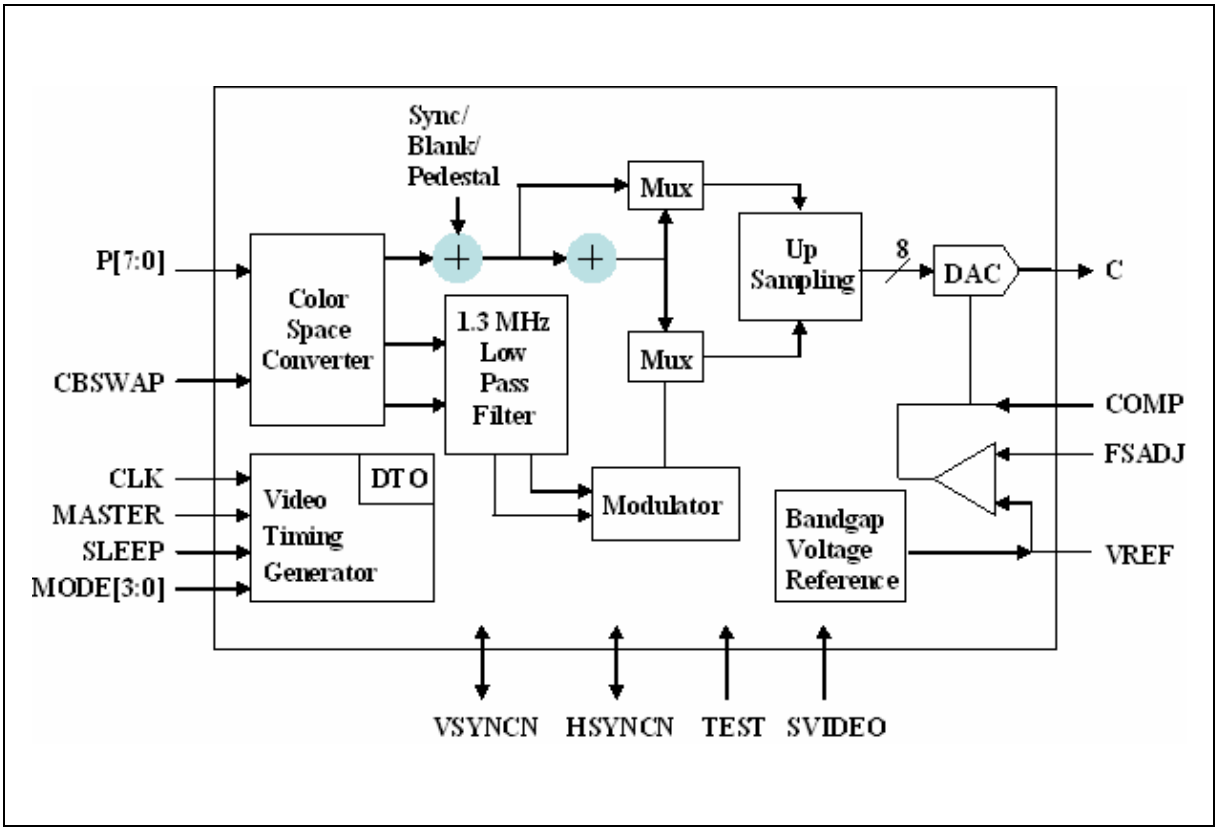
(All digital pins are TTL compatible)

PLCC PIN NO.	QFN PIN NO.	PIN NAME	I/O	DESCRIPTION
1	29	$\overline{\text{HSYNC}}$	I/O	Horizontal synchronization input/output. In master mode, this pin generates vertical synchronizations signal from internal. In slave mode, the signals are from external. HSYNCN is latched/output following the rising edge of CLK.
2	30	TEST	I	Test pin. These pins must be connected to DGND.
3, 4, 8, 10	4, 6, 31, 32	N.C.	---	No connection.
5	1	FSADJ	---	Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground. The relationship is $\text{Re}\ xt\ (\Omega) = 4080\ * VREF\ \ (V) / Iout\ \ (mA)$
6	2	COMP	---	Compensation pin. A 0.1uF ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
7	3	VAA	---	Analog power pin
9	5	VREF	I/O	Voltage reference output. It generates typical 1.2V for internal voltage reference. A 0.1uF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close as possible to minimize the length of the load.
11	7	CVBS_C	O	Composite/Chroma output. This is a high impedance current source Output. The output format can be selected by the PAL pin. The pin can drive a 37.5 mW load. If unused, this pin must be connected directly to GND.
12	8	AGND	---	Analog ground pin
13	9	SLEEP	I	Power save mode. A logical high on this pin puts the chip into power-down mode.
14	10	SVIDEO	I	SVIDEO select input pin. A logical high selects Y output. A logic low selects composite video output.
15	11	CBSWAP	I	Cr and Cb pixel sequence set up pin. A logical high swap the Cr and Cb sequence.

Pin Description, continued.

PLCC PIN NO.	QFN PIN NO.	PIN NAME	I/O	DESCRIPTION
16	12	MASTER	I	Master/slave mode select. A logical high for master mode operation. A logical 0 for slave mode operation
17-20	13-16	Mode[3:0]	I	Mode configuration pin.
21-28	17-24	P[0:7]	I	YCrCb pixel inputs. They are latched on the falling edge of CLK. YCrCb input data conform to CCIR 601.
29	25	CLK	I	2XPixel clock input for 8-bit YCrCb data.
30	26	DGND	---	Digital ground pin
31	27	VDD	---	Digital power pin
32	28	$\overline{\text{VSYNC}}$	I/O	Vertical synchronization input/output. In master mode, this pin generates vertical synchronizations signal from internal. In slave mode, the signals are from external. VSYNCN is latched/output following the rising edge of CLK.

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

7.1 Input formatting

The input circuitry accepts 8-bit CCIR601 4:2:2 YCrCb data . The data are input via the P[7:0] inputs and latched on the falling edge of CLK.

The input YCrCb pixel sequence can be arranged by setting the CBSWAP pin and the YCSWAP mode register. If the CBSWAP pin and the YCSWAP mode register are all zero, the first pixel data latched by the CLK pin after the falling edge of HSYNCN is Cb. The sequence appears as Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 .... This can be swap by setting the CBSWAP pin and the YCSWAP mode register.

The input clock rate can be CCIR601 2X13.5MHz or square pixel rate . Color burst frequency is derived from the CLOCK input. Any jitter on the CLOCK pin may induce a color burst frequency error. A stable clock source is recommended.

The Y of the 16-bit YCrCb data has nominal range from 16-235 and Cr/Cb has a nominal range from 16-240, with 128 equal to zero. When the Y value is between 1-15, the internal circuit will clamp these values to 16. When the Y value is 0 and 255, the internal circuit will set the Y value as 38. When the Cr/Cb is between 1-15, the internal circuit will clamp these values to 16. When the Cr value is 0 and 255, the internal circuit will set the Cr value as 112. When Cb value is 0 and 255, the internal circuit will set the Cb value as 225. Thus when the external video source is reset to 0 or 255, the color at video output will appear blue.

7.2 Mode selection

There are 7 mode registers which can be programmed by setting the four MODE[3:0] pins and the MASTER pin. The following table illustrates the arrangement of the 7 mode registers.

PIN DESCRIPTION				
THE MASTER PIN	**MODE[3]**	**MODE[2]**	**MODE[1]**	**MODE[0]**
0	YCSWAP	SETUP	PALSA	--
1	EFIELD	PAL625	INTERLACED	SQUARE

MODE REGISTER NAME	SET TO 0	SET TO 1	COMMENTS
EFIELD	The VSYNCN pin will output field signal. Low at VSYNCN pin for even field, high for odd field	The VSYNCN pin will output normal vertical synchronization signal.	Master mode only.
PAL625	525-line operation will be select	The 625-line operation will be select	Master mode only.
INTERLACED	Non-interlace operation will be select	The interlace operation will be select	Master mode only.
SQUARE	CCIR-601 timing is selected.	The square pixel timing is selected.	Master mode only.

Continued.

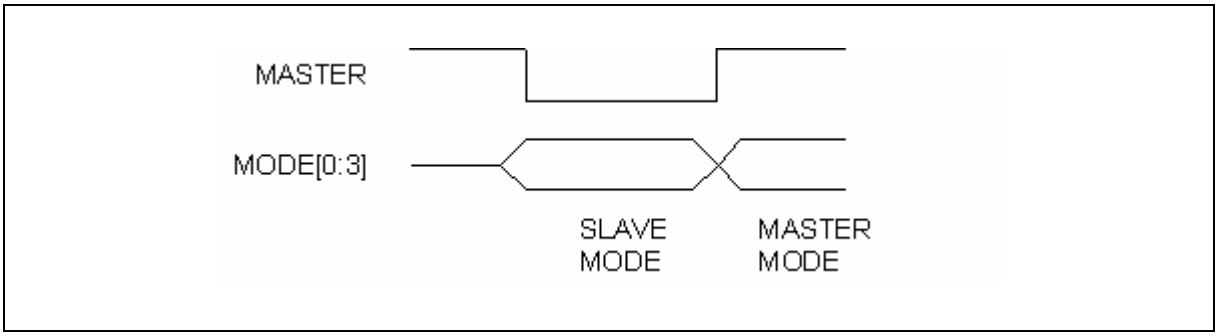
MODE REGISTER NAME	SET TO 0	SET TO 1	COMMENTS
YCSWAP	Do not swap Y and Cr/Cb	Swap Y and Cr/Cb sequence	Slave mode only.
SETUP	Disable the 7.5 IRE setup	Enable the 7.5 IRE setup	Slave mode only.
PALSA	When PAL625 register is set to high, PAL-BDGHI mode is selected. When PAL625 register is set to low, NTSC mode is selected.	When PAL625 register is set to high, PAL-Nc mode is selected. When PAL625 register is set to low, PAL-M mode is selected.	Slave mode only.

At slave mode, the W55VG580 will automatically detect the input video timing. The EFIELD, PAL625, INTERLACE, and SQUARE register will not be necessary. **W55VG680 will not generate synchronization signals which are from external. The control timing, for the detail, please reference table 2.**

At master mode, the MODE[3:0] pins will set EFIELD, PAL625, INTERLACED and SQUARE registers.

The YCSWAP, SETUP, and PALSA registers can be programmed by switching the W55VG580 to slave mode, then back to the master mode. At power-on, the YCSWAP, SETUP, and PALSA are set to zero. **For example, please reference the waveform of notice as below, the EFIELD, PAL625, INTERLACE, and SQUARE can be set when master pin go low, and the internal register will latch the setting data.**

Note: Configure waveform



7.3 The Relationship between TV System and Bit allocation

BITS[3:0]={ PALSA, PAL625, SQUARE, INTERLACE }
FL: Line Rate
FP: Pixel Rate
FSC: Sub-carrier Frequency

BITS[3:0]	FORMAT	PIXEL X LINE	FL	FP	FSC
0	M/NTSC, 601, NI	858x262	15734.264	13500000	3579545.00
1	M/NTSC, 601, I	858x525	15734.264	13500000	3579545.00
2	M/NTSC, S, NI	780x262	15734.264	12272727	3579545.00
3	M/NTSC, S, I	780x525	15734.264	12272727	3579545.00
4	BDGHIN/PAL, 601, NI	864x312	15625.000	13500000	4433618.75
5	BDGHIN/PAL, 601, I	864x625	15625.000	13500000	4433618.75
6	BDGHIN/PAL, S, NI	944x312	15625.000	14750000	4433618.75
7	BDGHIN/PAL, S, I	944x625	15625.000	14750000	4433618.75
8	M/PAL, 601, NI	858x262	15734.264	13500000	3575611.49
9	M/PAL, 601, I	858x525	15734.264	13500000	3575611.49
A	M/PAL, S, NI	780x262	15734.264	12272727	3575611.49
B	M/PAL, S, I	780x525	15734.264	12272727	3575611.49
C	Nc/PAL, 601, NI	864x312	15625.000	13500000	3582056.25
D	Nc/PAL, 601, I	864x625	15625.000	13500000	3582056.25
E	Nc/PAL, S, NI	944x312	15625.000	14750000	3582056.25
F	Nc/PAL, S, I	944x625	15625.000	14750000	3582056.25

7.4 Color Space Conversion

The 8-bit 4:2:2 YCrCb data input are linearly interpolated to 4:4:4 format and then converted to YUV format.

7.5 Low-Pass Filter

The U/V signal is low passed by a digital filter specified by CCIR 624.

7.6 Modulator

The U and V color difference signals are modulated by a **sub-carrier** frequency generated by an internal DTO. After modulation, they are summed together to produce luminance signal.

7.7 Video Timing

The W55VG680 can operate in master mode and slave mode. This is done by setting the MASTER pin. When the MASTER pin is set to logical low, the W55VG580 operates at slave mode. When The MASTER pin is set to logical high, the W55VG680 operates at master mode.
At master mode, the W55VG680 automatically generates the required timing from the CLK input. The HSYNCN and VSYNCN pins are output following the rising edge of CLK. Coincident falling edges of HSYNCN and VSYNCN indicates the beginning of an odd field. A falling edge of VSYNC without a coincident falling edge of HSYNCN indicates the beginning of an even field.
At slave mode, the W55VG680 accepts external horizontal and vertical synchronization signals via the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins and automatically detects the input video format. The W55VG680 then generates the detected video timing.
The W55VG680 automatically calculates the width of the horizontal sync pulse and the start and end of color burst. Color burst is automatically disabled on appropriate lines. Serration and equalization pulses are automatically inserted into appropriate lines.

7.8 Video and Burst Blanking

Video and burst information is automatically disabled according to the Rec. CCIR624.

7.9 Power Down

When the SLEEP pin is logical high, the W55VG680 enters sleep mode. The clock input and DAC outputs are disabled.

7.10 Analog outputs

The output, CVBS_C is an 8-bit D/A converter outputs. This output is specified to drive 37.5 loads. When the SVIDEO pin is connected to high, CVBS_C will output signal which can be interface to the S-Video machine. When the SVIDEO pin is connected to low, the CVBS_C will output composite video.

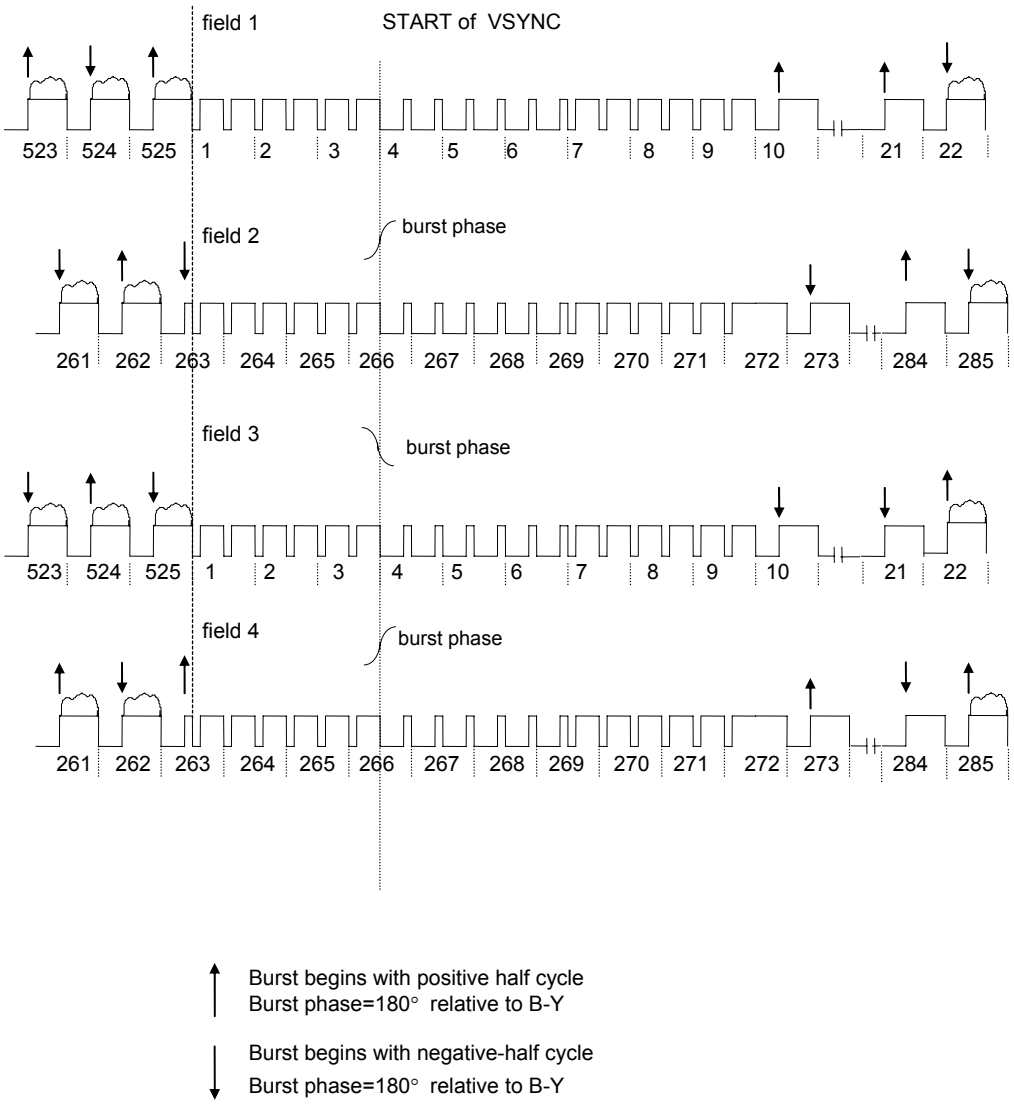


Figure 1. NTSC Interlace Video Timing
(SMPTE line conversion rather than CCIR-624 is used)

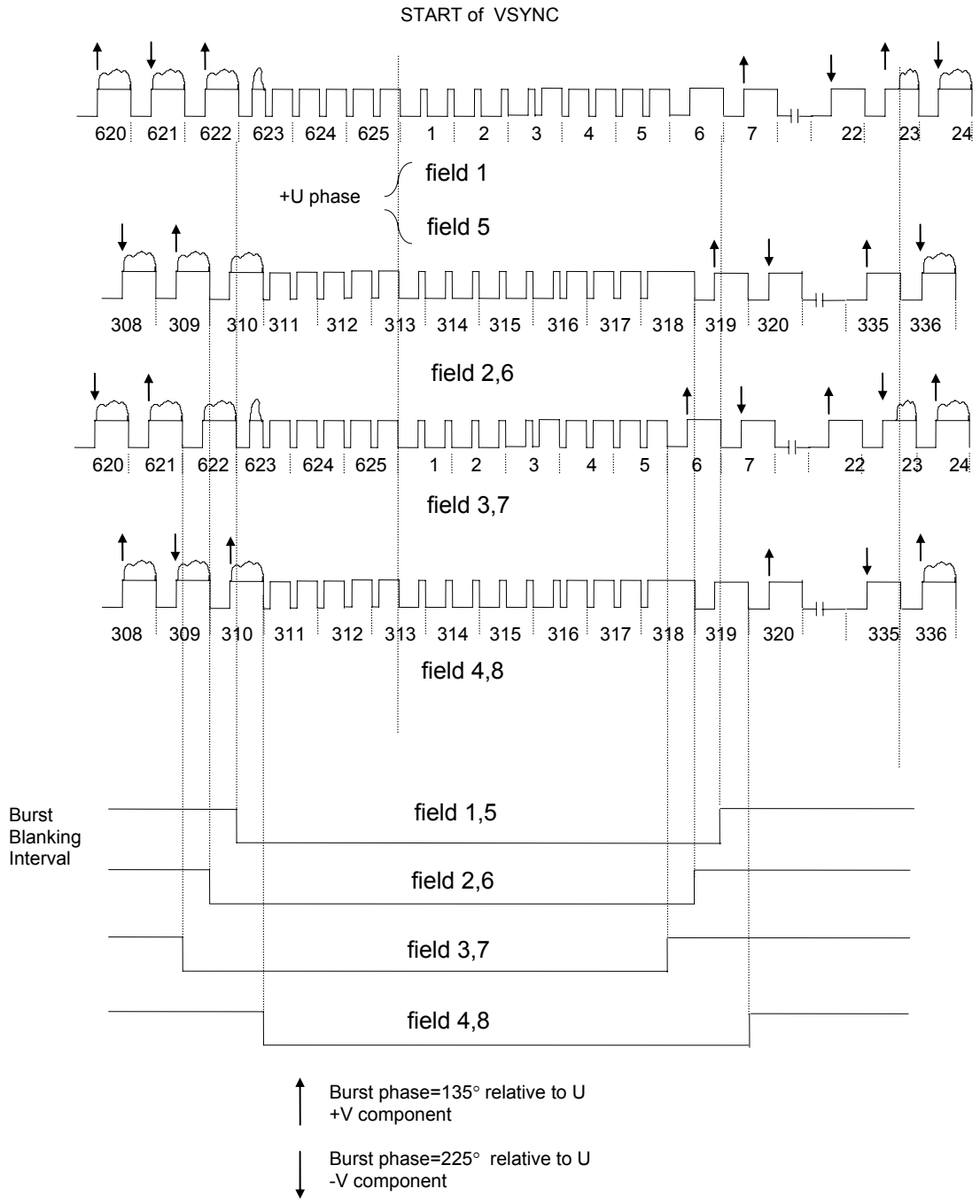


Figure 2. B,D,G,H,I/PAL Interlace Video Timing

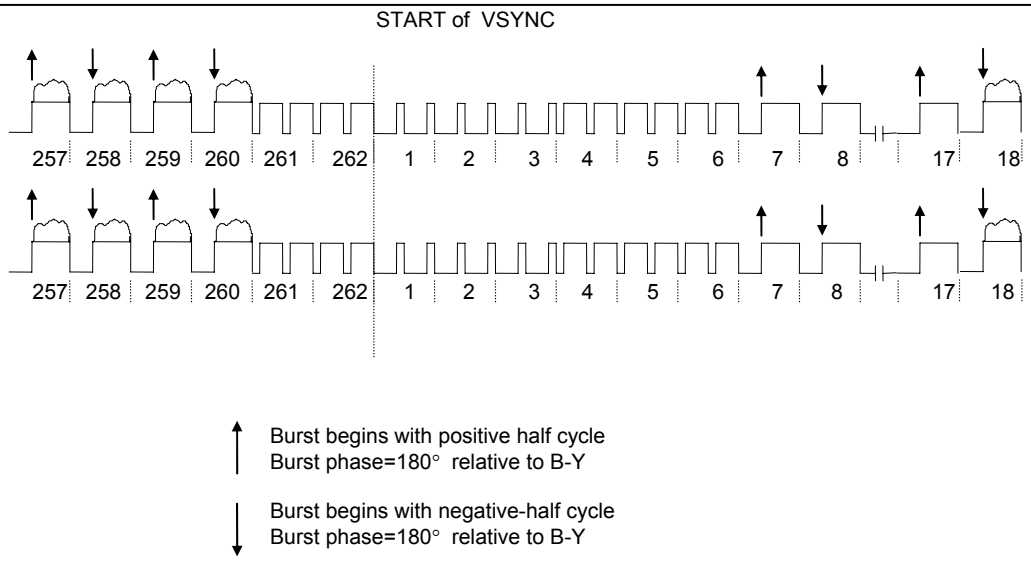


Figure 3. NTSC Non-interlace Video Timing

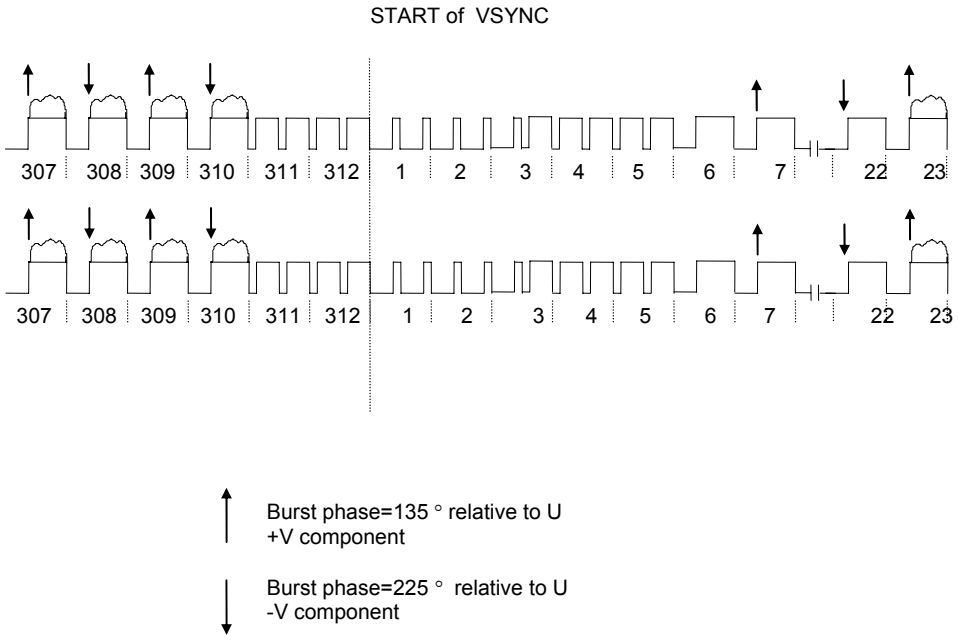


Figure 4. PAL Non-interlace Video Timing

8. ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply	VAA	**3.0**	**3.30**	**3.6**	V
Ambient Operating Temperature	TA	0	--	70	°C
DAC Output Load	RL	50	--	--	
External Voltage Reference	VREF	1.245	1.275	1.295	V

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply (Measured to ground)	VAA	--	--	**3.6**	V
Ambient Operating Temperature	TA	-55	--	125	°C
Voltage on Any Signal Pin	--	GND-0.5	--	VAA+0.5	V
Storage Temperature	TS	-65	--	+150	°C
Junction Temperature	TJ	--	--	+150	°C

Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latch up.

9. DC CHARACTERISTICS

(Recommended operating conditions using external voltage reference with RSET=**180** Ω , VREF=1.275V, NTSC CCIR601 operation and clock frequency= 27 MHz at 25°C , +5V)

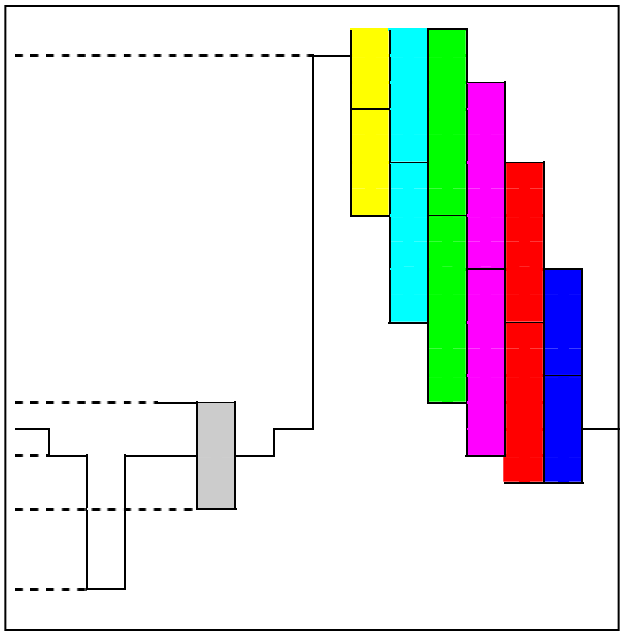
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VAA Supply Current	IAA@ 70°C IAA@ 0°C	-	**50** **50**	tbd tbd	mA mA
Video D/A Resolution	-	8	8	8	Bits
Integral Nonlinearity	INL	-	-	+/- 1	LSB
Differential Nonlinearity	DNL	-	-	+/- 1	LSB
Maximum Output Current	-	-	-	26.04	mA
Output Compliance	VOC	0	-	1.5	V
Video level Error					
Using External Reference	-	-	-	5	%
Using Internal Reference	-	-	-	10	%
Full-Scale DAC Output	-	-	182.5	-	IRE
Digital Inputs	-	-	-	-	
Input High Voltage	VIH	2.0	-	VAA+0.5	V
Input Low Voltage	VIL	GND-0.5	-	0.8	V
Input High current (Vin=2.4V)	IIH	-	-	1	uA
Input Low current (Vin=0.4V)	IIL	-	-	-1	uA
Digital Outputs					
Output High Voltage (IOH=-400uA)	VOH	2.4	-		V
Output Low Voltage (IOL=3.2mA)	VOL	-	-	0.4	V
Three-State Current	IOZ	-	-	50	uA
VREF Output Voltage	VREF	1.064	1.275	1.298	V
VREF Output current	IREF	-	10	-	uA

10. AC CHARACTERISTICS

(Recommended operating conditions using external voltage reference with RSET=180 Ω , VREFIN=1.235V, NTSC CCIR601 operation and clock frequency=27 MHz at 25 ℃, +5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Luminance Bandwidth	-	-	Fin/4	-	MHz
Chrominance Bandwidth	-	-	1.3	-	MHz
Differential Gain	-	-	1	-	%
Differential Phase	-	-	1	-	
SNR	-	-	60	-	dB
Hue Accuracy	-	-	1.5	3	
Color Saturation Accuracy	-	-	1.5	3	%
Analog Output Delay	5	-	30	-	ns
Analog Output Rise Time	-	-	3	-	ns
Analog Output Settling Time	-	-	30	-	ns
Pixel/Control Setup Time	1	0	-	-	ns
Pixel/Control Hold Time	2	6	-	-	ns
Control Output Delay Time	3	-	15	-	ns
CLOCK Frequency	Fin	24.54	27	29.5	MHz
CLOCK Pulse Width Low Time	-	10	-	-	ns
CLOCK Pulse Width High Time	-	10	-	-	ns
Pipeline Delay	4	-	28	-	Clocks

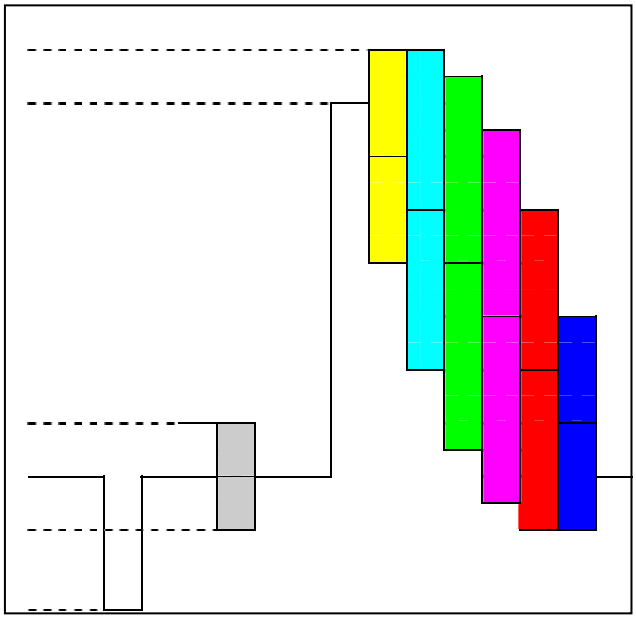
Color/Level	HSYNC	BLANK	mA	V	IRE
Peak Chroma	1	1	33.06	1.240	134
White	1	1	27.22	1.021	100
Peak Burst	1	1	11.97	0.449	20
Black	1	1	9.6	0.360	7.5
Blank	1	0	8.16	0.306	0
Peak Burst	1	0	4.37	0.164	-20
SYNC	0	0	0.53	0.020	-40



Note: 37.5 Ω load is used. VREF = 1.275V, RSET = 180 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

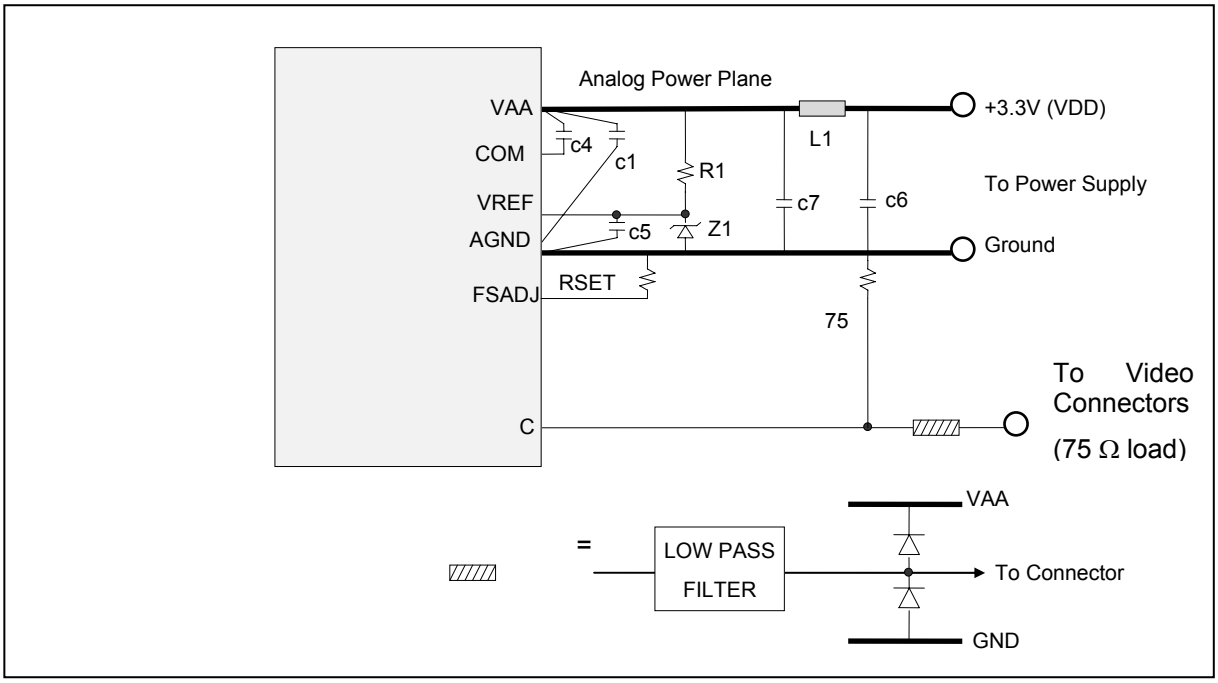
Figure 5. NTSC Composite Output Waveform

Color/Level	HSYNC	BLANK	mA	V	IRE
Peak Chroma	1	1	34.16	1.281	133
White	1	1	27.76	1.041	100
Peak Burst	1	1	12.8	0.480	21.5
Black/Blank	1	0	8.72	0.327	0
Peak Burst	1	0	4.64	0.174	-21.5
SYNC	0	0	0.53	0.02	-43



Note: 37.5 Ω load is used. VREF = 1.275V, RSET = 180Ω. 100% amplitude, 100% saturation are shown. CCIR 624 levels and tolerance are assumed.

Figure 6. PAL-BDGHI Composite Output Waveform



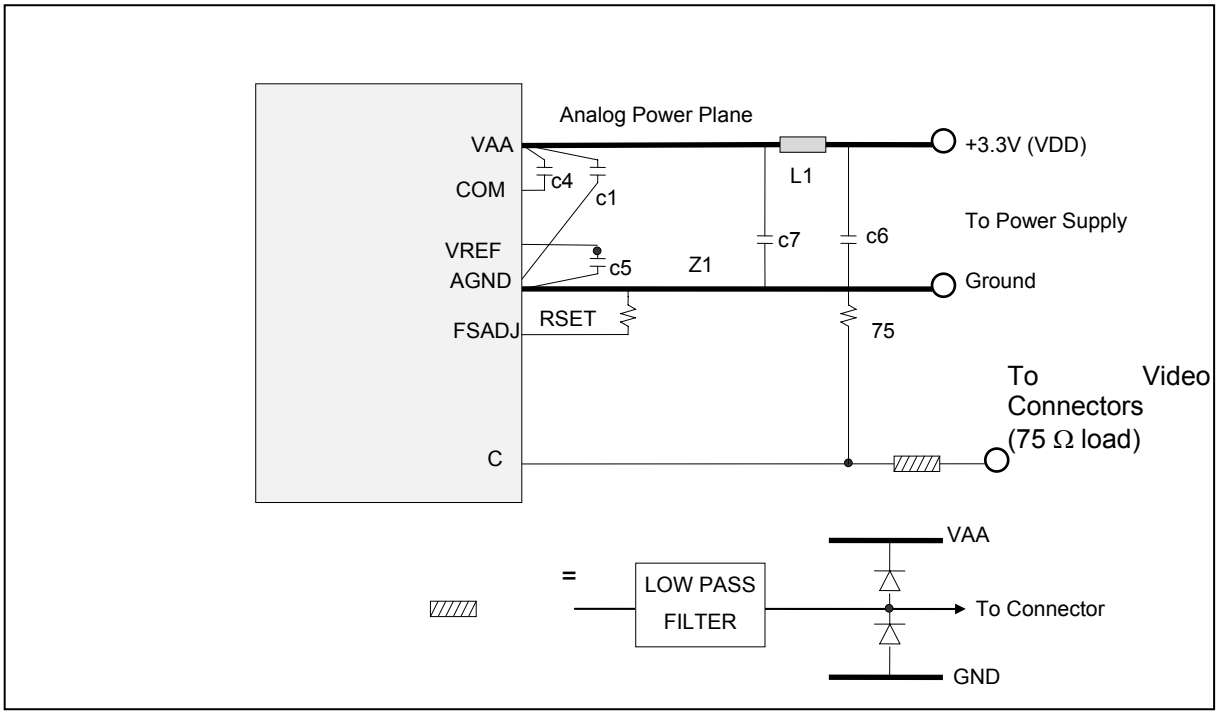
PART NUMBER	VALUE	VENDOR NUMBER
c1, c4, c5, c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
R1	1KW (5%)	
RSET	1% Metal Film	Dale CMF-55C
Z1	1.2V Zener Diode	LM358BZ-1.2

Note: 1. The vendor number is only for reference.

2. RSET is determined by (Iout=full scale output current)

$$\mathrm{Re}\,xt\,(\Omega) = 4080 * VREF\ (V) / Iout\ (mA)$$

Figure 7. Typical connection diagram and part list (using external voltage reference)



PART NUMBER	VALUE	VENDOR NUMBER
c1, c4, c5, c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
RSET	1% Metal Film	Dale CMF-55C

Note: 1. The vendor number is only for reference.

2. RSET is determined by (Iout=full scale output current)

$$\mathrm{Re}\ xt\ (\Omega) = 4080\ * VREF\ \ (V) / Iout\ \ (mA)\ \ \mathrm{Re}\ xt\ (\Omega) = 4080\ * VREF\ \ (V) / Iout\ \ (mA)$$

Figure 8. Typical connection diagram and part list (using internal voltage reference)

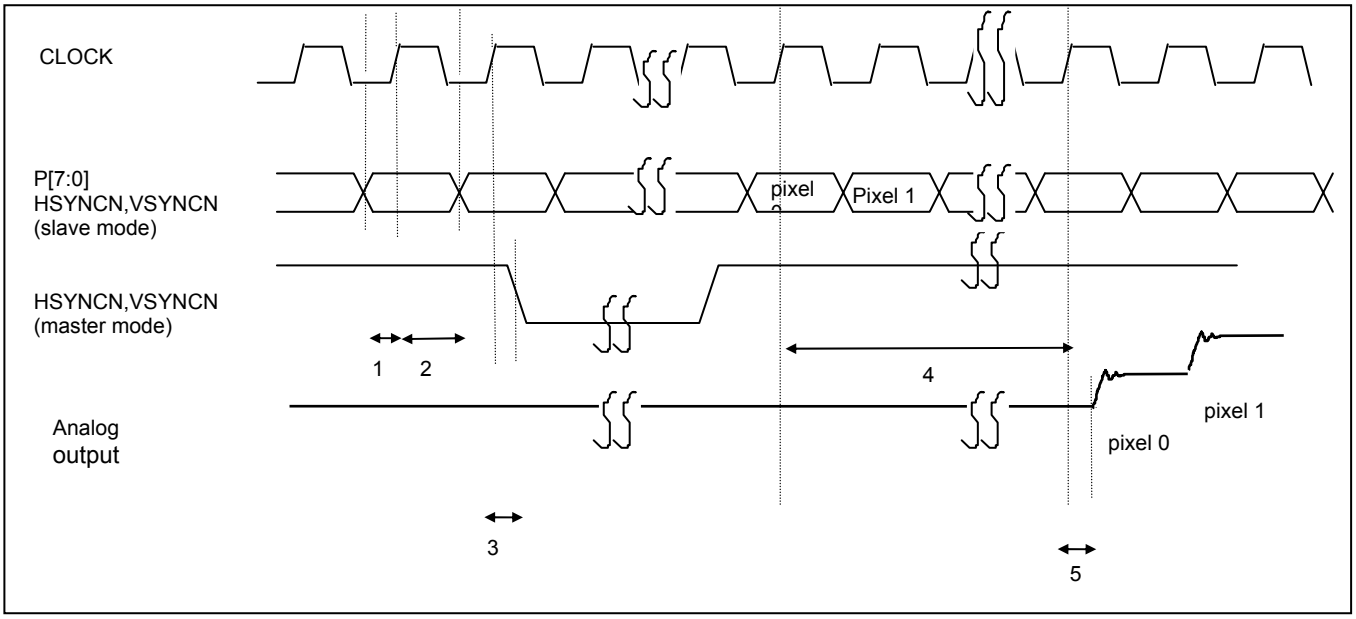


Figure 9. Video Input and Output Timing

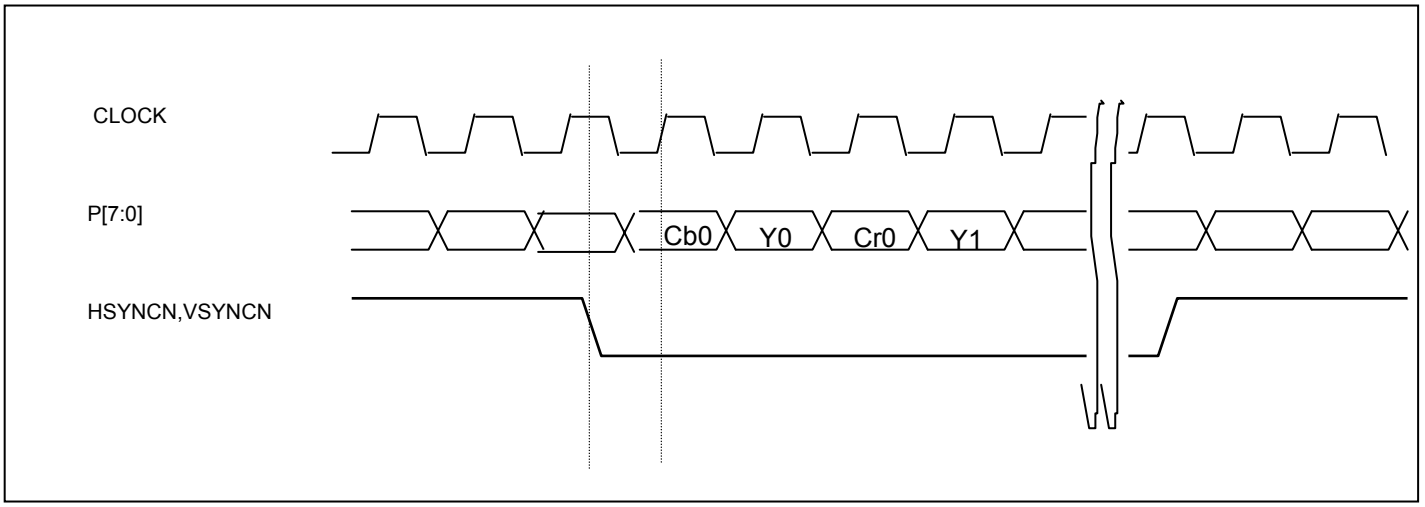


Figure10. Pixel sequence at power on reset (The pixel sequence can be swap by setting the CBSWAP pin and the MODE[3] pin at slave mode)

Table1. Field Resolution and clock Rates for Various Modes of Operation

OPERATING MODE	ACTIVE PIXELS	TOTAL PIXELS	CLK FREQUENCY (MHZ)
NTSC/PAL-M CCIR601	720 x 240	858 x 262	27
PAL-B,D,G,H,I,Nc	720 x 288	864 x 313	27
NTSC/PAL-M Square pixel	640 x 240	780 x 262	24.545454
PAL-B,D,G,H,I,Nc Square pixel	768 x 288	944 x 312	29.5

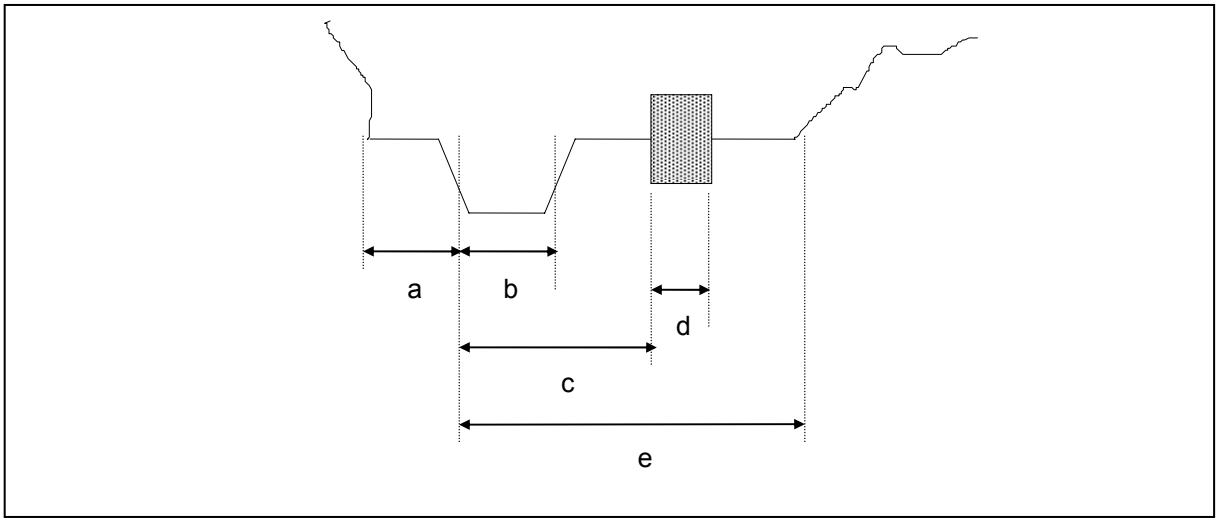


Table2. Various Video Timing

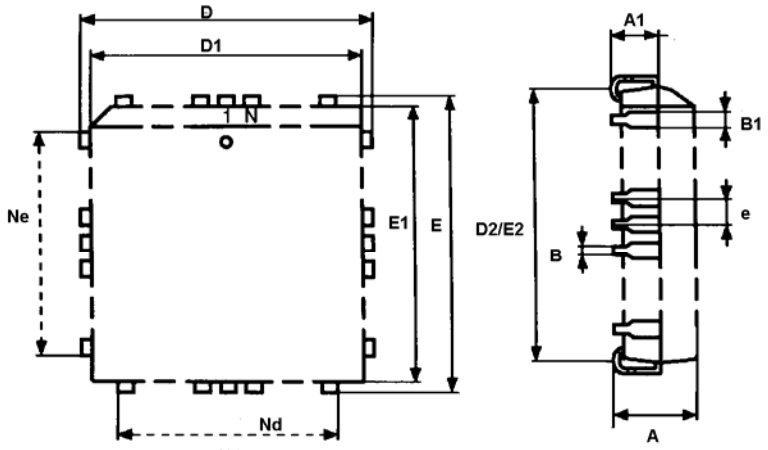
OPERATION MODE	FRONT PORCH (E)	HORIZONTAL SYNC WIDTH (B)	START OF BURST (C)	DURATION OF BURST (D)	BACK PORCH (E)
NTSC CCIR601	20	63	72	34	127
PAL-M CCIR610	20	63	78	34	127
PAL-B CCIR601	20	63	76	30	142
PAL-Nc CCIR601	20	63	76	34	142
NTSC SQUARE	18	58	65	31	115
PAL-M SQUARE	18	58	71	31	115
PAL-B SQUARE	22	69	83	33	155
PAL-Nc SQUARE	22	69	83	37	155
Notes: (1) The unit is the number of luminance pixel.					

11. PACKAGE INFORMATION

TYPE NUMBER	PACKAGED	AMBIENT TEMPERATURE RANGE	NOTE
W55VG680YG	QFN-32	0~70 °C	Lead-Free
W55VG680PG	PLCC-32	0~70 °C	Lead-Free
W55VG680H	Chip form	0~70 °C	---

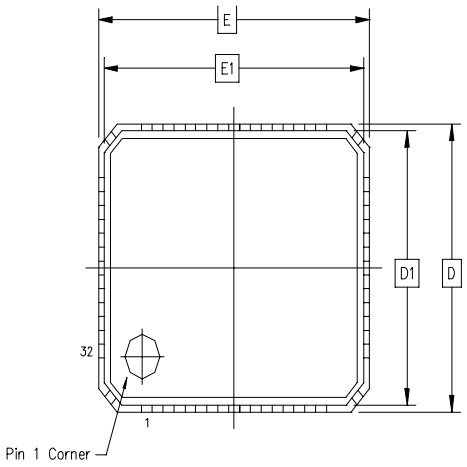
12. PACKAGE DIMENSION

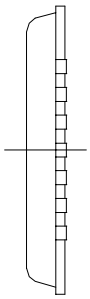
12.1 PLCC

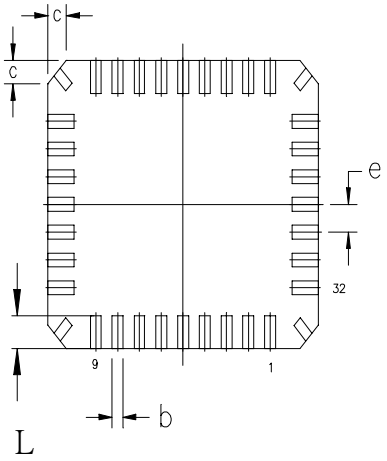


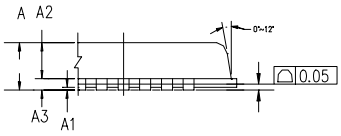
SYMBOL	INCHES			MM		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.1		0.14	2.54		3.56
A1	0.06		0.095	1.52		2.41
B	0.013		0.021	0.33		0.53
B1	0.026		0.032	0.66		0.81
D	0.485		0.495	12.32		12.57
D1	0.447		0.455	11.35		11.56
D2	0.39		0.43	9.91		10.92
E	0.585		0.595	14.86		15.11
E1	0.547		0.555	13.89		14.1
E2	0.49		0.53	12.54		13.46
e		0.05			1.27	
N					32	
Nd					7	
Ne					9	

12.2 QFN-32





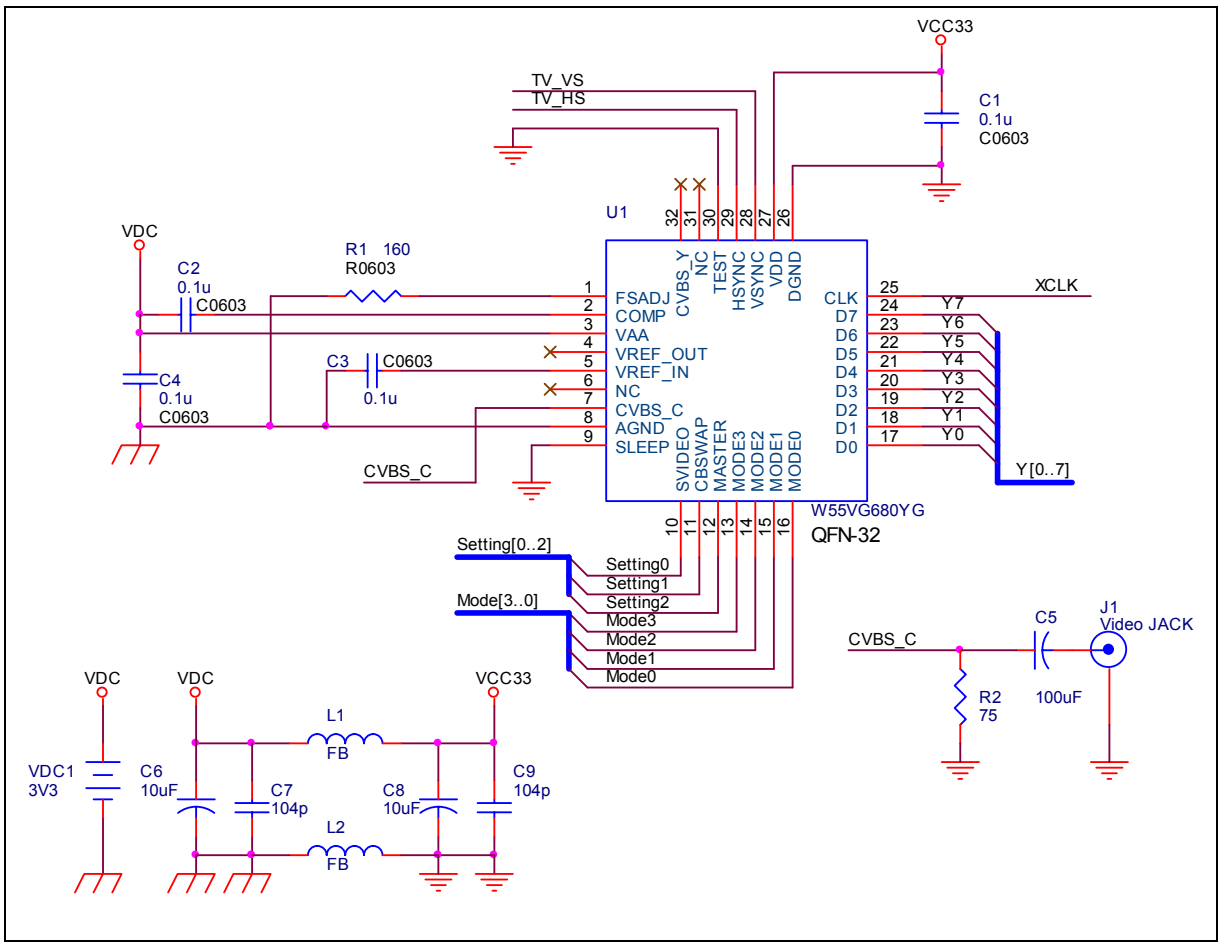




Cotrol Dimensions :Millmeters

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	---	1.00	0.0314	---	0.0394
A1	0.00	0.02	0.05	0.0000	0.0007	0.0019
A2	0.65	---	0.69	0.0255	---	0.0271
A3	0.203 REF.			0.0079 REF.		
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
C	0.24	0.42	0.60	0.0094	0.0165	0.0236
D	5.20 BSC			0.2047 BSC		
D1	4.95 BSC			0.1948 BSC		
E	6.20 BSC			0.2440 BSC		
E1	5.95 BSC			0.2342 BSC		
e	0.50 BSC			0.0196 BSC		
L	0.50	0.60	0.70	0.0196	0.0236	0.0275

13. APPLICATION CIRCUIT



14. BILL OF MATERIAL

Item	Q'ty.	Ref.	Value
1	4	C1,C2,C3,C4	0.1u
2	1	C5	100uF
3	2	C8,C6	10uF
4	2	C7,C9	104p
5	1	J1	Video JACK
6	2	L1,L2	FB
7	1	R1	160
8	1	R2	75
9	1	U1	W55VG680YG
10	1	VDC1	3V3

15. DOCUMENT HISTORY

DATE	REVISION	EDITOR	COMMENTS
01/27/2005	A1	Cliff Huang	Original issue
02/23/2005	A1.1	Cliff Huang	Data pin re-arrangement correct.
03/20/2005	A1.2	Cliff Huang	Update Application content and QFN package dimension.
04/13/2005	A1.3	Cliff Huang	Remove out PLCC packaged.
06/08/2005	A1.4	Cliff Huang	1. Changed Vref_in to Vref. And typical value is changed to 1.275 from 1.235V. 2. Change Rext formula.
09/12/2005	A1.5	Cliff Huang	1. REXT change to 180Ω from 10K. 2. Pin arrangement modified. 3. Modified output driving power, pin 11, as 37.5mW.
05/17/2006	A1.6	Cliff Huang	1. Edit proof. 2. HSYNCN & VSYNCN change to $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$. 3. SVIDEO only Y output. 4. Add Application circuit and Bill of Material.

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