



W55V94 TV-toy Controller

Data Sheet



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1. GENERAL DESCRIPTION

W55V94 is a highly-integrated chip for TV-toy applications. Several devices are embedded in the W55V94, including a 65C816 uC, CRT controller (CRTC), TV encoder, Programmable Sound Generator (PSG) and video mask ROM. Additionally, the Direct Memory Access (DMA) mechanism makes the W55V94 even more powerful in image processing.

2. FEATURES

- 27 MHz X'tal used for 27 MHz system and 6.75 MHz uC clocks.
- Embedded 65C816 uC core and power down mode is supported.
- Five interrupt sources, including Vertical blank, Horizontal blank, I/O port, TimerG and TimerN.
- Direct Memory Access (DMA) mechanism.
- Almost 4 KB of built-in dedicated Program RAM (PRAM) [\$000080 - \$000EFF] and a total of 2,176KB Program ROM (PROM) and Video ROM (VROM).
- Built-in VROM divided into four groups. Each group consists of four 128KB.
- Embedded TV-encoder that supports 320x240 pixel resolution.
- Four programmable color modes: 4/16/64/256 and 16M different colors.
- Fifteen picture layers: Background 0 (BG0), Background 1 (BG1), Sprite x 12 and Text x 1. Layer priority is: Text, Sprite, BG1, Sprite, and BG0: Sprite can be configured to be higher or lower than BG1.
- 8*8 pixel patterns in BG0 and BG1. Both BG0 and BG1 have the scrolling functions and BG0 is divided into 5 planes.
- Additional RAM [\$002000 - \$0029ED] that can be configured to BG1 RAM or PRAM.
- 16x16 pixel patterns in sprite layers. The W55V92 supports 512 different sprites, 96 sprites per frame and maximum 12 sprites per scan line. In addition, each sprite has zoom-in(x2) and mirror functions.
- 8x16 or 16x16 pixel patterns in Text. The W55V92 supports 8 lines of text and 27 characters per line.
- Built-in CMOS sensor interface for image display only.
- Dual tone melody and two-channel noise generator.
- Watch Dog Timer (WDT) configurable using mask option.
- Sixteen bi-directional ports and 8 input ports all built-in.
- Low power 3.0V ~ 3.6V operating voltage.



3. PAD DESCRIPTION

PAD NAME	PAD NO	I/O	DESCRIPTION
IP0[7:0]	62, ..., 55	I	Input port with internal pull-high selection.
BP0[7:0]	10, ..., 3	I/O	Configurable to be input or output port. In output mode, its sink current can up to 8 mA and with the CMOS/open-drain output selection. In input mode, with internal pull-high selection. BP0[7] can be configured to be Infrared (IR) transmission carrier output.
BP1[7:0]	27, ..., 20	I/O	Configurable to be input or output port. In output mode, its sink current can up to 8 mA and with the CMOS/open-drain output selection. In input mode, with pull-high resistor selection.
XIN	16	I	27MHz (within 50 PPM deviation) crystal clock input, external 18pF capacitor suggested.
XOUT	17	O	27MHz crystal clock input, external 18pF capacitor suggested.
TEST	15	I	This pin must be connected VSS.
DAC	54	O	Audio output for external speaker.
PAL/NTSC	28	I	High: PAL video output format Low: NTSC video output format.
COMP	49	O	Composite/Chroma output, the output format can be selected by PAL/NTSC pin. This pin can drive a 37.5 W load. If unused, it shall be connected to AGND.
VREF	48	O	Voltage reference output. It generates typical 1.2V reference voltage and may be used to drive VREF_IN pin directly
CEXT	45	O	For TV-encoder signal compensation concerns, 0.1 uF ceramic capacitor shall be connected to VAA. The lead length shall be kept short as possible to avoid noise.
REXT	44	O	Full-Scale adjust control pin. The Full-Scale current of D/A converter (embedded in TV encoder) can be adjusted by connecting a external resistor between this pin and AVSS. The relationship is: REXT (ohm) = 2015 * VREF (V) / Iout (mA)
RESET	14	I	System hardware reset, internal pull-high
VDD	1, 11, 18, 30, 52		Digital power supply, +3.3V $\pm$ 03V.

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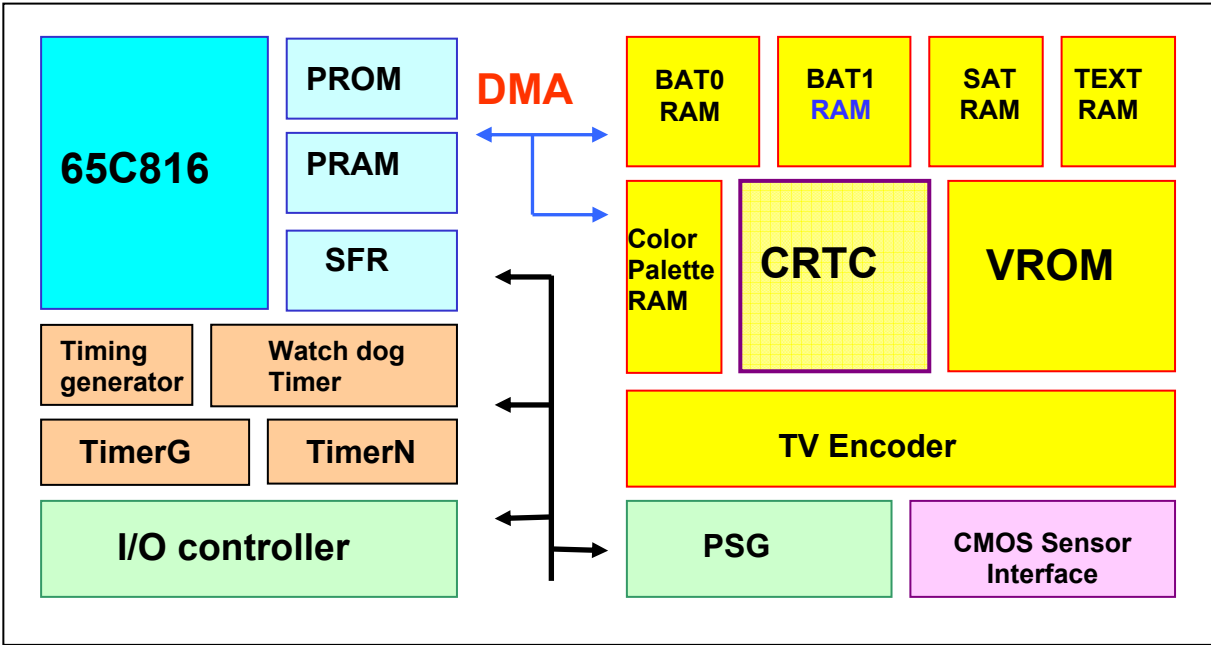


PAD DESCRIPTION, continued.

PAD NAME	PAD NO	I/O	DESCRIPTION
DVDD	42	I	Digital power for TV-encoder, +3.3V $\pm$ 03V.
AVDD1, AVDD2	46, 47	I	Analog power supply, +3.3V $\pm$ 03V
VSS	2, 12, 19, 31, 53	I	Digital ground.
DVSS	43	I	Digital ground for TV-encoder.
AVSS1, AVSS1	50, 51	I	Analog ground.
SCLK	29	O	Clock pin. The main clock output via this pin.
SData [0:7]	32, 33, 34, 35, 36, 37, 38, 39	I	CMOS sensor interface. W55V94 access data which is a 8-bit row data format from CMOS sensor by this interface.
SVsync	41	I	Vertical synchronization signle input pin. Vsync is active low. The vertical signal is from CMOS sensor for verticality synchronize.
SHsync	40	I	Horizontal synchronization signle input pin. Hsync is active low. The horizontal signal is from CMOS sensor should output for Horizon synchronize.
CLK	13	O	27MHz clock output.

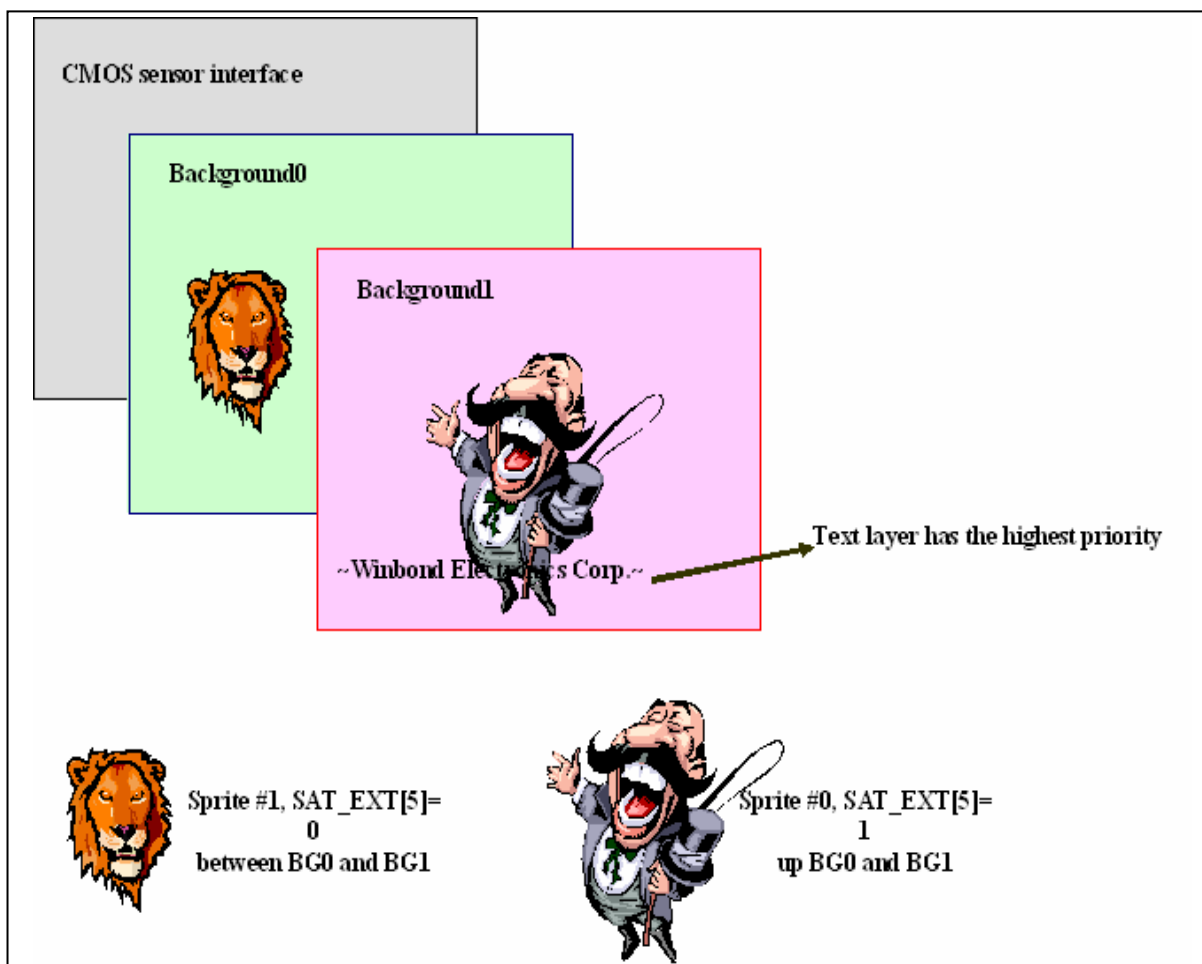


4. BLOCK DIAGRAM



5. LAYER PRIORITY

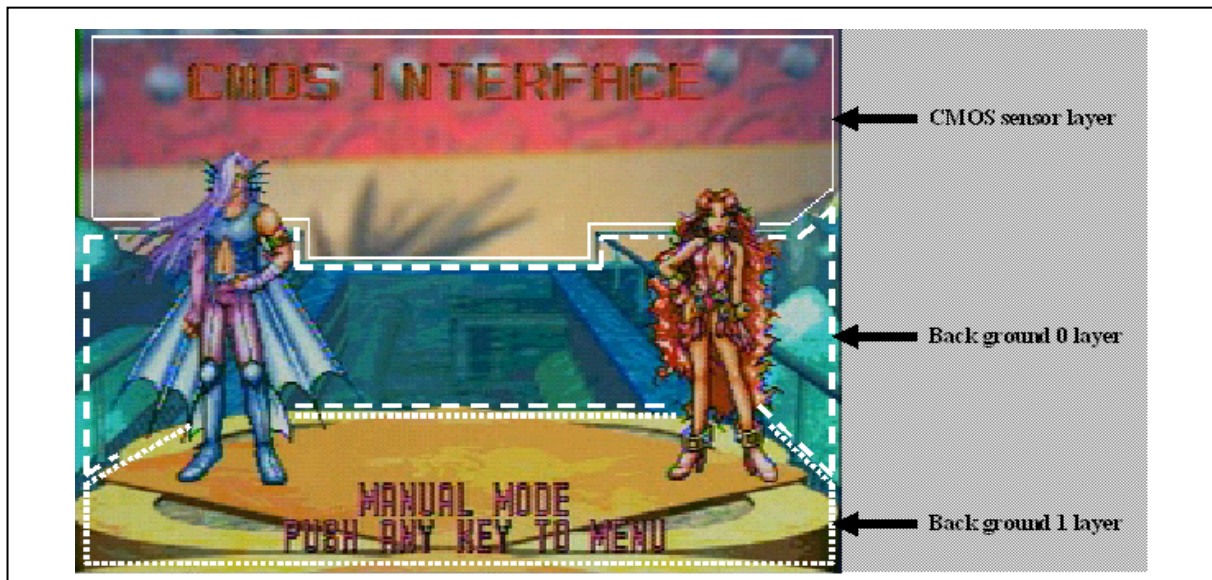
Total 15 picture layers: BG0, BG1, Sprite x 12 and Text x 1 can be displayed. The layer priority is Text > Sprite > BG1 > Sprite > BG0 > CMOS sensor. The priority of Sprite can be changeable by setting register SAT_EXT[5]. The CMOS sensor interface is only supported for NTSC system but not for PAL.



W55V94 Data Sheet



W55V94 support CMOS sensor interface, the image data from CMOS sensor can be displayed on TV directly. **But it doesn't support motion detection function.** The real picture show on TV for each one of layer as below:





6. ABSOLUTE MAXIMUM RATINGS

6.1 DC Characteristics

(VDD-VSS = 3.6V, No load, FOSC = 27 MHz Crystal, T_A = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V _{DD}	-	3.0	-	3.6	V
Operating Current (no Load, no Voice, no Melody)	I _{OP}	-	-	75	80	mA
Standby current	I _{SB}	STOP mode, V _{DD} = 3.3V	-	-	2	uA
Output current BP0	I _{OL}	V _{OUT} = 0.4v, V _{DD} =3.0v	6	-	-	mA
	I _{OH}	V _{OUT} = 2.6v, V _{DD} =3.0v	-6	-	-	
Output current BP1	I _{OL}	V _{OUT} = 0.4v, V _{DD} =3.0v	6	-	-	mA
	I _{OH}	V _{OUT} = 2.6v, V _{DD} =3.0v	-6	-	-	
Positive-going threshold voltage	VT+	VDD = 3.3V, IP0, BP0, BP1 set as input mode.	2.0	2.2	-	V
Negative-going threshold voltage	VT-	VDD = 3.3V, IP0, BP0, BP1 set as input mode.	-	0.8	1	V
Hysteresis	VHYST	VDD = 3.3V, VHYST = VT+ - VT		1.4		V
DAC full-scale current	I _{DAC}	V _{DD} = 3.3 v, 3mA option	2.4	3.0	3.6	mA
		V _{DD} = 3.3 v, 5mA option	4.0	5.0	6.0	
Pull-high resistor Input ports	R _{PH}	IP0	200	-	360	K
		BP0	200	-	360	
		BP1	200	-	360	
		RESET	200	-	360	
Pull-low resistor	R _{PL}	Sensor_data	85	-	-	K



6.2 AC Characteristics

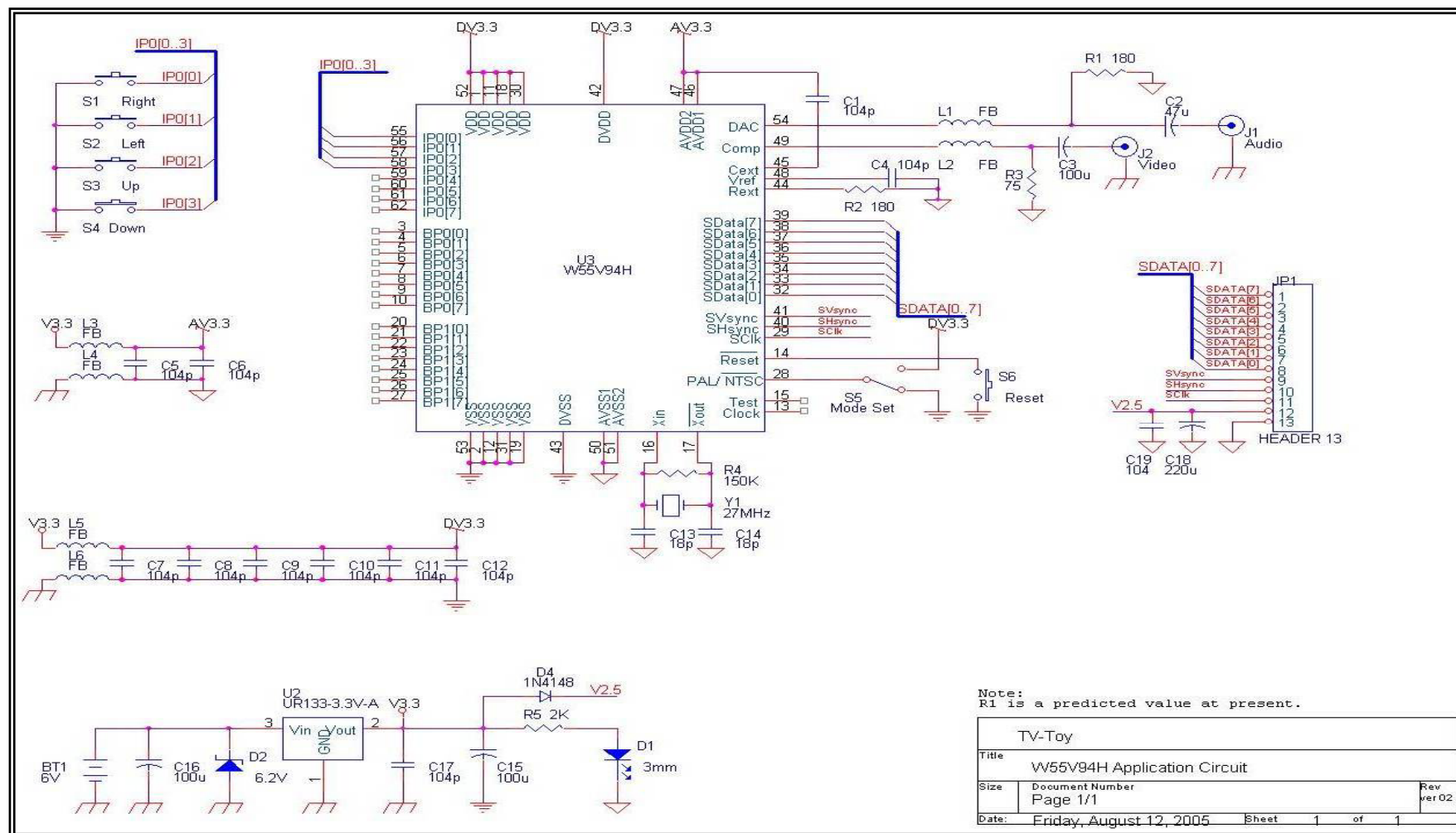
PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Main clock wakeup delay	WDm	-	-	3	5	mS

6.3 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond the listed value may affect the life and reliability of the device.

7. APPLICATION CIRCUIT



W55V94 Data Sheet



Bill Of Materials

Item	Quantity	Reference	Part
1	1	BT1 6V	
2	11	C1,C4,C5,C6,C7,C8,C9,C10, C11,C12,C17	104p
3	1	C2	47u
4	3	C3,C15,C16	100u
5	2	C14,C13	18p
6	1	C18	220u
7	1	C19	104
8	1	D1	3mm
9	1	D2	5.6V
10	1	D4	1N4148
11	1	JP1	HEADER 13
12	1	J1	Audio
13	1	J2	Video
14	6	L1,L2,L3,L4,L5,L6	FB
15	2	R2,R1	180
16	1	R3	75
17	1	R4	150K
18	1	R5	2K
19	1	S1	Right
20	1	S2	Left
21	1	S3	Up
22	1	S4	Down
23	1	S5	Mode Set
24	1	S6	Reset
25	1	U2	UR133-3.3V-A
26	1	U3	W55V94H
27	1	Y1	27MHz



8. DOCUMENT REVISION HISTORY

DATE	REVISION	EDITOR	REMARKS
02/22/2005	Ver. A0.9	Cliff Huang	Original issue
03/35/2005	Ver. A1.2	Cliff Huang	Revise PAD name, and application circuit.
04/18/2005	Ver. A1.3	Cliff Huang	Add important notice.
04/26/2005	Ver. A1.4	Cliff Huang	Revise DC characteristics.
05/05/2005	Ver. A1.5	INChu	Modify pin 13 name to become CLK.
08/06/2005	Ver. A1.6	INChu	Modify DC characteristics
05/02/2006	Ver. A1.7	INChu	Modify Application Circuit.



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