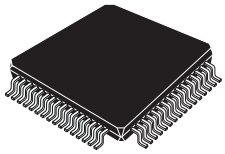
TDA7529

RF front-end for AM/FM DSP car-radio with IF sampling

Features

- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- I/Q mixer for FM IF 10.7MHz with image rejection and integrated LNA
- I/Q mixer for AM IF 10.7MHz up conversion with high dynamic range
- Integrated balun, Which allows saving of external mixer tank
- RF AGC, IF AGC, DAGC
- Low noise IF amplifier with switched wide dynamic AGC range
- IF switch for FM / AM / IBOC
- Electronic alignment for the preselection stages
- I^2C/SPI controlled
- single 5v SUPPLY
- Alternative frequency control signals to DSP



LQFP64

Description

The front-end is a high performance tuner circuit for AM/FM - DSP car-radios with 10.7MHz IF sampling. It contains mixer and IF amplifiers for AM and FM, fully integrated VCO and PLL synthesizer on a single chip. Use of BiCMOS technology allows the implementation of several tuning functions and a minimum of external components.

Table 1. Device summary

Part number	Package	Packing
TDA7529	LQFP64 exposed pad (10x10x1.4)	Tray
TDA7529TR	LQFP64 exposed pad (10x10x1.4)	Tape and reel

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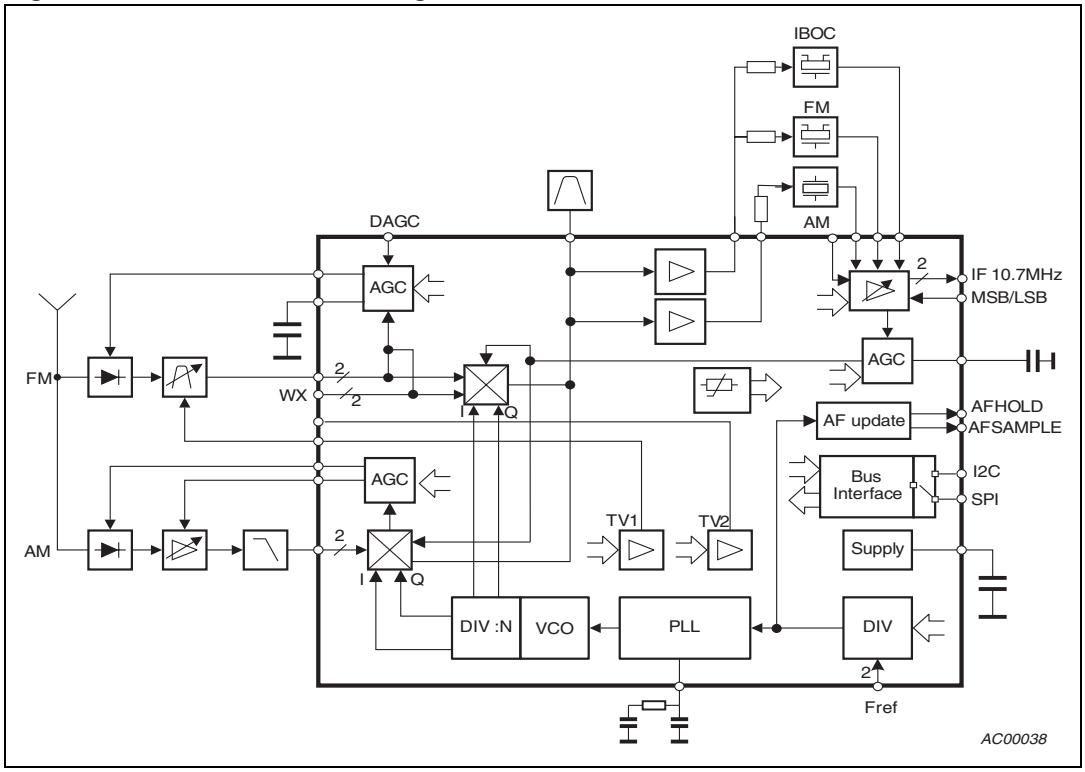
Figure 1. Functional block diagram



2 Pins description

Figure 2. Pin connection

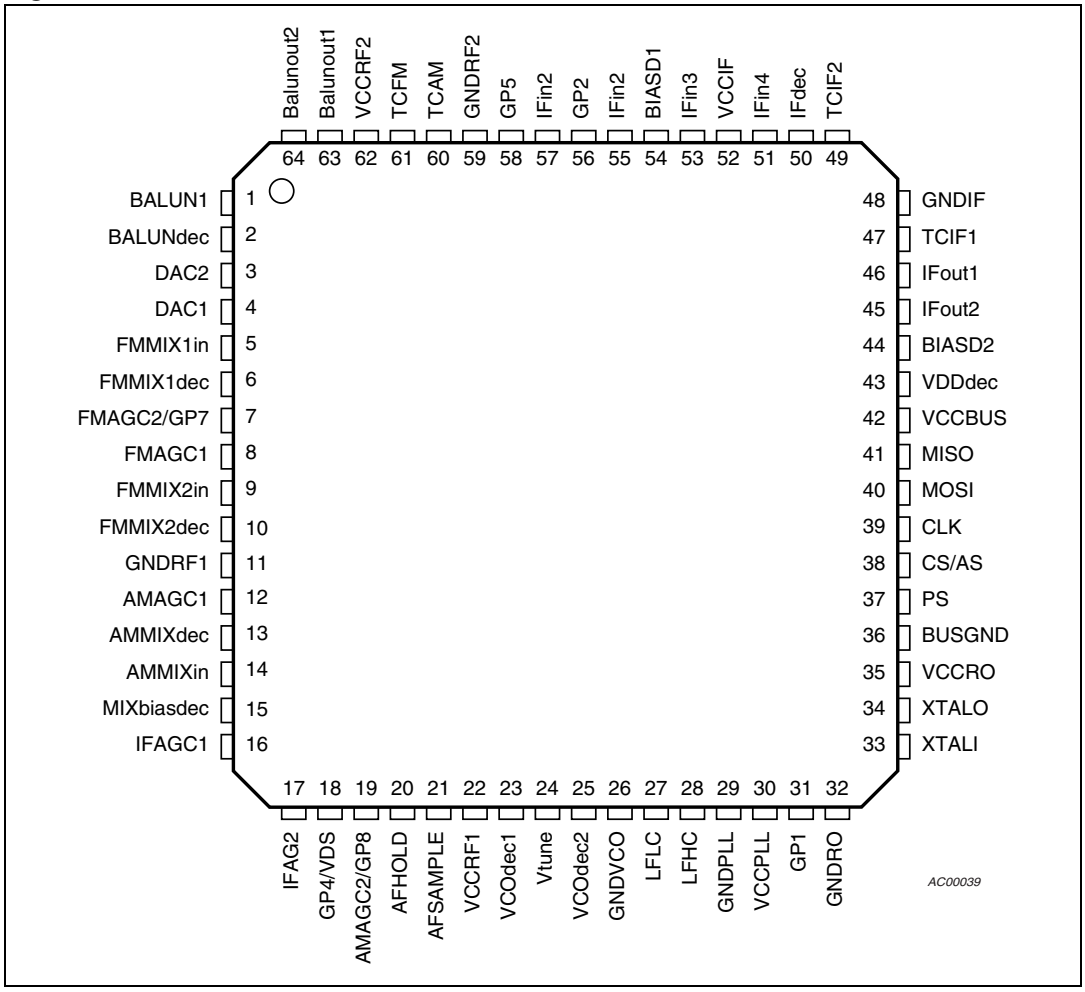


Table 2. Pin assignment

Pin #	Pin Name	Description
1	BALUN1	active balun input 1
2	BALUNdec	active balun input 2 (de coupling)
3	DAC2	Tuning DAC 2 output
4	DAC1	Tuning DAC 1 output
5	FMMIX1in	FM mixer input – high gain stage = mode 1
6	FMMIX1dec	FM mixer de couple
7	FMAGC2/GP7	FM AGC voltage output / alternative GP7 output
8	FMAGC1	FM PIN diode driver output
9	FMMIX2in	FM Mixer input – low gain stage = mode2

Table 2. Pin assignment (continued)

Pin #	Pin Name	Description
10	FMMIX2dec	FM Mixer de couple
11	GNDRF1	GND RF1 section
12	AMAGC1	AMAGC PIN diode driver output
13	AMMIXdec	AM mixer de couple
14	AMMIXin	AM mixer input
15	MIXbiasdec	Mixer bias de coupling
16	IFAGC1	IFAMP gain control via IFAGC - LSB
17	IFAGC2	IFAMP gain control via IFAGC - MSB
18	GP4/VDS	GPIO 4 / VDS input
19	AMAGC2 / GP8	AMAGC voltage output / alternative GP8 output
20	AFHOLD	AF state machine hold output
21	AFSAMPLE	AF state machine sample output
22	VCCRF1	Supply RF1 section
23	VCOdec1	BIAS de couple for VCO
24	Vtune	VCO tuning voltage
25	VCOdec2	BIAS de couple for VCO
26	GNDVCO	VCO Ground
27	LFLC	Loop filter low current output
28	LFHC	Loop filter high current output
29	GNDPLL	PLL Ground
30	VCCPLL	Supply PLL
31	GP1	GPIO 1
32	GNDRO	Ground PLL digital part
33	XTALI	Reference oscillator input
34	XTALO	Reference oscillator output
35	VCCRO	Supply PLL digital part
36	BUSGND	BUSinterface Ground
37	PS	Protocol Select
38	CS/AS	Chip select / Address select
39	CLK	SPI / I2C clodk
40	MOSI	SPIdata input / I2C Data
41	MISO	SPI Data Output
42	VCCBUS	Supply of BUSinterface
43	VDDdec	De couple of internal 3.3V (=3,3V + Vbe)

Table 2. Pin assignment (continued)

Pin #	Pin Name	Description
44	BIASD2	De coupling for Biasing
45	IFout2	Differential IF output 2
46	IFout1	Differential IF output 1
47	TCIF1	time constant IF AGC for AM
48	GNDIF	ground IF section
49	TCIF2	time constant IF AGC for FM
50	IFdec	De couple of IF amplifier
51	IFin4	IF input 4
52	VCCIF	Supply IF section
53	IFin3	IF input 3
54	BIASD1	De coupling for Biasing
55	IFin2	IF input 2
56	GP2	GPIO 2
57	IFin1	IF input 1
58	GP5	GPIO 5
59	GNDRF2	GND RF2 section = active balun GND
60	TCAM	AM AGC time constant
61	TCFM	FM AGC time constant
62	VCCRF2	Supply voltage RF2 section
63	Balunout1	Active balun output 2 = FM output
64	Balunout2	Active balun output 1 = AM output

3 Function description

3.1 IMR Mixer and active balun output

The IMR mixer has two FM inputs (referred as mode 1 / mode 2) and one AM input selectable by software. The FM inputs differ by their gains, noise figures, IIP3 and maximum signal handling capability. The mode 1 FM input (with the higher gain, lower IIP3 and lower noise figure) is normally coupled with passive antenna input stages; the mode 2 FM input is normally used for input stages featuring an external preamplifier.

There are two single ended outputs of the IMR mixer: Balunout1 has a 4 dB higher gain than Balunout2. It is not recommended to use both outputs in parallel.

The Balun1 pin is the current mixer output over an internal resistor. The LC filter at Balun1 can be realized with a low cost SMD-coil (Q ~ 4).

3.2 FM RF-AGC

The FM AGC system is controlled by a peak detector, whose gain can be varied by the keyed AGC. The latter function is meant to be controlled by a D/A converter in the back-end part of the system.

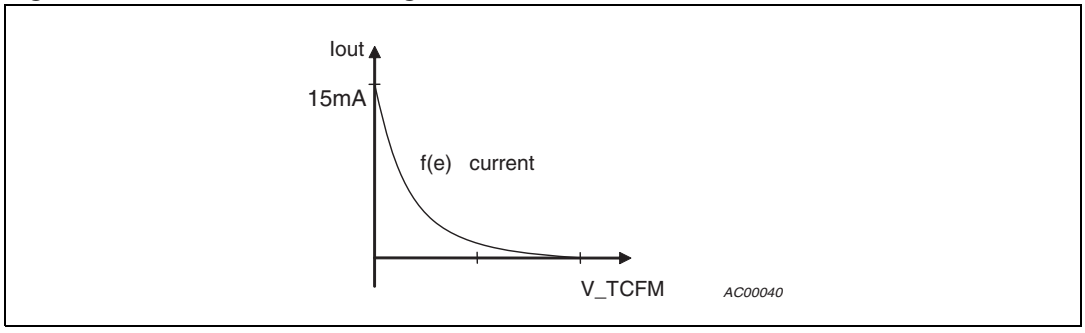
The time constant of the FM RF-AGC is defined by an external capacitor connected to TCFM and programmable internal currents. The currents can be selected independently for AGC attack and decay. By this the ratio between the attack and the decay time can be programmed between 0.4 and 250.

The FM RF-AGC has two output pins to drive one PIN diode attenuator and the external preamplifier gain control.

The AGC outputs can be programmed to the following modes:

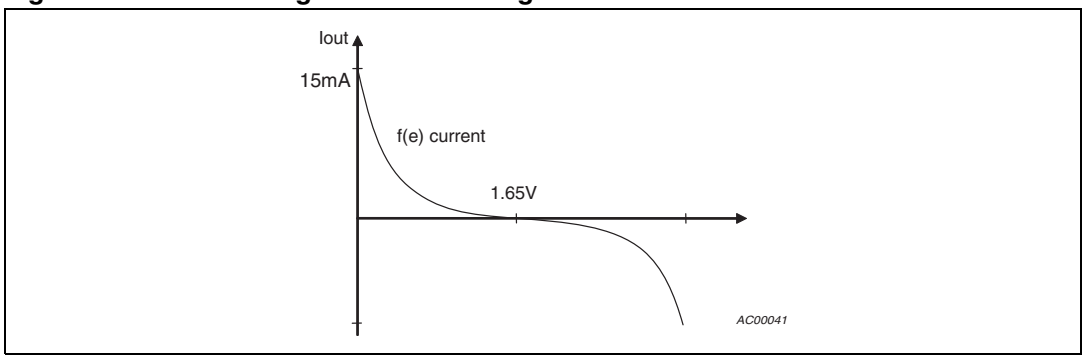
1. Positive current I=f(e): after reaching the AGC threshold voltage, the current output delivers a current I=f(e) up to 15mA in a voltage range from 0.1V (@10µA sink current) up to V_{CC}-1.2V with a quasi-exponential characteristic referred to the voltage at TCFM.

Figure 3. Positive current diagram



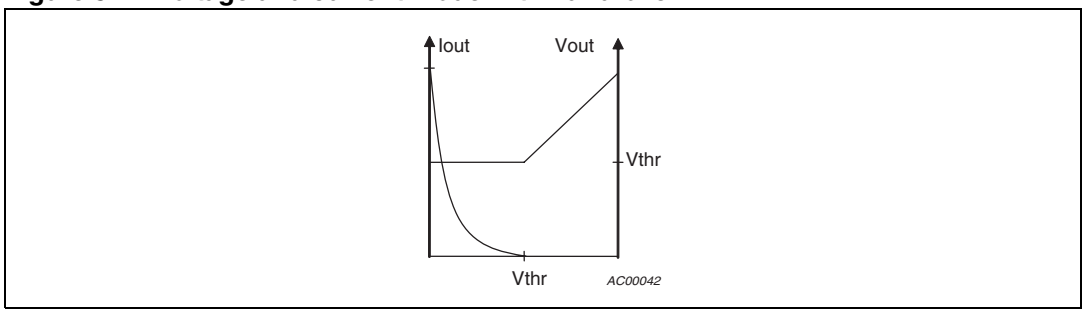
2. Pos/neg current I = f(e): below the AGC threshold voltage the AGC output sinks a constant current of -5 mA. When the RF input level crosses the AGC threshold voltage, the current is reduced down to 0 mA with a quasi-logarithmic behavior. At half control voltage the current becomes positive and reaches up to 15mA following an exponential function.

Figure 4. Positive/negative current diagram



3. Constant current mode: the output current can be set to 2 mA source current. The AGC detector is in power -down mode and only the PIN diode driver is active.
4. Voltage and current mode with hand-over: the Vthr level is programmable with 6 bit in the range of 0.2V to 2.56V. The voltage Vthr is the internal reference voltage of an external cascode transistor emitter feedback loop.

Figure 5. Voltage and current mode with hand-over



The voltage output swing is comprised between 0V and 3.3V (VDD).

The microcontroller can read the voltage at the AGC capacitor via the serial control interface.

3.3 AM RF-AGC

The AM AGC system is controlled by an average detector. The time constant of the AM RF-AGC is defined by an external capacitor connected to TCAM and programmable internal currents with symmetrical attack/decay behavior.

The AM RF-AGC has two output pins to drive one PIN diode attenuator and the external preamplifier gain control.

The AGC outputs can be programmed to the same modes as the FM RF-AGC with the exception of pos/neg current.

The microcontroller can read the voltage at the AGC capacitor via the serial control interface.

3.4 IF AGC and IF amplifier

The IF AGC system is controlled in AM with an average detector and in FM with a peak detector, and reduces the mixer gain. The time constant is defined by two external capacitors connected to TCIF1 and TCIF2 respectively, and programmable internal currents.

The microcontroller can read the voltage at the AGC capacitors via the serial control interface.

The IF amplifier gain is not affected by the on-chip IF-AGC but is meant to be controlled by the back-end part of the system through pins IFAGC1 and IFAGC2. The gain is reduced in 6 dB steps starting from the programmed value "G" according to the following table:

Table 3. IF AGC and IF amplifier

IFAGC2	IFAGC1	Gain
0	0	G
0	1	G - 6dB
1	1	G - 12dB
1	0	G - 18dB

3.5 Dividers

The mixer divider V is followed by a divide-by-4-stage that generates 0°/90°/-90° LO signals for the IMR mixer (90°/-90° mode to switch between upper or lower side-band suppression in the IMR mixer).
The main divider N can be operated in integer mode.

3.6 D/A Converters

The front-end contains two D/A-converters for tuning the filters of the FM pre-stage. The converters have a resolution of 9 bit.

3.7 VCO

The 3.7 GHz VCO has an internal switch that allows extending the oscillation frequency range. This is required by the fact that each of the two resulting VCO sub-bands (upper/lower) cannot individually cover the complete required frequency range versus temperature and process; for this reason a calibration procedure is needed to determine the process type (typical, slow, fast) and select the transition frequency between the two VCO sub-bands.

To run the procedure the VCO range 2 must be selected, the synthesized frequency needs to be set to 4GHz; then if Vtuning > 2.6V then the process is 'slow', if Vtuning < 1.7V then is 'fast' and otherwise is 'typical'. The switching frequency as a function of the process is reported in the following table:

Table 4. Switching frequency as a function of the process

SLOW	TYP	FAST
3.635GHz	3.72GHz	3.794GHz

3.8 FREF

The reference frequency for the PLL can be derived by a XTAL directly connected to the device or by means of an LVDS signal. In the latter case an external matching resistor must be used to obtain the desired input signal level.

3.9 A/D converter

The front-end contains a 6 bit SAR A/D-converter for sensing several analog values of the tuner. The following analog sources can be switched to the ADC input by software command:

- FM RF AGC capacitor voltage
- AM RF AGC capacitor voltage
- IF AGC capacitor voltage (automatically connected to the FM or AM IF AGC filtering capacitor)
- PLL tuning voltage
- Temperature sensor
- GPIO 1 voltage
- GPIO 2 voltage
- ADC reference generated from VCC.

The ADC can be clocked by an integrated RC-oscillator, in which case the oscillation frequency is programmable, or by the PLL reference frequency.

3.10 GPIO - general purpose IO interface pins

The front-end has seven GPIO - general purpose control pins to switch external stages (output), e.g amplifiers, or to read the status of external stages (input), e.g. control voltages. Some control pins are multiplexed with other functions that are not necessary in every tuner design (FM AGC keying, AM cascode control). All the GPIOs may put in tristate or in enable mode. When in enable the GPIOs can be configured as shown in the following table.

All GPIOs are short-circuit protected by current limiter and voltage-tolerant up to 3.5V.

Table 5. GPIO - general purpose IO interface pins

GPIO ports	FUNCTION	
GPIO1	selects function of GPIO1: if input, connects GPIO1 to ADC (ADC must then be configured to use GPIO1 as input); if output, level depends on GPIO Out Lev Ctrl → GPIO1	- AnlgIn to AD - DigOut
GPIO2	selects function of GPIO2: if input, connects GPIO2 to ADC (ADC must then be configured to use GPIO2 as input) and to KAGC (FM KAGC must then be enabled); if output, level depends on GPIO Out Lev Ctr → GPIO2	- AnlgIn to AD – Kagc In - DigOut
GPIO4	selects function of GPIO4: if input, configures GPIO4 as AM Cascode V_{DS} input; if output, level depends on GPIO Out Lev Ctrl → GPIO4	- AnlgIn - DigOut
GPIO5	selects function of GPIO5: if input, it is directly connected to read-only register byte 48 bit 4; if output, level depends on GPIO Out Lev Ctrl → GPIO5. When set to input, it is necessary to set IF AMP → GPIO5 out mode to “ON GPIO5 out En” (labels are wrong). Also used for production testing as analog output (not relevant for application).	- DigIn - Out (Dig or Anlg)
GPIO6	selects function of GPIO6 if device is configured in I^2C mode: if input, it is directly connected to read-only register byte 48 bit 5; if output, level depends on GPIO Out Lev Ctrl → GPIO5. When the device is configured in SPI mode, program GPIO Out Lev Ctr → GPIO5 to “Low”. The value of GPIO mode → GPIO5 does not matter	- Din (spi MISO out) - Dout (spi MISO out)
GPIO7	selects function of GPIO7: if digital output is selected, level depends on GPIO Out Lev Ctrl → GPIO7; otherwise, configures GPIO7 as FM AGC Vout	- Digital Out - FM agc Vout
GPIO8	selects function of GPIO8: if output, level depends on GPIO Out Lev Ctrl → GPIO8; otherwise, configures GPIO8 as AM AGC Vout	- Digital Out - AM agc Vout

3.11 AFSAMPLE/AFHOLD

On the TDA7529 there are two dedicated open drain pins (AFSAMPLE and AFHOLD), that allow the control of the DSP (mute and quality controls) during AF update.

Details are given in *Chapter 5*.

3.12 Serial BUS interface

The TDA7529 has a serial data port for communication with the microcontroller. It is used for programming the device and for reading out its detectors. This port supports data communication using the SPI and the I^2C protocol. The data transfer of several consecutive bytes is supported by the auto increment feature.

Table 6. Supports data communication using the SPI and the I^2C protocol

	Pin	SPI signal	Pin	I^2C signal
Signal 1	PS	Protocol Select SPI/I^2C	PS	Protocol Select SPI/I^2C
Signal 2	CS	Chip Select	AS	Address Select
Signal 3	CLK	Clock	CLK	Clock
Signal 4	MOSI	Master Out – Slave In	DATA	bidirectional Data
Signal 5	MISO	Master In – Slave Out	GP6	General Purpose Out

The "PS"- pin (Protocol Select) determines which communication protocol is used. The information is not latched, so any level change at this pin immediately affects the protocol used by the TDA7529.

The SPI protocol is selected by setting PS = 0 while, during the I^2C operation, PS needs to be open (internally set to 1).

SPI-Protocol: CPOL=1, CPHA=1.

The CS pin performs the Chip Select function during the SPI operation; it has to be reset to 0 during transmission or reception, otherwise set to 1 (the CS pin is set to 1 by leaving it open).

Both the CS and the AS functions are performed by the CS pin.

When the I^2C mode is used, the "AS" pin determines which I^2C address or group of addresses (see below) is used. Three different external connections are defined to represent three groups of addresses (refer to the following table for details). The information is not latched, so any level change at this pin immediately affects the address used by the TDA7529.

First the IC address is transmitted including the R/W bit for setting the direction of the following data transfer

Table 7. I^2C addresses

Tuner:	Tuner 3	Tuner 2	Tuner 1
level at pin AS	2.2V – 3.5V	1.1V – 1.7V	0.0V – 0.6V
address:	1100 1xxd	1100 x1xd	1100 xx1d
MSB ... LSB			
1100 000d			
1100 001d			R / W
1100 010d		R / W	
1100 011d		W	W
1100 100d	R / W		
1100 101d	W		W
1100 110d	W	W	
1100 111d	W	W	W

x = must be "0" for reading, can be "1" or "0" for writing to the TDA7529

d = determinates the direction of data transfer, reading or writing

R / W = indicates the address to read to and/or to write from a single TDA7529

W = indicates those addresses that can be used to transmit equal data to several TDA7529 frontends. A read out has no purpose for these addresses (data collision), but must be possible without damaging the tuner IC.

The two serial bus protocols, I^2C and SPI, are as follows:

Figure 6. I^2C (sub address mode)

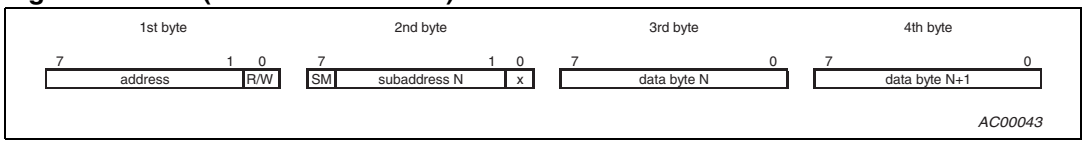
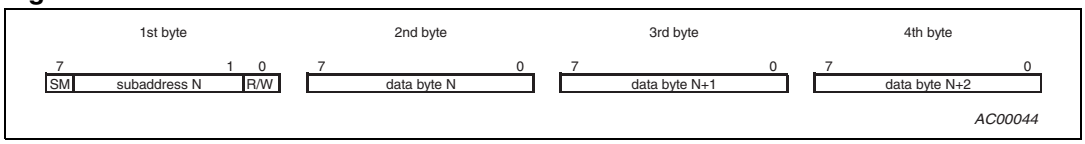


Figure 7. SPI



Data auto increment mode is always active regardless of the serial bus mode chosen.

4 Electrical specifications

Electrical parameters are guaranteed if F_{ref} = 100kHz, with frequency stability of +/- 20ppm max.

4.1 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Abs. supply voltage				5.5	V
T_{amb}	Ambient temperature range		-40		105	°C
T_{stg}	Storage temperature		-55		150	°C
T_j	Junction temperature				150	°C

4.2 Thermal data

Table 9. Thermal data

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient	2s2p std Jedec board with thermal via underneath the component (36 board via: diameter = 0.5mm / pitch = 1.5mm), max 30% missing soldering			33	°C/W

4.3 General key parameters

Table 10. General key parameters

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
V_{CC}	5V supply voltage		4.7	5	5.35	V
I_{CC}	Supply current @ 5V			145	175	mA
I_{CC_pwd}	Supply current @ 5V in power down mode			9	14	mA
T_{amb}	Ambient temperature range		-40		105	°C

4.4 FM - section

Refer to application circuit in figure 3. V_{CC} = 4.7V to 5.35V; T_{amb} = -40 to +105°C; f_c = 76 to 108 MHz; 60dBµV antenna level; mono signal, unless otherwise specified. Antenna level equivalence: 0dBµV = 1µV_{rms}, all RF levels are intended as PD.

Table 11. FM - section

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
FM IMR Mixer and active balun						
G_{mix1}	Mixer conversion gain	mode 1 (unloaded)	20	22	24	dB
		mode 2 (unloaded)	14	16	18	
	Gain attenuation range	controlled by IF-AGC	18	20		dB
R_{in}	Input impedance	mode 1	30	50		kΩ
		mode 2	5	6.5	9.5	
R_{out}	Output impedance	active balun	15	20	30	Ω
V_{out_max}	Max. output voltage	without clipping (unloaded)	122			dBµV
v_{noise}	Input noise voltage	Mode1, Rsource=1.5kΩ, noiseless		3	3.7	nV/√Hz
		Mode 2, Rsource=800, noiseless		5	6	
IIP3	3rd order intercept point(1)	mode 1 up to Vin/tone = 90 dBµV	123	125		dBµV
		mode 2 up to Vin/tone = 98 dBµV	132	134		
IIP2	2nd order intercept point	mode 1	144			dBµV
		mode 2	152			
IRR	Image rejection ratio	without gain/phase adjust	30			dB
		with gain/phase adjust	40	45		
FM RF AGC						
L_{thr}	Mixer input referred RF level threshold	mode 1, min. setting	82	85	88	dBµV
		mode 1, max setting	97	100	103	
		mode 2, min. setting	90	93	96	
		mode 2, max setting	105	108	111	
	Threshold steps	4 bit control	0.5	1	1.5	dB
	Pin diode source current	AGC control pin 1 Logarithmic current	10			mA
	Pin diode sink current	AGC control pin 1 Logarithmic current			-3	mA
	Pin diode source current in constant current mode		1	2		mA
	Threshold shift keyed AGC	Control input = 1V	10.5	12.5	13.5	dB/V

1. parameter guaranteed by correlation.

4.5 AM - section

Refer to application circuit in figure 3. V_{CC} = 4.7V to 5.35V; T_{amb} = -40 to +105°C; LW, MW and SW bands; 74dBµV antenna level, unless otherwise specified. Antenna level equivalence: 0dBµV = 1µVrms, all RF levels are intended as EMF.

Table 12. AM - section

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
AM IMR Mixer and active balun						
Gmix1	Mixer conversion gain		7.2	9	10.5	dB
∆gmix1	Gain attenuation range	controlled by IF-AGC	18	20		dB
Rin	Input impedance		5	6.5	9.5	kΩ
Rout	Output impedance		15	20	30	W
	Min. external load		400			W
Vin_max	Max. output voltage	without clipping (unloaded)	122			dBµV
Vnoise	Input noise voltage			6	8.3	nV/√Hz
IIP3	3rd order intercept point		130	134		dBµV
IIP2	2nd order intercept point		159			dBµV
IRR	Image rejection ratio	without gain/phase adjust	30			dB
IRR	Image rejection ratio	with gain/phase adjust	40	45		dB
AM RF AGC External capacitance for time constant from 1nF to 4700nF – time constant values are directly proportional to the external capacitor value						
Lthr	Mixer input referred RF level threshold	min. setting	83	86	89	dBµV
		max setting	98	101	104	
	threshold steps	4 bit control	0.5	1	1.5	dB
	Pin diode source current	AGC control pin 1 Logarithmic current	10			mA
	Min. voltage	AGC control pin 1 with 5µA sink current			0.1	V
	Isink	5µA sink current	5	10		µA
	Pin diode source current in constant current mode		1			mA
	Max. voltage	AGC control pin 1	V_{CC}-1.4	V_{CC}-1.2		V
	Max. output voltage in GPO mode	AGC control pin 2	V_{DD}-0.3		V_{DD}	V
	Min. output voltage	AGC control pin 2			0.3	V

Table 12. AM - section (continued)

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	Fast attack time constant	active in case of overdrive (more than 7dB)	0.05	0.5	5	ms
	Time constant	Range, mode T1 Range, mode T2 Range, mode T3		0.5-50 2.5-250 12.5-1250		ms ms ms

4.6 IF - section

Table 13. IF - section

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
IF AMPLIFIER						
Grange	Gain range	Input 1-3 (FM,HD,AM), min.	23	25	27	dB
		Input 1-3 (FM,HD,AM), max	36	38	40	
		Input 4 (HD-Radio AM), min.	15	17	19	
		Input 4 (HD-Radio AM), max	29	31	33	
Gstep	Gain step	3 bit control	1.5	2	2.5	dB
ΔAGC	AGC range		16.5	18	19	dB
	AGC steps	2-bit control	5.2	6	6.6	
Rin_input1	Input impedance input 1	FM –input @ 10.7MHz	230	330	450	W
Rin_input2	Input impedance input 2	HD-Radio FM input @ 10.7MHz	2.2	2.9	3.6	kΩ
Rin_input3	Input impedance input 3	AM input @ 10.7MHz	7	8.2	10	kΩ
Rin_input4	Input impedance input 4	HD-Radio AM input @ 10.7MHz	7	8.7	11	kΩ
Rout	Differential output impedance			15		W
Vout_max	Max. output voltage		115		117	dBµV
Gain, load	Gain variation in loaded conditions	10pF between each IFAMP outputs and GND, 10kΩ differential load			0.5	dB
IIP3,load	IIP3 decrease in loaded conditions	10pF between each IFAMP outputs and GND, 10kΩ differential load			1	dB
IIP3	3rd order intercept point	input stage 1-3, @ 25dB gain	119	122		dBµV
		input stage 4, @ 17dB gain	130	133		
IIP2	2nd order intercept point	input stage 1-3	142			dBµV
		input stage 4	154			

Table 13. IF - section (continued)

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
Vnoise_input 1	IN1 input noise voltage	@ source impedance 330Ω · noiseless, @31dB gain		3.5	4.2	nV/√Hz
Vnoise_input 2	IN2 input noise voltage	@ source impedance 470Ω · noiseless, @ 31dB gain, with external 560Ω input termination resistor		3.8	4.6	nV/√Hz
Vnoise_input 3	IN3 input noise voltage	@ source impedance 2.2kΩ · noiseless, @ 29dB gain, with external 2.7kΩ input termination resistor		5	6.5	nV/√Hz
Vnoise_input 4	IN4 input noise voltage	@ source impedance 2.2kΩ · noiseless, @ 24dB gain, with external 2.7kΩ input termination resistor		7	8.5	nV/√Hz
IF AGC External capacitance for time constant from 10nF to 500nF in FM (asym. mode), from 100nF to 4700nF in AM (sym. mode) – time constant values are directly proportional to the external capacitor value						
Lthr	IFAmp input referred	FM, min. setting	88.5	91	93.5	dBµV
		FM, max setting	99.5	101	103.5	
		AM, min. setting	86.5	89	91.5	
		AM, max setting	96.5	99	101.5	
	Threshold steps		1	1.5	2	dB
	Fast attack mode in AM-mode, range	active in case of overdrive	0.05	0.5	5	ms
	Time constant attack, range	FM: asym. mode U1 FM: asym. mode U2 AM: sym. mode S1 AM: sym. mode S2		10-500 0.05-2.5 2.0-100 20-1000		µs ms ms ms
	Time constant decay, range	FM: asym. mode U1 / U2 AM: sym. mode S1 AM: sym. mode S2		2-100 2-100 20-1000		ms ms ms

4.7 VCO

Table 14. VCO

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	Frequency range VCO	±8% tuning range	3430		4010	MHz
	Phase Noise of LO	Free running VCO; values referred @ 100MHz @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz	 -46 -76 -103	 -40 -60 -86 -106		dBc/Hz
	Deviation error	FM reception, de-emphasis 50µs, fNF=20Hz...20kHz @ min. VCO frequency		8		Hz

4.8 Reference frequency input buffer

Table 15. Reference frequency input buffer

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
Reference frequency input buffer mode						
	Max input voltage high				1475	mV
	Min. input voltage low		925			mV
	Input differential voltage		200		400	mV
	Input impedance (xtal mode)		150			kΩ
	Input impedance (lvds mode)		10			kΩ
	Input voltage range	Single ended mode	200		1000	mV_{PP}

4.9 Dividers

Table 16. Dividers

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
Mixer divider V – integer values						
N_V	divider value divider_V	7 bit	5		131	
Divide by 4 – generation of 0°/90°/-90° LO signal for IMR						
	I/Q phase error of divider	phase calibration in IMR	-0.5		0.5	DEG
Main divider N – integer divider						
N_N	divider value divider_N	21bit (32/33 pre scaler)	992		2097151	
Reference divider R – integer values						
N_R	divider value divider_R	8 bit	1		255	

4.10 Phase locked loop

Table 17. Phase Locked Loop

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	Settling time AM/FM	$\Delta f < 0,01\%$ @ f_{PFD} = 100 kHz		800	1200	µs
	Spurious suppression	@ divided VCO signal	70			dB

4.11 Phase frequency detector and charge pump

Table 18. Phase frequency detector and charge pump

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
PFD						
f_{PFD}	PFD input frequency		2		3000	kHz
Charge pump						
	Sink current	high current mode bit1	-0.4	-0.65	-0.9	mA
		high current mode bit2	-0.8	-1.3	-1.7	mA
		high current mode bit3	-1.7	-2.4	-3.1	mA
		high current mode bit4	-3.1	-4.5	-5.8	mA
		low current mode bit5	-40	-60	-80	µA
		low current mode bit6	-80	-120	-160	µA
		low current mode bit7	-160	-240	-320	µA
		low current mode bit8	-320	-480	-640	µA
		low current mode bit9	-640	-960	-1280	µA
	Source current	high current mode bit1	0.4	0.65	0.9	mA
		high current mode bit2	0.8	1.3	1.7	mA
		high current mode bit3	1.7	2.4	3.1	mA
		high current mode bit4	3.1	4.5	5.8	mA
		low current mode bit5	40	60	80	µA
		low current mode bit6	80	120	160	µA
		low current mode bit7	160	240	320	µA
		low current mode bit8	320	480	640	µA
		low current mode bit9	640	960	1280	µA

4.12 Temperature sensor

Table 19. Temperature sensor

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	Temperature range		-40		150	°C
	Resolution	°C/LSB (no direct measurement possible)		5		°C
	Absolute error				15	°C
	Relative error			0.5		LSB

4.13 D/A-Converter

Table 20. D/A-Converter

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
V_{out}	Output voltage minimum value	Unloaded output	0.5	0.6	0.8	V
	Output voltage maximum value	Unloaded output	VCC – 0.2	VCC – 0.1		V
	Output impedance			2		kΩ
	Max. output current		500			µA
	Average Voltage step	resolution 9bit	8.5	9	9.5	mV
	INL		-2		2	LSB
	DNL		-0.5		0.5	LSB
	Conversion time	@ C_L=1nF		20	40	µs
VSRR	Supply voltage ripple rejection ratio		20			dB

4.14 A/D-Converter

Table 21. A/D-Converter

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	INL		-2		2	LSB
	DNL		-0.5		0.5	LSB
	Input voltage range		0		V_{DD}	V
t_{ADC}	Conversion time				7	µs

4.15 GPIO – general purpose IO interface pins

Table 22. GPIO - general purpose IO interface pins

Pin name	GPIO functionality						Multiplexed functionality details are given in the corresponding chapters
	GPIO-Output				GPIO-Input		
	High level		Low level		Functionality	voltage	
	voltage	Source current	voltage	Sink current			
GP1	3.3V	1 mA	0V	1 mA	Analog input ADC	0 ... 3.3V	
GP2	3.3V	1 mA	0V	1 mA	Analog input ADC	0 ... 3.3V	FM key AGC input
GP4	3.3V	0.1 mA	0V	10 mA	AM cascode V_{DS} input	0 ... 3.3V	
GP5	3.3V	1 mA	0V	1 mA	Digital Input	0 / 3.3V	
GP6	3.3V	1 mA	0V	1 mA	Digital Input	0 / 3.3V	SPI MISO output
GP7	3.3V	1 mA	0V	1 mA			FM-AGC voltage output
GP8	3.3V	1 mA	0V	1 mA			AM-AGC voltage output

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
	High level output voltage	@ 100kΩ load to GND	V_{DD}-0.3			V
	Low level output voltage	@ 100kΩ load to V_{DD}			0.3	V
	High level source current	GP1 / GP2 / GP5 / GP6: @ 1kΩ load to GND	0.5	1		mA
	High level source current	GP4 @ 1kΩ load to GND	0.08	0.1		mA
	low level sink current	GP1 / GP2 / GP5 / GP6: @ 1kΩ load to V_{DD}	0.8	1		mA
	low level sink current	GP4: @ 100Ω load to V_{DD}	8.0	10		mA
	Input impedance	digital input mode	100			kΩ
	Input voltage range	GP1 / GP2	0		3.5	V
	High level input voltage	GP5 / GP6 used as digital input	2.2		3.5	V
	Low level input voltage	GP5 / GP6 used as digital input	-0.05		1.0	V

4.16 AFSAMPLE / AFHOLD

Table 23. AFSAMPLE / AFHOLD

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
	Output voltage at AFSAMPLE/AFHOLD				3.6	V
	Maximum sink current	V_o = 0.4V	800			µA

4.17 Serial Data Interface

Table 24. Serial Data Interface

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
VDD	Supply voltage		2.7		3.5	V
f_{clk}	Clock frequency	Guaranteed range @ SPI Guaranteed range @ I^2C	4 1			MHz MHz
	Power On Delay time	Ready for communication after Power-On-Reset			10	ms
	High level output voltage	Output signals	V_{DD}-0.3		V_{DD}	V
	Low level output voltage	Output signals	-0.05		0.3	V
	High level source current	Output signals	0.08	0.1		mA
	low level sink current	Output signals	0.8	1		mA
	Rise / fall time	Output signals, 90%	15	25	40	ns
	High level input voltage	Input signals, except AS	2.0		3.5	V
	Low level input voltage	Input signals, except AS	-0.05		1.0	V
	High level input voltage	AS input signal	2.2		3.5	V
	Medium level input voltage	AS input signal	1.1		1.7	V
	Low level input voltage	AS input signal	-0.05		0.6	V
	Input impedance	Input signals	100			kΩ
	Power-On impedance	All signals	100			kΩ
	Rise / fall time	Input signals except CLK, min. acceptable duration range, 90%	0.01		1000	µs
		Input signal CLK, min. acceptable duration range, 90%	0.01		10	µs

5 Tuning state machine

Frequency changes in a system employing the TDA7529 can be efficiently performed using a built-in state machine which simplifies the microprocessor supervisory functions. The state machine, which can work in 8 different modes, can be invoked by a simple WRITE operation into the tuner registers and, provided that the frequency to be jumped to has been pre-loaded into the front-end registers through a previous separate or is loaded through a concurrent WRITE operation, the FE jump sequence is automatically managed and flags are provided to the back-end to indicate the current condition.

5.1 Tuning state machine modes

Hereafter the description of the 8 modes can be found. They are chosen by Byte 12 bits<6:4>.

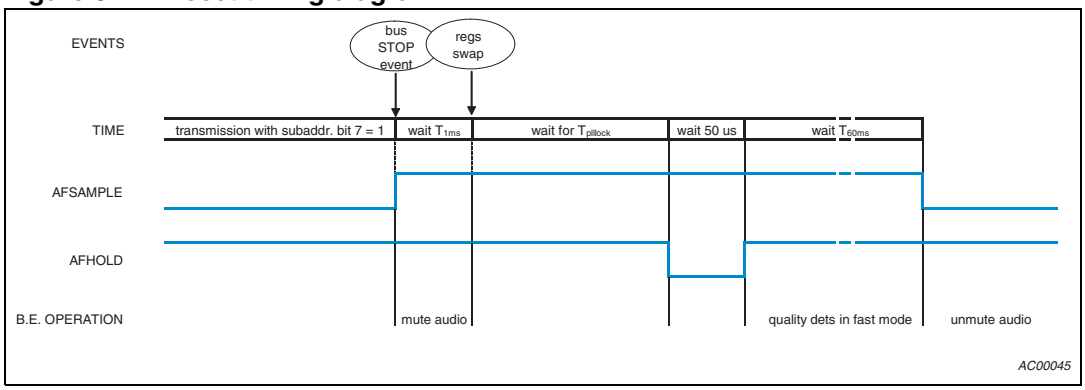
The diagrams depicting the FE and flag conditions for each of the 8 modes are as follows:

5.1.1 Mode 000: buffer (nil)

When this mode is selected, no action is undertaken by the state machine.

5.1.2 Mode 001: preset

Figure 8. Preset timing diagram



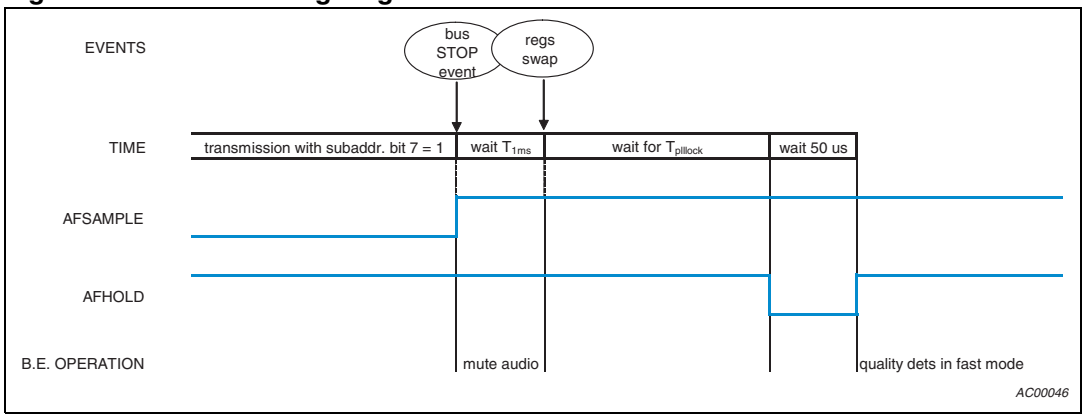
This mode is used to jump to a different frequency and stay there, with reception at the end of the sequence.

AFSAMPLE can be used to tell the back-end when to mute and to unmute the audio output. The 60 ms mute time (programmable) after the PLL has reached the locked condition can be used to check the RDS signal presence and content in addition to the analog quality information.

AFHOLD can be used to tell the back-end to switch to faster time constants for quick quality acquisition.

5.1.3 Mode 010: search

Figure 9. Search timing diagram



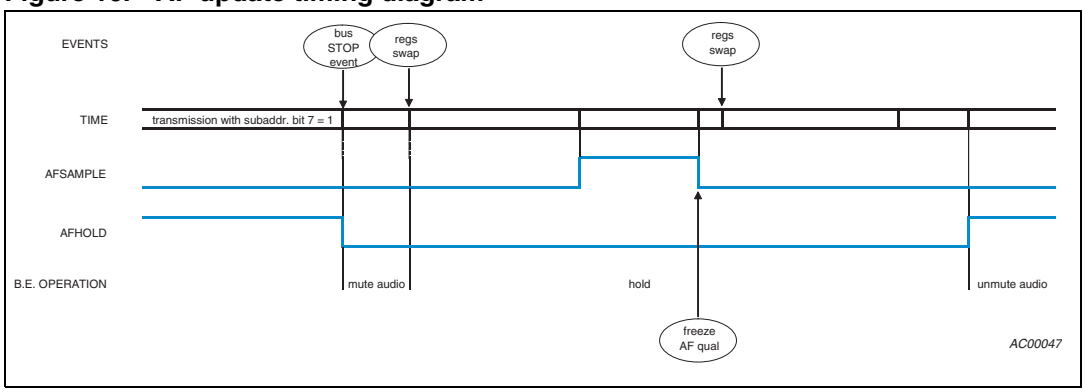
This mode is used to jump to a different frequency and stay there, with audio muted.

AFSAMPLE can be used to tell the back-end when to mute the audio output.

AFHOLD can be used to tell the back-end to switch to faster time constants for quick quality acquisition.

5.1.4 Mode 011: AF update

Figure 10. AF update timing diagram



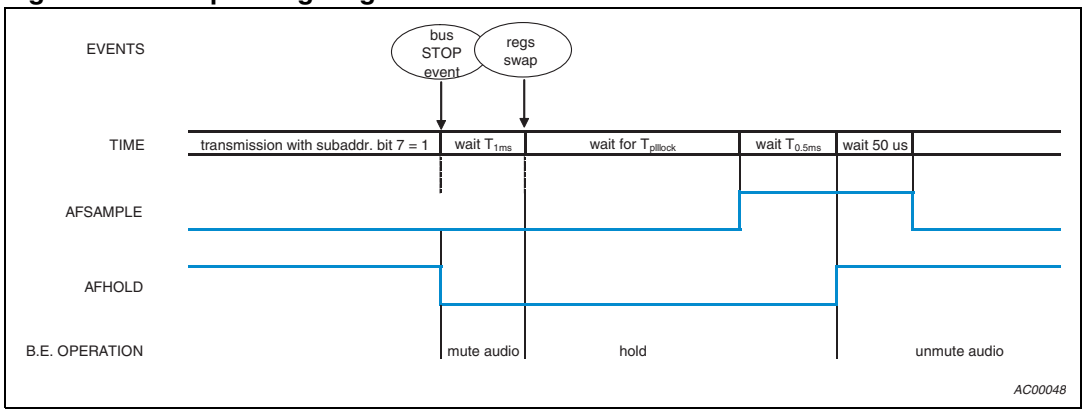
This mode is used to jump to an AF frequency, check its quality, jump back to the starting frequency and continue reception.

AFSAMPLE can be used to tell the back-end when to acquire the AF frequency quality.

AFHOLD can be used to tell the back-end to mute/unmute the audio and keep normal processing on hold.

5.1.5 Mode 100: jump

Figure 11. Jump timing diagram



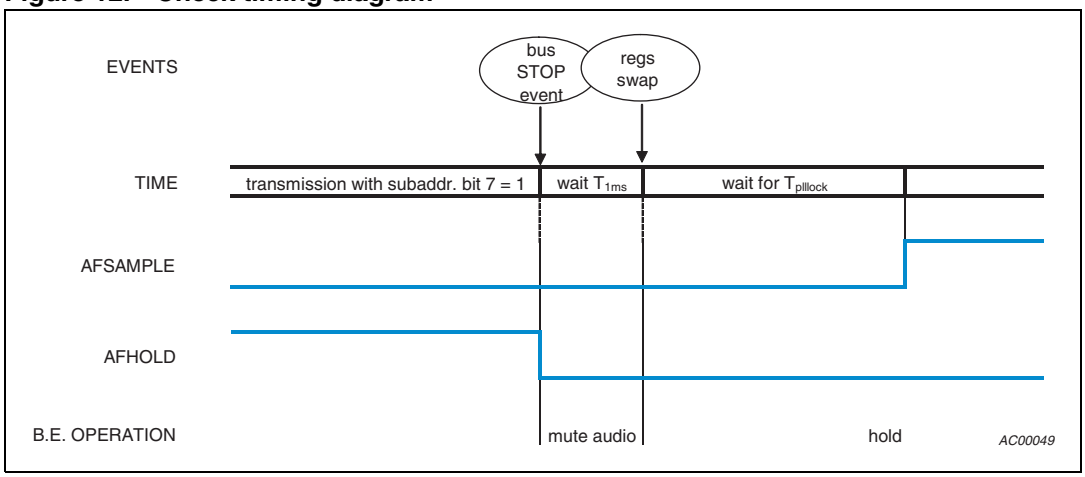
This mode is used to jump to a different frequency and stay there, with reception at the end of the sequence.

AFHOLD can be used to tell the back-end to mute/unmute the audio and keep normal processing on hold.

AFSAMPLE can be used to tell the back-end when the quality signal processing can be restarted, with a stable situation to start from.

5.2 Mode 100: check

Figure 12. Check timing diagram



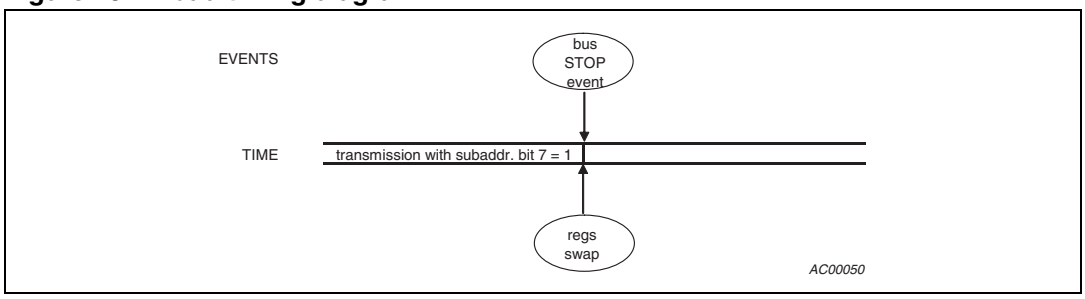
This mode is used to jump to a different frequency and stay there, with audio muted.

AFHOLD can be used to tell the back-end to mute/unmute the audio and keep normal processing on hold.

AFSAMPLE can be used to tell the back-end when to freeze the quality signal processing.

5.3 Mode 110: load

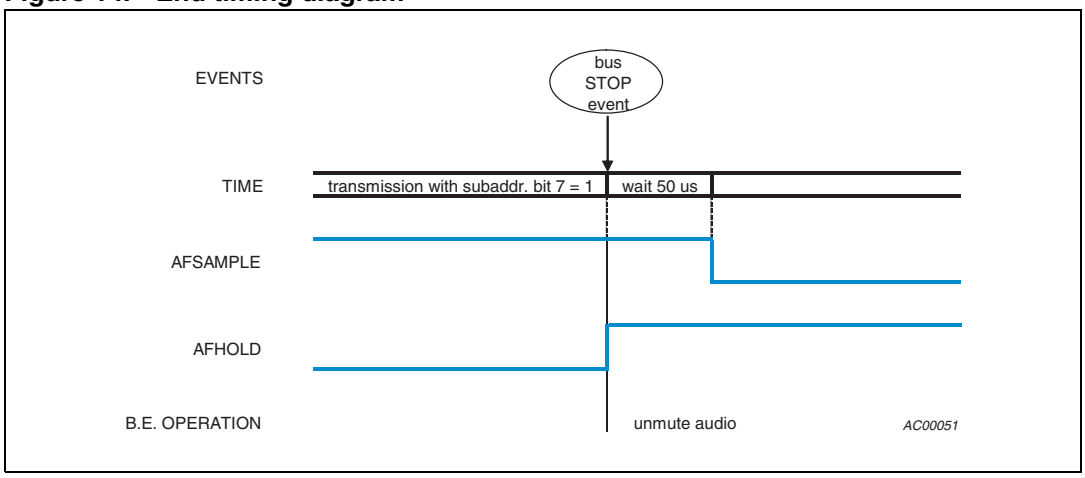
Figure 13. Load timing diagram



The content of the buffer and control registers is swapped. No transition occurs on the AFHOLD and AFSAMPLE lines.

5.4 Mode 111: end

Figure 14. End timing diagram



This mode is used to end sequences that terminate with muted audio, after the decision on whether to stay to that frequency or jump to a different one has been taken.

AFHOLD can be used to tell the back-end to unmute the audio.

AFSAMPLE can be used to tell the back-end to restore normal quality signal processing.

Most of the wait times of the algorithm can actually be programmed.

The following table summarizes the minimum, maximum and default values of the programmable wait times. The indicated values are valid only for the advised configuration where the phase detector reference frequency is 100 kHz.

Table 25. Values of the programmable wait times

PARAMETER NAME	REGISTER		VALUE	TIME
T_{pllock}	Byte 15 bits<7:3>	min.	00000	20 us
		default	00110	1 ms
		maximum	11111	5 ms
$T_{0.5ms}$	Byte 30 bits<7:2>	min.	000000	70 us
		default	000101	0.5 ms
		maximum	111111	5 ms
T_{1ms}	Byte 20 bits<7:2>	min.	000000	10 us
		default	001100	1 ms
		maximum	111111	5 ms
T_{2ms}	Byte 29 bits<7:2>	min.	000000	50 us
		default	011000	2 ms
		maximum	111111	5 ms
T_{60ms}	Byte 04 bits<7:3>	min.	00000	1 ms
		default	10111	60 ms
		maximum	11111	80 ms

5.5 Register SWAP

Some of these modes contain one or two register "swap" operation(s). The changes within the register structure during a swap operation depend on the operating mode of the chip.

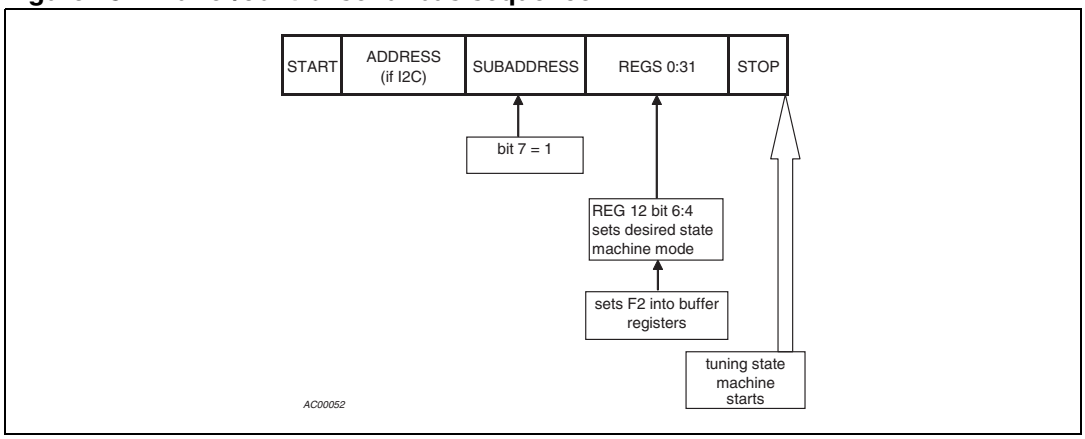
If the chip is programmed in the "buffer/control" mode (chosen by setting byte 12 bit 7 = 1), which is necessary to take advantage of the tuning state machine, it is suggested that the microprocessor write data only in the normal register bank (bytes from 16 to 31), because the state machine itself takes care of exchanging the content of the normal register bank with that of the shadow bank (bytes from 32 to 47) during a swap. The normal registers are intended to be written to by the radio microprocessor, whereas the registers that actually control the device circuits are the shadow ones.

In any case it is suggested that the bits 5 and 4 of byte 0, that define which control bank is actually used to drive the device circuits, should not be touched after setting them to 0 after reset because they are automatically updated by the tuning state machine.

5.6 State machine start

The tuning state machine is activated only at the end of the transmission if bit 7 of the subaddress is 1. The activation sequence, therefore, is to be done in the following way.

Figure 15. Buffer/control serial bus sequence



6 Registers description

Figure 16. Registers description

No	name	r/w	MSB (7)	6	5	4	3	2	1	LSB (0)	Power on default
0	**Short reg**	r/w	x	x	ShAGC	ShPLL	ADCstart	ADCen	GPIOen	PWR	00h
1	ADCctrl	r/w	ADCclk	ADCs2	ADCs1	ADCs0		RCenable	ADCautomode	Temp_pwr	00h
2	GPIOval	r/w	GPO8_AMAGCv	GPO7_FMAGCv	GPIO6_MISO	GPIO5_Aout	GPO4_AMcas	CP_curr_switch	GPIO2io	GPIO1io	00h
3	AGCmixCtrl	r/w	IFin1_AM_FM	KeyAGCen	FMAGCpwr	AMAGCpwr	MixinFMAM	BalunoutIMP	Mixout1	Mixout2	00h
4	Misc1	r/w	WAIT60ms(4)	WAIT60ms(3)	WAIT60ms(2)	WAIT60ms(1)	WAIT60ms(0)	disvcc	PLLtest	AMAGC_Isink	00h
5	DivR	r/w	divr7	divr6	divr5	divr4	divr3	divr2	divr1	divr0	00h
6	IFAGC_SH	r/w	IFAGC_FM_AM	IFAGCthr2	IFAGCthr1	IFAGCthr0			GPIO5 output	IFsection_pwr	00h
7	FMAGC	r/w	FMthr3	FMthr2	FMthr1	FMthr0	FMAGCmodeC1	FMAGCmodeC0	FMAGCmodeV1	FMAGCmodeV0	00h
8	FM_AM_Vthr	r/w	AMAGCfat	AFH_MUX	Vthr5	Vthr4	Vthr3	Vthr2	Vthr1	Vthr0	00h
9	MIXalign1	r/w	IFAMP_Ictrl2	IFAMP_Ictrl1	IredH	IredL	Casc_ctrl	IMRF2	IMRF1	IMRF0	00h
10	MIXalign2	r/w	IMRph3	IMRph2	IMRph1	IMRph0	IMRG3	IMRG2	IMRG1	IMRG0	00h
11	PLLctrl	r/w	DZ4	DZ3	DZ2	DZ1	CPcur_800u	SWfref	divRen	PLLpwr	00h
12	PLLctrl2	r/w	FUNC	MODE2	MODE1	MODE0	DS4	DS3	DS2	DS1	00h
13	PLLtest	r/w	POL	PFD_D1	PFD_D0	PLLT4	PLLT3	PLLT2	PLLT1	PLLT0	00h
14	Misc2	r/w	IFAGCin4ctrl	EnSMOOTH	reg48sel	IFAMP_Ictrl0	RCfreq_1	RCfreq_0	VCOMag1	VCOMag0	00h
15	WAIT_LOCK	r/w	WAIT LOCK(4)	WAIT LOCK(3)	WAIT LOCK(2)	WAIT LOCK(1)	WAIT LOCK(0)	DIVVtest	VCOext	LOCK_bit	00h
16	AGCtc_A	r/w	IFAGCtcAM	IFAGCtcFM	AMtc1	AMtc0	FMtc3	FMtc2	FMtc1	FMtc0	00h
17	AMAGC_A	r/w	AMthr3	AMthr2	AMthr1	AMthr0	AMAGCmodeC1	AMAGCmodeC0	AMAGCmodeV1	AMAGCmodeV0	00h
18	GPIOm_A	r/w	GPO8hl	GPO7hl	GPIO6hl	GPIO5hl	GPO4hl		GPIO2hl	GPIO1hl	00h
19	IFCTRL_A	r/w	IFin0_Std_IBOC	IFAmpgainA2	IFAmpgainA1	IFAmpgainA0	MixinFM	AMAGCinbuffer	RCtest		00h
20		r/w	WAIT1ms(5)	WAIT1ms(4)	WAIT1ms(3)	WAIT1ms(2)	WAIT1ms(1)	WAIT1ms(0)			00h
21	DivN_A1	r/w	divnA20	divnA19	divnA18	divnA17	divnA16	divnA15	divnA14	divnA13	00h
22	DivN_A2	r/w	divnA12	divnA11	divnA10	divnA9	divnA8	divnA7	divnA6	divnA5	00h
23	DivN_A3	r/w	divnA4	divnA3	divnA2	divnA1	divnA0				00h
24	DivV_A	r/w	VCO1r	divVA6	divVA5	divVA4	divVA3	divVA2	divVA1	divVA0	00h
25	CPcur_A	r/w	CPAh3	CPAh2	CPAh1	CPAh0	CPAl3	CPAl2	CPAl1	CPAl0	00h
26	DAC1_A	r/w	DAC1A8	DAC1A6	DAC1A5	DAC1A4	DAC1A3	DAC1A2	DAC1A1	DAC1A1	00h
27	DAC2_A	r/w	DAC2A8	DAC2A6	DAC2A5	DAC2A4	DAC2A3	DAC2A2	DAC2A1	DAC2A1	00h
28	PLL_DAC_A	r/w	IQselA	VCOsw			DAC2A0	DAC1A0	DAC2off	DAC1off	00h
29	Misc4_A	r/w	WAIT2ms(5)	WAIT2ms(4)	WAIT2ms(3)	WAIT2ms(2)	WAIT2ms(1)	WAIT2ms(0)		MIN16	00h
30		r/w	WAIT0.5ms(5)	WAIT0.5ms(4)	WAIT0.5ms(3)	WAIT0.5ms(2)	WAIT0.5ms(1)	WAIT0.5ms(0)	AGCtest1	AGCtest0	00h
31		r/w	IF test	ADC test	ADCDAC5	ADCDAC4	ADCDAC3	ADCDAC2	ADCDAC1	ADCDAC0	00h
32	AGCtc_B	r/w	this byte is valid on the output if bit SHAGC is set to '1', otherwise byte Nr. 16 is valid on the output								00h
33	AMAGC_B	r/w	all bytes from 33 to 45 are valid on the output if SHPLL is set to '1', otherwise byte 17 to 29 are valid on the output								00h
34	GPIOm_B	r/w									00h
35	IFCTRL_B	r/w									00h
36	AMFilt_B	r/w									00h
37	DivN_B1	r/w									00h
38	DivN_B2	r/w									00h
39	DivN_B3	r/w									00h
40	DivV_B	r/w									00h
41	CPcur_B	r/w									00h
42	DAC1_B	r/w									00h
43	DAC2_B	r/w									00h
44	PLL_DAC_B	r/w									00h
45	Misc4_B	r/w									00h
46											00h
47											00h
48	READ_Status	r	lock		GPIO6r	GPIO5r	MaskMetal1	MaskMetal0	MaskSet1	MaskSet0	00h
49	READ_ADC	r		ADCok	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	00h

6.1 Data byte specification

6.1.1 Short_reg (0)

Table 26. Short_reg (0)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**Global PWR** Power down the IC Power on the IC
						0 1		**GPIO enable** all GPIO in tristate all GPIO enable
					0 1			**ADCen** 6bit ADC on 6bit ADC off
				0 1				**ADCstart** No conversion Starts a single AD conversion
			0 1					**ShPLL** PLL register from 17 to 31 are valid PLL register from 33 to 47 are valid
		0 1						**ShAGC** AGC TC register 16 is valid AGC TC register 32 is valid
	X							**Not used**
X								**Not used**

6.1.2 ADCctrl (1)

Table 27. ADCctrl (1)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Temperature sensor power
							0	Enabled
							1	Disabled
								ADC auto mode
						0		automatic restart disable
						1		automatic restart enable
								RC oscillator enable
					0			enable
					1			disable
				X				**ADCstart (like bit 0.3)**
								ADC input selection
	0	0	0					Temp sensor
	1	0	0					FM AGC
	0	1	0					AM AGC
	1	1	0					IF AGC
	0	0	1					VCO tuning voltage (3/5 * Vtune)
	1	0	1					GP1
	0	1	1					GP2
	1	1	1					2/5 * VCC
								ADC clock selection
0								ADC clock source = RC osc
1								ADC clock source = refdiv output

6.1.3 GPIO mode (2)

Table 28. GPIO mode (2)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**GPIO1 input / output** Analog input to AD converter digital output
						0 1		**GPIO2 input / output** Analog input to AD converter Digital output
					0 1			**CP Current Switch** Automatic switch disabled Automatic switch enabled
				0 1				**GPIO4 input / output** Analog Input digital output
			0 1					**GPIO5 input / output** digital input output (analog or digital)
		0 1						**GPIO6 input / output** digital input (or MISO output in SPI mode) digital output (or MISO output in SPI mode)
	0 1							**GPIO7 input / output** FM AGC voltage output Digital output
0 1								**GPIO8 input / output** AM AGC voltage output Digital output

6.1.4 AGC and mixer control (3)

Table 29. AGC and mixer control (3

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
						0 0 1 1	0 1 0 1	**Mixout 1 / 2** All Off = power down mixer section Mixout 1 active Mixout 2 active Forbidden state
					0 1			**Balun output drive capability** Low drive capability High drive capability
				0 1				**Mixer input FM / AM selection** AM input active FM input active
			0 1					**AM AGC On / Off** Off On
		0 1						**FM AGC On / Off** Off On
	0 1							**Keyed AGC enable** Keyed AGC off keyed AGC on
0 1								**IF input selection FM / AM** IF input AM IF input FM

6.1.5 Register (4)

Table 30. Register (4)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								AMAGC Isink (2mA fixed current)
							0	Off
							1	On
								PLLtest
						0		Off
						1		On
								Disvcc
					0			POR activated from IFVCC
					1			POR non activated from IFVCC
								WAIT60ms
0	0	0	0	0				1ms (min. value)
1	0	1	1	1				60ms (default value)
1	1	1	1	1				80ms (max value)

6.1.6 Divider R (5)

Table 31. Divider R (5)

MSB							LSB	Divider R value
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider R value
							X	DivR0
								:
								:
X								DivR7

6.1.7 IF AGC control (6)

Table 32. IF AGC control (6)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**IF section On / Off** Off On
						0 1		**GPIO 5 output mode** Off On = GPIO 5 analog output enable
				X	X			**Not used**
	0 0 : : 1	0 0 : : 1	0 1 : : 1					**IF AGC threshold** IF output level = 89dBµV(AM) / 91dBµV (FM) IF output level = 90.5dBµV(AM) / 92.5dBµV (FM) : : IF output level = 99dBµV(AM) / 101dBµV (FM)
0 1								**IF AGC mode FM / AM selection** FM mode AM mode

6.1.8 FM AGC (7)

Table 33. FM AGC (7)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Voltage output mode
						0	0	Off
						0	1	N/A
						1	0	Calibration mode
						1	1	Voltage output On
								Current output mode
				0	0			Off
				0	1			Constant 2mA output
				1	0			Positive current output
				1	1			Neg. / Pos. current output
								FM AGC threshold
0	0	0	0					Mixer input level = 93dBµV (FM1) / 97dBµV (FM2)
0	0	0	1					Mixer input level = 94dBµV (FM1) / 98dBµV (FM2)
0	0	1	0					Mixer input level = 95dBµV (FM1) / 99dBµV (FM2)
0	0	1	1					Mixer input level = 96dBµV (FM1) / 100dBµV (FM2)
0	1	0	0					Mixer input level = 97dBµV (FM1) / 101dBµV (FM2)
0	1	0	1					Mixer input level = 98dBµV (FM1) / 102dBµV (FM2)
0	1	1	0					Mixer input level = 99dBµV (FM1) / 103dBµV (FM2)
0	1	1	1					Mixer input level = 100dBµV (FM1) / 104dBµV (FM2)
1	0	0	0					Mixer input level = 93dBµV (FM1) / 97dBµV (FM2)
1	0	0	1					Mixer input level = 92dBµV (FM1) / 96dBµV (FM2)
1	0	1	0					Mixer input level = 91dBµV (FM1) / 95dBµV (FM2)
1	0	1	1					Mixer input level = 90dBµV (FM1) / 94dBµV (FM2)
1	1	0	0					Mixer input level = 89dBµV (FM1) / 93dBµV (FM2)
1	1	0	1					Mixer input level = 88dBµV (FM1) / 92dBµV (FM2)
1	1	1	0					Mixer input level = 87dBµV (FM1) / 91dBµV (FM2)
1	1	1	1					Mixer input level = 86dBµV (FM1) / 90dBµV (FM2)

6.1.9 AGC voltage threshold (8)

Table 34. AGC voltage threshold (8)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Transfer voltage from voltage out to current out
		0	0	0	0	0	0	200mV
		0	0	0	0	0	1	237.5mV
		:	:	:	:	:	:	:
		:	:	:	:	:	:	:
		1	1	1	1	1	0	2.5625V
		1	1	1	1	1	1	2.6V
								AM fast attack
0								Off
1								On

6.1.10 Mixer alignment 1 (9)

Table 35. Mixer alignment 1 (9)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								IQ-filter frequency adjust
					0	0	0	+2.4MHz
					0	0	1	+1.8MHz
					:	:	:	:
					1	0	0	0
					:	:	:	:
					1	1	1	-1.8MHz
								Cascode control loop On / Off
				0				On
				1				Off
								Mixers current control
		0	0					Normal bias
		0	1					Low reduction
		1	0					High reduction
		1	1					N/A
								IFAMP driving capability
0	0							Normal
0	1							Intermediate 1
1	0							Intermediate 2
1	1							High

6.1.11 Mixer alignment 2 (10)

Table 36. Mixer alignment 2 (10)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								IQ-filter gain adjust
				0	1	1	1	-0.7dB
				0	1	1	0	-0.6dB
				0	1	0	1	-0.5dB
				:	:	:	:	:
				0	0	0	0	0dB
				1	0	0	0	0dB
				:	:	:	:	:
				1	1	1	0	+0.6dB
				1	1	1	1	+0.7dB
								IQ-filter phase adjust
0	0	0	0					0
0	0	0	1					+0.2 deg
0	0	1	0					+0.2 deg
0	0	1	1					+0.4 deg
0	1	0	0					+0.6 deg
:	:	:	:					:
0	1	1	1					+1.2 deg
1	0	0	0					-1.2 deg
1	0	0	1					-1.0 deg
1	0	1	0					-1.0 deg
1	0	1	1					-0.8 deg
1	1	0	0					-0.6 deg
:	:	:	:					:
1	1	1	0					-0.2 deg
1	1	1	1					0

6.1.12 PLL control 1 (11)

Table 37. PLL control 1 (11)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**PLL enable** PLL Off PLL On
						0 1		**Divider R enable** Divider R off; = div / 1 Divider R on
					0 1			**Select reference input** Reference frequency input = LVDS Reference frequency input = Xtal
				0 1				**Charge pump current 800µA** 0 µA 800 µA
0 : 1	0 : 1	0 : 1	0 : 1					**Slope of high current CP** highest : lowest

6.1.13 PLL control 2 (12)

Table 38. PLL control 2 (12)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
				0 : 1	0 : 1	0 : 1	0 : 1	**Delay of high current CP** shortest : longest
	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1					**State machine modes decode** Buffer mode Preset Search AF update Jump Check Load End
0 1								**Register functionality control** Normal/shadow mode Buffer/control mode

6.1.14 PLL test (13)

Table 39. PLL test (13)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
			X	X	1	0		**PLL test** Set to default
	0	1						**PFD** default
0								**PFD polarity**

6.1.15 Misc 2 (14)

Table 40. Misc 2 (14)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
						0 0 1 1	0 1 0 1	**VCO magnitude** 1V 2V 3V 4V
				0 0 1 1	0 1 0 1			**Oscillation frequency of RC oscillator** 0.68 MHz 1.31 MHz 1.92 MHz 2.49 MHz
			0 1					**IFAMP current control** Normal bias High current mode bias
		0 1						**Reg48sel** ShAGC and ShPLL on D48<1:0> MaskMetal and MaskSet on D48<1:0>
	0 1							**EnSMOOTH** Smooth disabled Smooth enabled
0 1								**IFAGC control when IN4 selected** Normal Thresholds shift

6.1.16 WAIT LOCK (15)

Table 41. WAIT LOCK (15)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								TEST
						0	0	D18<0>
						0	1	LOCK_bit
						1	0	CMPout
						1	1	VdivOUT
								WAIT LOCK
0	0	0	0	0				0.04ms (min. value)
0	0	1	1	0				1ms (default value)
1	1	1	1	1				5.08ms (default value)

6.1.17 AGC time constant settings (16 / 32)

Table 42. AGC time constant settings (16 / 32)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								FM AGC decay time constant
						0	0	D1
						0	1	D2
						1	0	D3
								FM AGC attack time constant
				0	0			A1
				0	1			A2
				1	0			A3
								AM AGC time constant
		0	0					T1
		0	1					T2
		1	0					T3
								IF AGC time constant FM
	0							U1
	1							U2
								IF AGC time constant AM
0								S1
1								S2

6.1.18 AMAGC control (17 / 33)

Table 43. AMAGC control (17 / 33

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								AM AGC voltage output mode
						0	0	Off
						0	1	Voltage output / sense internal
						1	0	Calibration
						1	1	Voltage output / sense external
								AM AGC current output mode
				0	0			Off
				0	1			Constant 2mA
				1	0			Positive current
				1	1			N/A
								AM AGC thresholds
0	0	0	0					Mixer input level = 94 dBµV
0	0	0	1					Mixer input level = 95 dBµV
0	0	1	0					Mixer input level = 96 dBµV
0	0	1	1					Mixer input level = 97 dBµV
0	1	0	0					Mixer input level = 98 dBµV
0	1	0	1					Mixer input level = 99 dBµV
0	1	1	0					Mixer input level = 100 dBµV
0	1	1	1					Mixer input level = 101 dBµV
1	0	0	0					Mixer input level = 94 dBµV
1	0	0	1					Mixer input level = 93 dBµV
1	0	1	0					Mixer input level = 92 dBµV
1	0	1	1					Mixer input level = 91 dBµV
1	1	0	0					Mixer input level = 90 dBµV
1	1	0	1					Mixer input level = 89 dBµV
1	1	1	0					Mixer input level = 88 dBµV
1	1	1	1					Mixer input level = 87 dBµV

6.1.19 GPIO output level control (18 / 34)

Table 44. GPIO output level control (18 / 34)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0	**GPIOx high / low output level**
							1	GPIO1 low
								GPIO1 high
						0		GPIO2 low
						1		GPIO2 high
	:	:	:	:	:			:
	X	X	X	X	X			GPIOx low / high
	:	:	:	:	:			:
0								GPIO8 low
1								GPIO8 high

6.1.20 IF control (19 / 35)

Table 45. IF control (19 / 35)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**Not used**
								RC test
						0		Test enabled
						1		Test disabled
								AMAGC input buffer
					0			Buffer enabled
					1			Buffer disabled
								Mixer input selection for FM
				0				FM1 mixer input
				1				FM2 mixer input
								IF amplifier Gain
	0	0	0					25dB (input1-3) / 19dB (input4)
	0	0	1					27dB (input1-3) / 21dB (input4)
	:	:	:					:
	1	1	0					37dB (input1-3) / 31dB (input4)
	1	1	1					39dB (input1-3) / 33dB (input4)
								IF input selection analog / IBOC
0								IBOC
1								Analog

6.1.21 AF state machine wait time 1 (20 / 36)

Table 46. AF state machine wait time 1 (20 / 36)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**Not used**
						X		**Not used**
0 0	0 0	0 1	0 1	0 0	0 0			**WAIT 1ms** 0.04ms (min. value) 1ms (default value)

6.1.22 PLL main divider (N-divider) 1 (21 / 37)

Table 47. PLL main divider (N-divider) 1 (21 / 37)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider N value
							X	M8
						X		M9
					X			M10
				X				M11
			X					M12
		X						M13
	X							M14
X								M15

6.1.23 PLL main divider (N-divider) 2 (22 / 38)

Table 48. PLL main divider (N-divider) 2 (22 / 38)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider N value
							X	M0
						X		M1
					X			M2
				X				M3
			X					M4
		X						M5
	X							M6
X								M7

6.1.24 PLL main divider (N-divider) 3 (23 / 39)

Table 49. PLL main divider (N-divider) 3 (23 / 39)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
				X				**Divider N value**
			X					A0
		X						A1
	X							A2
X								A3
								A4

6.1.25 PLL Divider ratio calculation

Table 50. PLL Divider ratio calculation

M counter							A counter					Notes
M16	M15	…	M7	…	M1	M0	A4	A3	A2	A1	A0	N= 32*P + A M=32 N= M*P + A M>32 (P=32)

6.1.26 VCO divider (V-divider) (24 / 40)

Table 51. VCO divider (V-divider) (24 / 40)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**Divider V value**
						X		V0
					X			V1
				X				V2
			X					V3
		X						V4
	X							V5
								V6
								VCO range selection
0								Range 2
1								Range 1

6.1.27 Charge pump current (25 / 41)

Table 52. Charge pump current (25 / 41)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**Low current charge pump** 50 µA
						X		100 µA
					X			200 µA
				X				400 µA
			X					**High current charge pump** 0.5 mA
		X						1mA
	X							2mA
X								4mA

6.1.28 Tuning DAC 1 (26 / 42)

Table 53. Tuning DAC 1 (26 / 42)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**DAC 1 voltage 8..1** DAC1_.
						X		DAC1_2
					X			DAC1_3
				X				DAC1_4
			X					DAC1_5
		X						DAC1_6
	X							DAC1_7
X								DAC1_8

6.1.29 Tuning DAC 2 (27 / 43)

Table 54. Tuning DAC 2 (27 / 43)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**DAC 2 voltage 8..1** DAC2_1
						X		DAC2_2
					X			DAC2_3
				X				DAC2_4
			X					DAC2_5
		X						DAC2_6
	X							DAC2_7
X								DAC2_8

6.1.30 DAC output voltage = 600mV + DACval * 9mV

6.1.31 Different controls (28 / 44)

Table 55. Different controls (28 / 44)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**DAC 1 On / Off** Off On
						0 1		**DAC 2 On / Off** Off On
					X			**DAC 1_0**
				X				**DAC 2_0**
		X	X					**Not used**
	X							**Not used**
0 1								**IQ phase select** I anticipates Q Q anticipates I

6.1.32 Misc 3 (29 / 45)

Table 56. Misc 3 (29 / 45)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**PLL N divider MSB** M16
						X		**Not used**
0 0 1	0 1 1	0 1 1	0 0 1	0 0 1	0 1 1			**WAIT 2ms** 0.08ms (min. value) 2ms (default value) 5.04ms (default value)

6.1.33 Analog test select (30 / 46)

Table 57. Analog test select (30 / 46)

MSB						LSB		Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
						0 0 1 1	0 1 0 1	**Analog test output signal select** IF AGC FM AGC AMAGC DAC voltage of ADC
0 0 1	0 0 1	0 0 1	0 1 1	0 1 1	0 0 1			**WAIT 0.5ms** 0.02ms (min. value) 0.5ms (default value) 5.06ms (max value)

6.1.34 AD converter test (31 / 47)

Table 58. AD converter test (31 / 47)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
		X	X	X	X	X	X	**ADC DAC direct programming** DAC 0 DAC 1 DAC 2 DAC 3 DAC 4 DAC 5
	0 1							**ADC test enable** Off On
0 1								**AGC test enable** Off On

6.1.35 Read 1 (48)

Table 59. Read 1 (48)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
						0 0 1 1	0 1 0 1	**Mask set revision** A B C D
				0 0 1 1	0 1 0 1			**Metal mask revision** A B C D
			0 1					**GPIO 5 level** low high
		0 1						**GPIO 6 level** low high

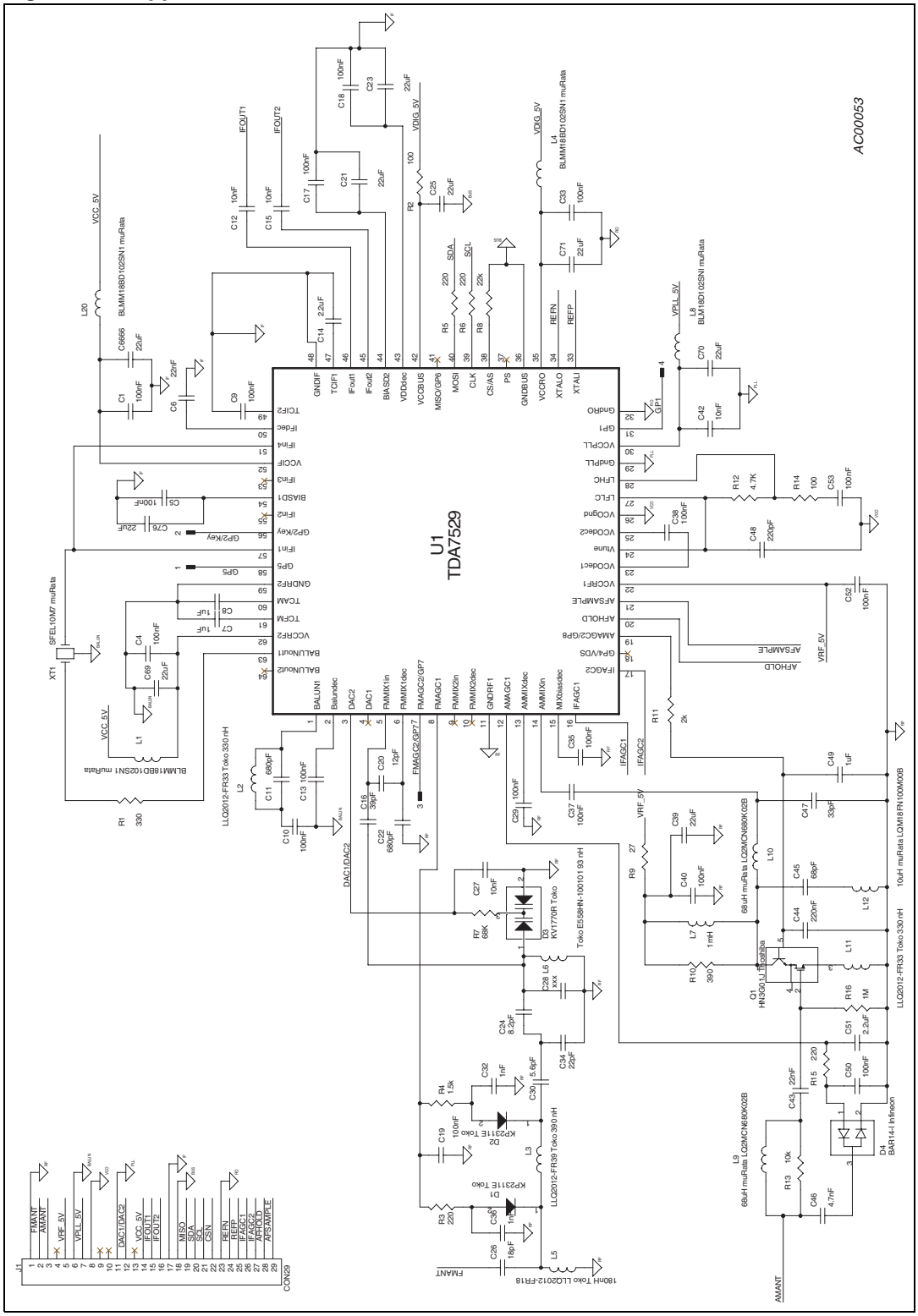
6.1.36 Read 2 (49)

Table 60. Read 2 (49)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							X	**AD converter result** ADC0
						X		ADC1
					X			ADC2
				X				ADC3
			X					ADC4
		X						ADC5
								AD converter result status
	0							Not OK
	1							OK

7 Application schematic

Figure 17. Application schematic



8 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

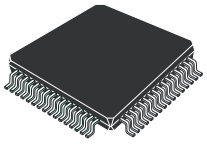
ECOPACK specifications are available at: www.st.com.

Figure 18. LQFP64 (10x10x1.4mm) exposed pad down mechanical data and package dimensions (exposed pad size for D2 and E2: 4.5mm max.)

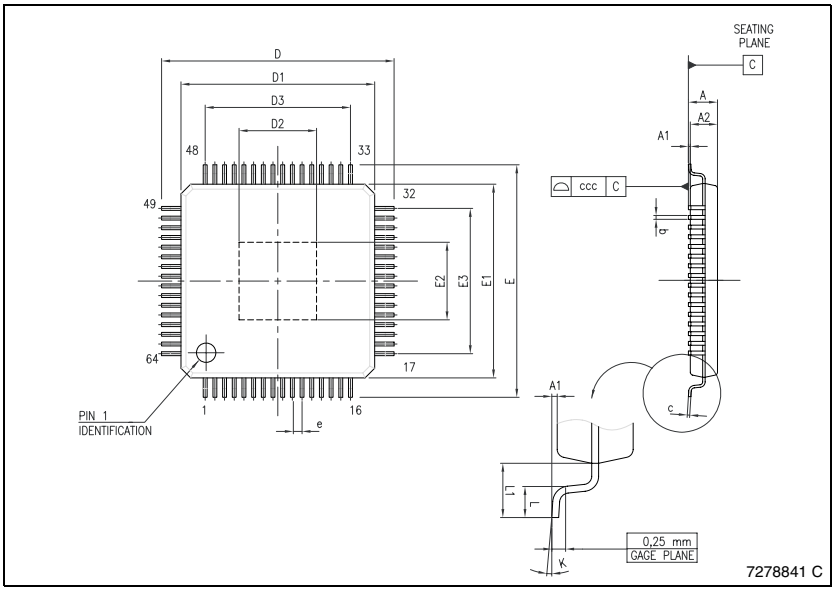
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D2	According to Pad size					
D3		7.500			0.2953	
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E2	According to Pad size					
E3		7.500			0.2953	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k		3.500	7.000		0.1378	0.2756
ccc			0.080			0.0031

Note: 1. Exact shape of each corner is optional.

OUTLINE AND MECHANICAL DATA



LQFP64 (10x10x1.4mm) Exposed Pad Down



9 Revision history

Table 61. Document revision history

Date	Revision	Changes
7-Mar-2007	1	Initial release.

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