# STS9D8NH3LL

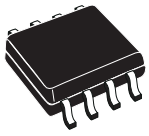
## Dual N-channel 30V - 0.012Ω - 9A SO-8
## Low on-resistance STripFET™ Power MOSFET

**PRELIMINARY DATA**

## General features

| Type | | $V_{DSS}$ | $R_{DS(on)}$ | Qg | $I_D$ |
|---|---|---|---|---|---|
| STS9D8NH3LL | $Q_1$ | 30V | < 0.022Ω | 7nC | 8A |
| | $Q_2$ | 30V | < 0.015 | 9nC | 9A |

- Optimal $R_{DS}$(on) x Qg trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

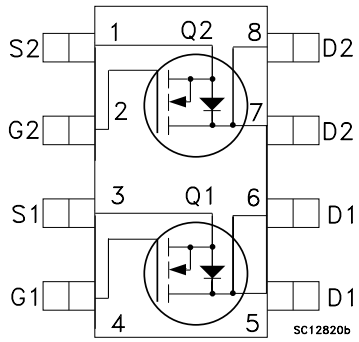


**S0-8**

## Description

This device uses the latest advanced design rules of ST's STrip based technology. The Q1 and Q2 transistors, show respectively, the best gate charge and on-resistance for minimizing the switching and conduction losses. This application specific Power MOSFET has been designed to replace two SO-8 packages in DC-DC converters.

## Internal schematic diagram




## Applications

- Switching application

## Order codes

| Part number | Marking | Package | Packaging |
|---|---|---|---|
| STS9D8NH3LL | 9D8H3LL- | SO-8 | Tape & reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Type | Value | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($v_{GS}$ = 0) | $Q_1$<br>$Q_2$ | 30<br>30 | V<br>V |
| $V_{GS}$ | Gate- source voltage | $Q_1$<br>$Q_2$ | ±16<br>±16 | V<br>V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25°C | $Q_1$<br>$Q_2$ | 8<br>9 | A<br>A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100°C | $Q_1$<br>$Q_2$ | 5<br>5.6 | A<br>A |
| $I_{DM}$ (1) | Drain current (pulsed) | $Q_1$<br>$Q_2$ | 32<br>36 | A<br>A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | $Q_1$<br>$Q_2$ | 2<br>2 | W<br>W |

1. Pulse width limited by safe operating area

**Table 2. Thermal data**

| | | | |
|---|---|---|---|
| $R_{thj\text{-}a}$ | (1)Thermal resistance junction-ambient max | 62.5 | °C/W |
| $T_J$ | Thermal operating junction-ambient | 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10s

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 3. On/off states**

| Symbol | Parameter | Test conditions | Type | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | $Q_1$<br>$Q_2$ | 30<br>30 | | | V<br>V |
| $I_{DSS}$ | Zero gate voltage Drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating | $Q_1$<br>$Q_2$ | | | 1<br>1 | µA<br>µA |
| $I_{DSS}$ | Zero gate voltage Drain current ($V_{GS}$ = 0) | $V_{DS}$ =Max rating @125°C | $Q_1$<br>$Q_2$ | | | 10<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 16V | $Q_1$<br>$Q_2$ | | | ±100<br>±100 | nA<br>nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | $Q_1$<br>$Q_2$ | 1<br>1 | | | V<br>V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10V, $I_D$ = 4A<br>$V_{GS}$ = 10V, $I_D$ = 4.5A | $Q_1$<br>$Q_2$ | | 0.018<br>0.012 | 0.022<br>0.015 | Ω<br>Ω |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 4.5V, $I_D$ = 4A<br>$V_{GS}$ = 4.5V, $I_D$ = 4.5A | $Q_1$<br>$Q_2$ | | 0.020<br>0.014 | 0.025<br>0.0175 | Ω<br>Ω |

**Table 4. Dynamic**

| Symbol | Parameter | Test conditions | Type | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | $Q_1$<br>$Q_2$ | | 857<br>965 | | pF<br>pF |
| $C_{oss}$ | Output capacitance | | $Q_1$<br>$Q_2$ | | 147<br>285 | | pF<br>pF |
| $C_{rss}$ | Reverse transfer capacitance | | $Q_1$<br>$Q_2$ | | 20<br>38 | | pF<br>pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 15V, $I_D$ = 8A, $V_{GS}$ = 5V *(see Figure 2)* | $Q_1$<br>$Q_2$ | | 7<br>9 | 10<br>12 | nC<br>nC |
| $Q_{gs}$ | Gate-source charge | | $Q_1$<br>$Q_2$ | | 2.5<br>3.7 | | nC<br>nC |
| $Q_{gd}$ | Gate-drain charge | | $Q_1$<br>$Q_2$ | | 2.3<br>3 | | nC<br>nC |

**Table 5. Switching times**

| Symbol | Parameter | Test conditions | Type | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$=15 V, $I_D$=4A, $R_G$=4.7Ω, $V_{GS}$= 4.5V *(see Figure 4)* | $Q_1$ | | 12 | | ns |
| | | | $Q_2$ | | 15 | | ns |
| $t_r$ | Rise time | | $Q_1$ | | 14.5 | | ns |
| | | | $Q_2$ | | 32 | | ns |
| $t_{d(off)}$ | Turn-off delay time | $V_{DD}$=15 V, $I_D$=4A, $R_G$=4.7Ω, $V_{GS}$= 4.5V *(see Figure 4)* | $Q_1$ | | 23 | | ns |
| | | | $Q_2$ | | 18 | | ns |
| $t_f$ | Fall time | | $Q_1$ | | 8 | | ns |
| | | | $Q_2$ | | 8.5 | | ns |

**Table 6. Source drain diode**

| Symbol | Parameter | Test conditions | Type | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | $V_{DD}$=15V, $I_D$=4A $R_G$=4.7Ω, $V_{GS}$=4.5V | $Q_1$ | | | 8 | A |
| | | | $Q_2$ | | | 9 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | $V_{DD}$=15V, $I_D$=4A $R_G$=4.7Ω, $V_{GS}$=4.5V | $Q_1$ | | | 32 | A |
| | | | $Q_2$ | | | 36 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 8A, $V_{GS}$ = 0 | $Q_1$ | | | 1.5 | V |
| | | | $Q_2$ | | | 1.3 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 8A, $V_{DD}$ = 15V di/dt = 100A/µs, $T_j$ = 150°C *(see Figure 3)* | $Q_1$ | | 15 | | ns |
| | | | $Q_2$ | | 24 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | $Q_1$ | | 5.7 | | nC |
| | | | $Q_2$ | | 17.4 | | nC |
| $I_{RRM}$ | Reverse recovery current | | $Q_1$ | | 0.76 | | A |
| | | | $Q_2$ | | 1.54 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

# 3 Test circuit

**Figure 1. Switching times test circuit for resistive load**

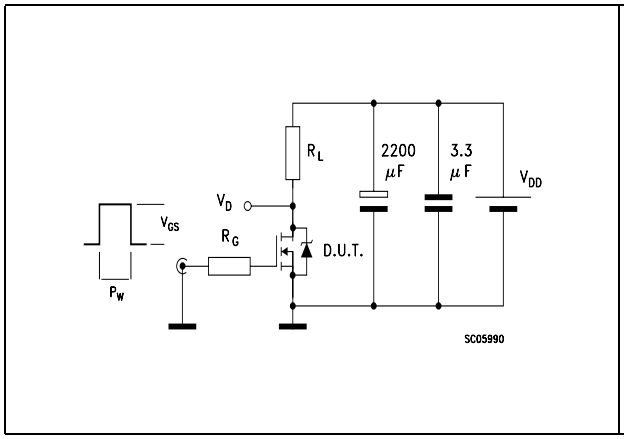



**Figure 2. Gate charge test circuit**

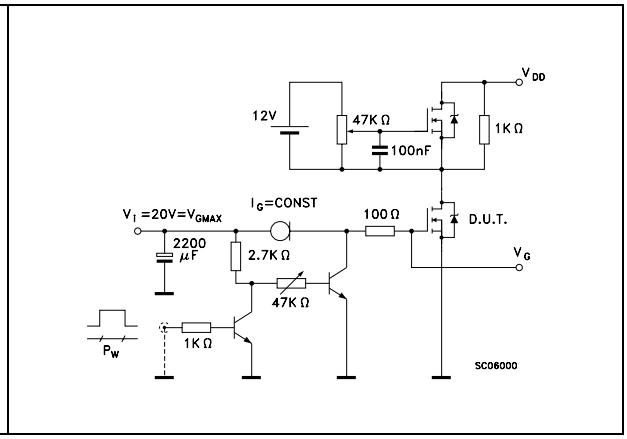



**Figure 3. Test circuit for inductive load switching and diode recovery times**

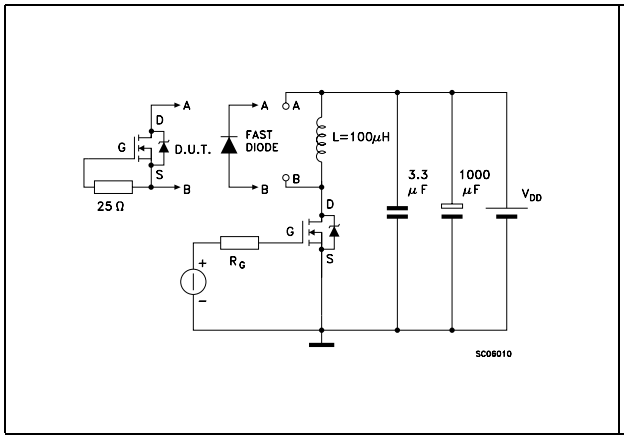



**Figure 4. Unclamped Inductive load test circuit**

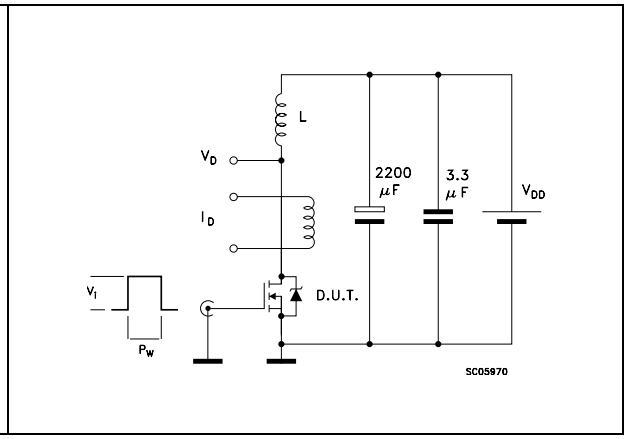



**Figure 5. Unclamped inductive waveform**

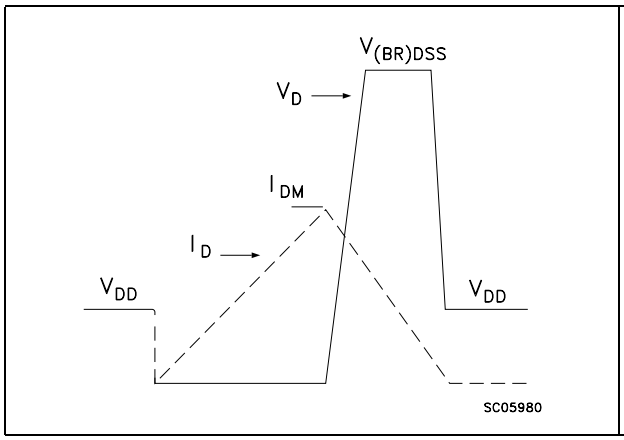
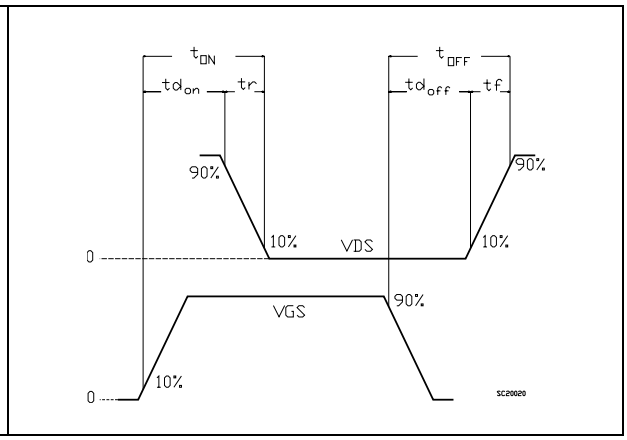



**Figure 6. Switching time waveform**

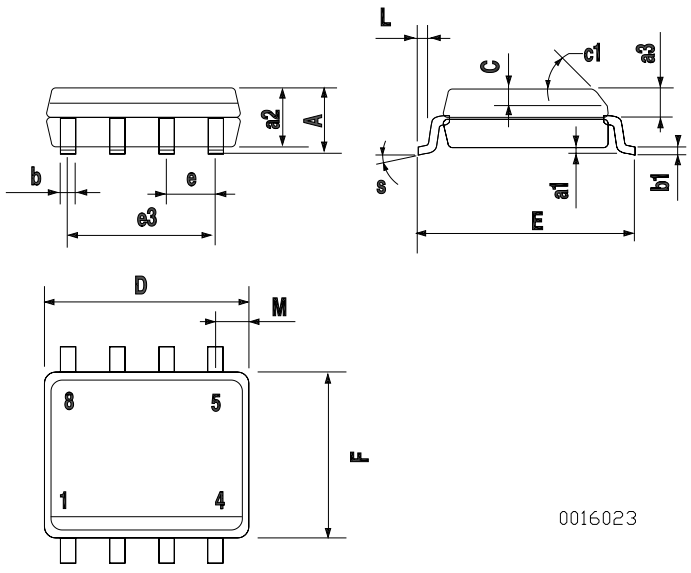


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

## SO-8 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.003 | | 0.009 |
| a2 | | | 1.65 | | | 0.064 |
| a3 | 0.65 | | 0.85 | 0.025 | | 0.033 |
| b | 0.35 | | 0.48 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.019 |
| c1 | 45 (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.188 | | 0.196 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.14 | | 0.157 |
| L | 0.4 | | 1.27 | 0.015 | | 0.050 |
| M | | | 0.6 | | | 0.023 |
| S | 8 (max.) | | | | | |



# 5 Revision history

**Table 7. Revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jan-2007 | 1 | First release |
| 06-Mar-2007 | 2 | Some value changed on *Table 3* ($R_{DS(on)}$ for Q2) |

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