STL6NM60N

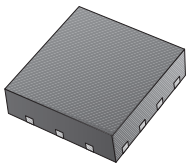
N-channel 600V - 0.85Ω - 5.75A - PowerFLAT™ (5x5) Ultra low gate charge MDmesh™ II Power MOSFET

Features

Type	V_{DSS} @ T_{JMAX}	$R_{DS(on)}$	I_D
STL6NM60N	650V	<0.92Ω	5.75A(1)

1. The value is rated according Rthj-case

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

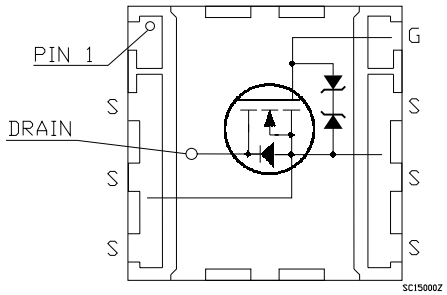


PowerFLAT (5x5)

Description

This series of devices implements the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Internal schematic diagram



Application

- Switching application

Order code

Part number	Marking	Package	Packaging
STL6NM60N	L6NM60N	PowerFLAT™ (5x5)	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25°C (steady state)	5.75	A
I_D (1)	Drain current (continuous) at T_C=100°C	3.62	A
I_{DM} (1),(2)	Drain current (pulsed)	23	A
I_D (3)	Drain current (continuous) at T_C = 25°C	1	A
I_D (3),(2)	Drain current (continuous) at T_C=100°C	0.65	A
I_{DM} (1), (2)	Drain current (pulsed)	4	A
P_{TOT} (3)	Total dissipation at T_C = 25°C (steady state)	2.1	W
P_{TOT} (1)	Total dissipation at T_C = 25°C (steady state)	70	W
	Derating factor (3)	0.02	W/°C
dv/dt (4)	Peak diode recovery voltage slope	5	V/ns
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	°C

1. The value is rated according Rthj-case
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of 1inch², 2oz Cu
4. $I_{SD} \leq 4.6A$, dv/dt ≤ 400A/µs, $V_{DD} = 80\%V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Typ	Max	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	--	1.8	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.2	58.5	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec

Table 3. Avalanche characteristics

Symbol	Parameter	Typ	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (1)	2	A
E_{AS}	Single pulse avalanche energy (2)	65	mJ

1. Pulse width limited by Tjmax
2. Starting Tj = 25°C, $I_D = I_{AS}$, V_{DD} = 50V

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	600			V
dv/dt (1)	Drain-source voltage slope	V_{DD}= 480V, V_{GS} = 10V, I_D = 4.6A		40		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 2.3A		0.85	0.92	Ω

1. Characteristics value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 2.3A		4		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =50V, f=1 MHz, V_{GS}=0		420 30 4		pF pF pF
$C_{oss\ eq.}$ (2)	Output equivalent capacitance	V_{GS} =0V, V_{DS} =0V to 480V		70		pF
Rg	Gate input resistance	f=1MHz Gate DC Bias=0 test signal level=20mV open drain		6		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=480V, I_D = 4.6A V_{GS} =10V *(see Figure 14)*		13 2 7		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 300V, I_D = 2.3A, R_G= 4.7Ω, V_{GS} = 10V *(see Figure 13)*		10 8 40 9		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				1	A
I_{SDM} (1), (2)	Source-drain current (pulsed)				4	A
V_{SD}(3)	Forward on voltage	I_{SD}= 4.6A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 4.6A, di/dt = 100A/µs, V_{DD}=20V, Tj= 25°C *(see Figure 15)*		300 2 12		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 4.6A, di/dt = 100A/µs, V_{DD}=20V, Tj= 150°C *(see Figure 15)*		470 3 12		ns nC A

1. Pulse width limited by safe operating area
2. When mounted on FR-4 board of 1inch², 2oz Cu
3. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

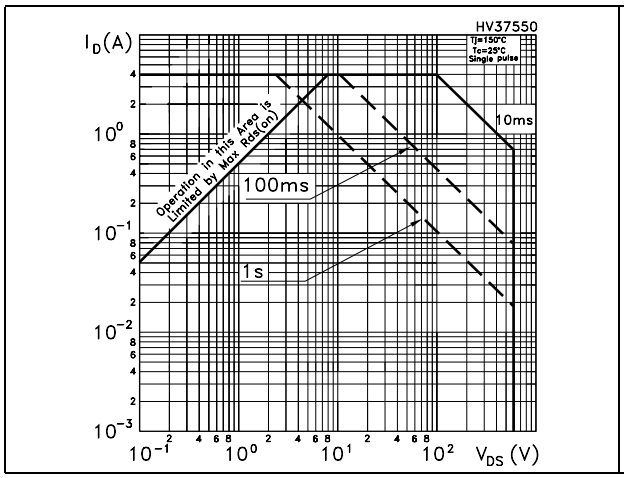


Figure 2. Thermal impedance

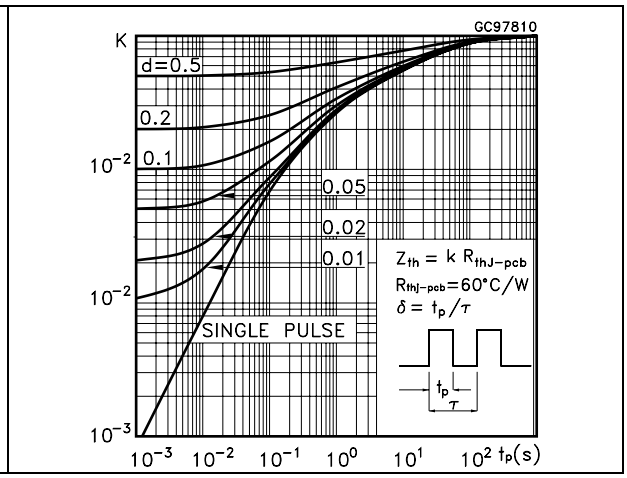


Figure 3. Output characteristics

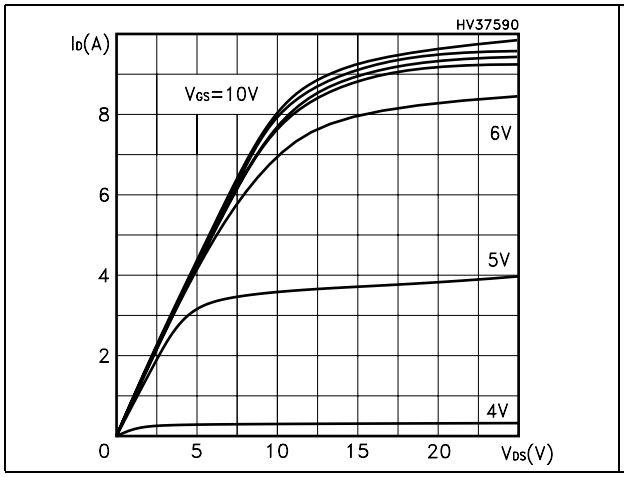


Figure 4. Transfer characteristics

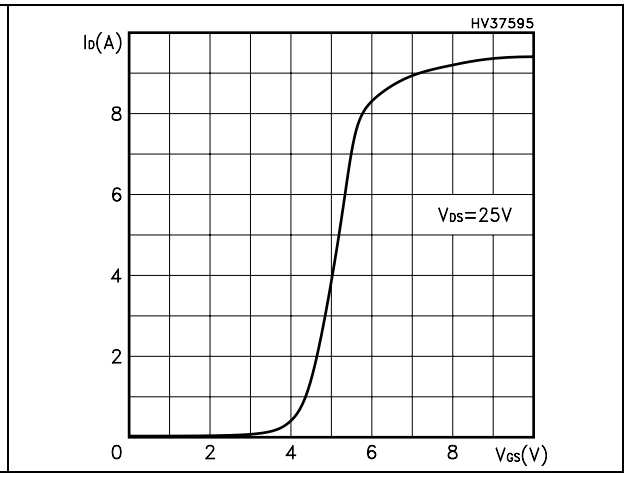


Figure 5. Transconductance

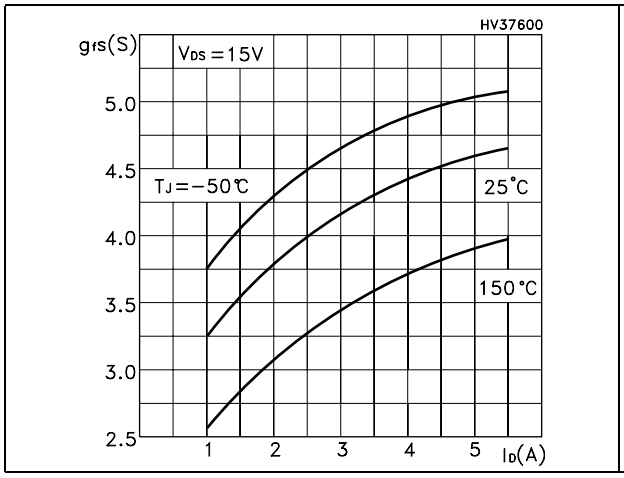


Figure 6. Static drain-source on resistance

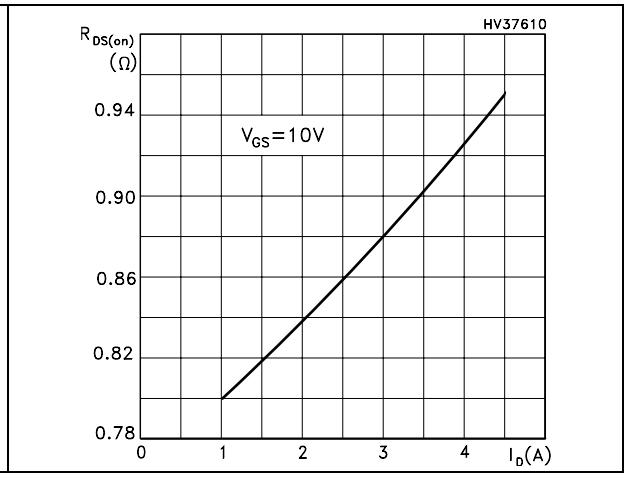


Figure 7. Gate charge vs gate-source voltage

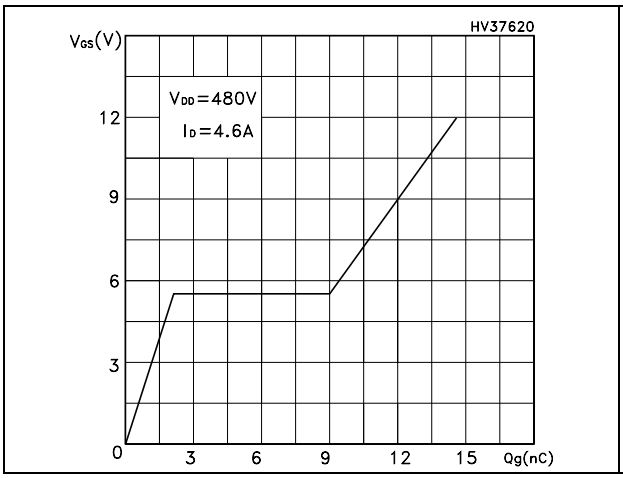


Figure 8. Capacitance variations

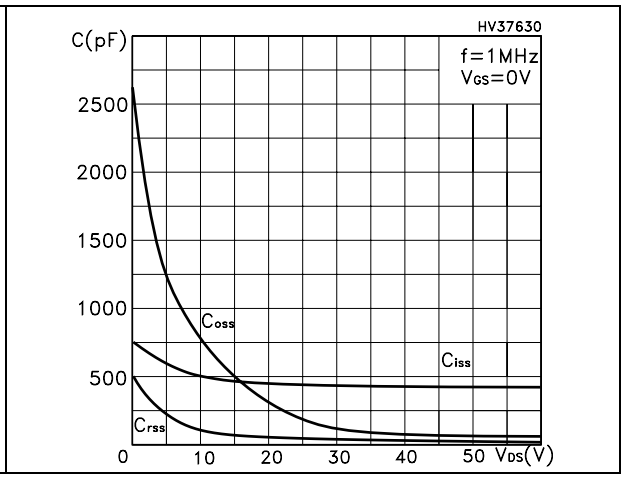


Figure 9. Normalized gate threshold voltage vs temperature

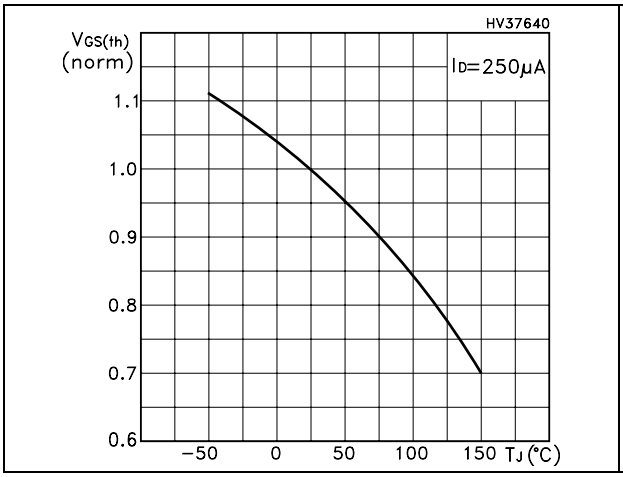


Figure 10. Normalized on resistance vs temperature

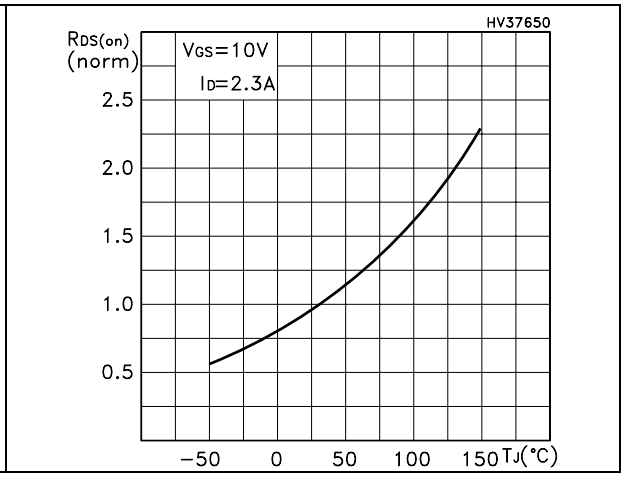


Figure 11. Source-drain diode forward characteristics

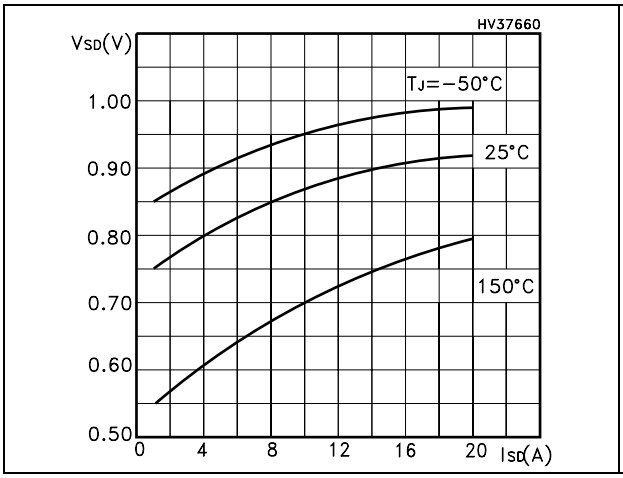
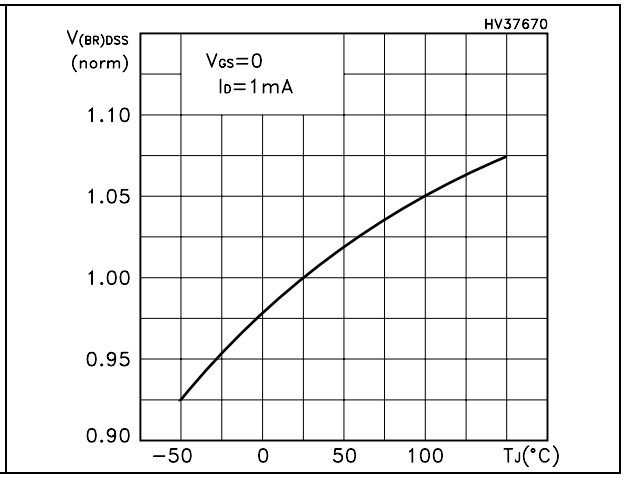


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

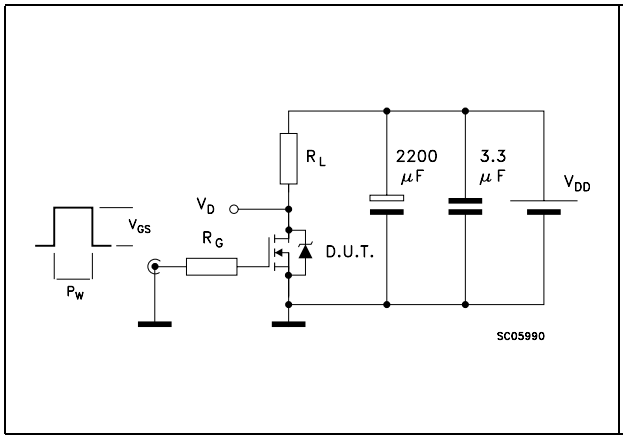


Figure 14. Gate charge test circuit

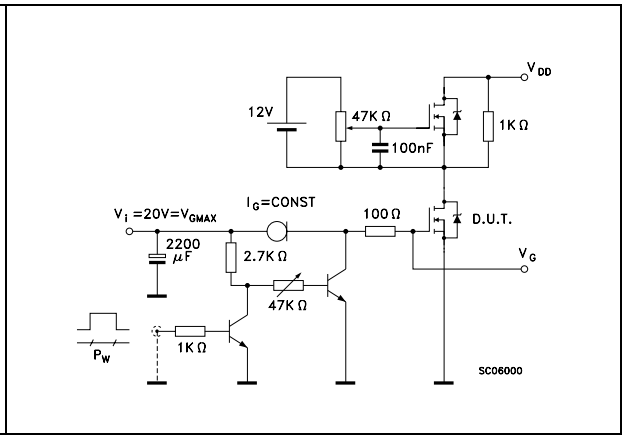


Figure 15. Test circuit for inductive load switching and diode recovery times

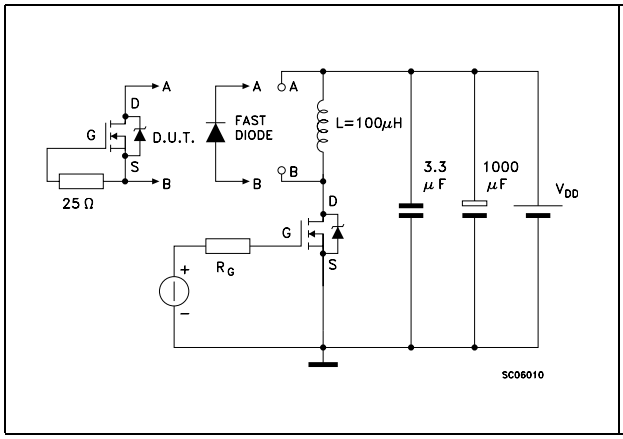


Figure 16. Unclamped inductive load test circuit

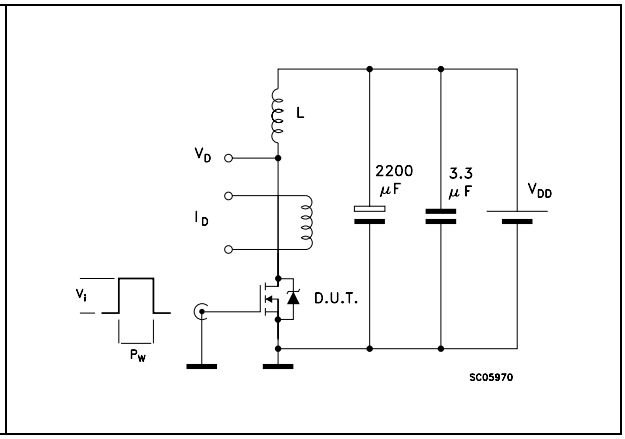


Figure 17. Unclamped inductive waveform

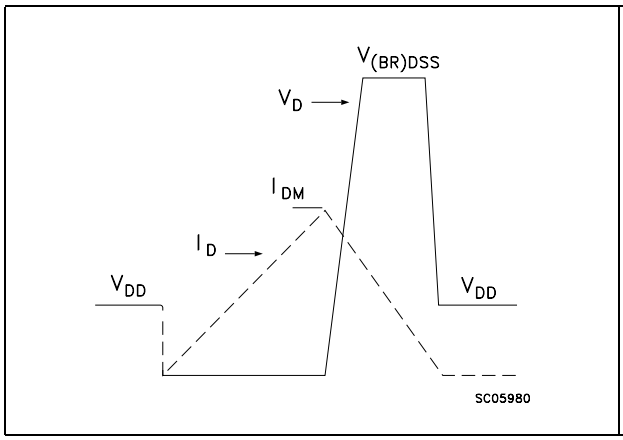
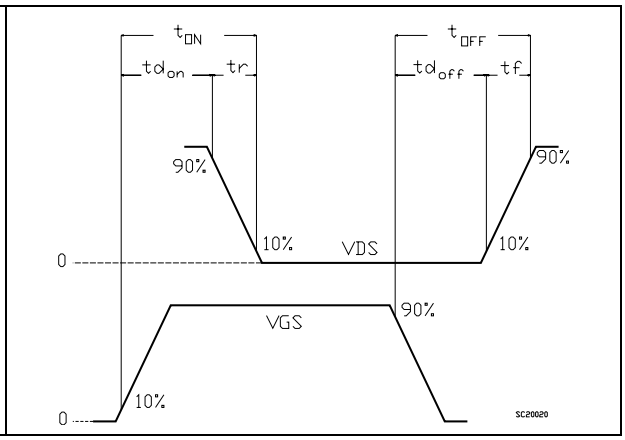


Figure 18. Switching time waveform

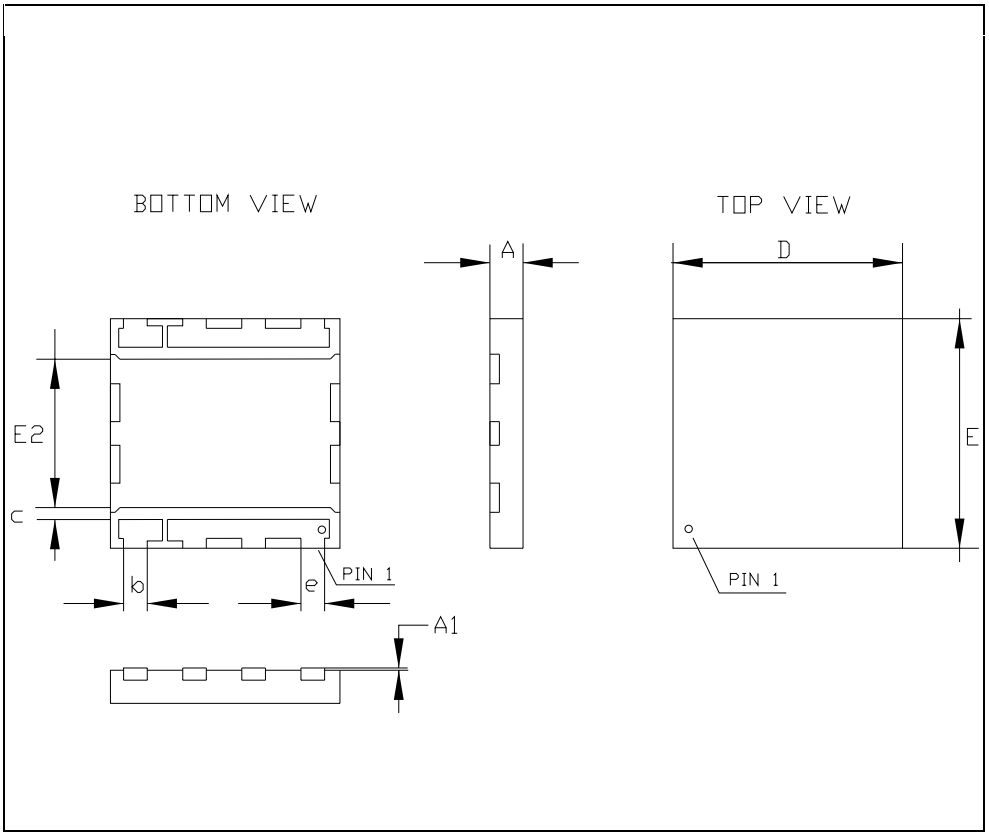


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

PowerFLAT™(5x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
e		1.27			0.050	



5 Revision history

Table 8. Revision history

Date	Revision	Changes
04-May-2007	1	First release
23-May-2007	2	Update test conditions on *Table 6*

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